SiT6700EBB Evaluation Board User Manual

Contents

1 Introduction

The SiT6700EBB evaluation board provides the ability to evaluate the functionality of the 32 kHz oscillators on a simple board that makes it easy to power up the oscillator and observe the output buffered through an operational amplifier. The analog buffer isolates the device from the significant loading, which is important for performing best waveform and current measurements.

The SiT6700EBB supports the following products:

Base Part Number	Type	Output frequency	Package
SiT1630	XO	32.768, 16.384 kHz	2.9 x 2.8 mm SOT23-5
SiT1631	XO	32.768 kHz	2.9 x 2.8 mm SOT23-5

EVB Features

- Support for all device configuration modes: XO
- SMA output for direct or buffered connection to measurement equipment
- Probing points for accurate waveform measurement

SiTime typically ships the EVB with the XO mounted using SiTime recommended reflow profile. The device should only be evaluated in its original soldered down state for best signal integrity and frequency stability. The device performance is not guaranteed if it is de-soldered and then re-soldered either manually or via reflow process.

2 I/O Descriptions

Table 1. SiT6700EBB I/O

Connector designator	I/O	Description
J2	**Power Supply**	Two-pin connector for DC power supply.
J3	**Buffer power**	Three-pin connector for DC buffer power supply. The operational amplifier requires a dual power supply and should be -2.5V for negative power rail (V-) and +7.5V for the positive supply (V+).
J1	**Buffered Output**	Buffered output through SMA connector. The test points for active probe are placed closely to the oscillator output for better signal integrity (see Figure A2). Section 3.2 describes in details the recommended measurement configurations.
J6	**Output**	Direct OUT output through two-pin connector.
J4	**Current measurement**	Two-pin connector for current measurement.

3 EVB Usage Descriptions

3.1 EVB Configurations

This EVB uses an operational amplifier to buffer the oscillator clock output to make it easy to connect to test and measurement equipment through SMA cables without loading the ultra-low power clock output driver. The ADA4817-1 FET operational amplifier is used in a unity gain buffer configuration. It is a unity-gain stable, ultra-high speed, voltage feedback amplifier with FET inputs.

The test points for active probe are placed closely to the oscillator output for better signal integrity (see Figure A2).

Figure A1 in Appendix A shows the complete electrical schematic of SiT6700EBB. Components labeled "DNP" are not assembled.

Shipment Configuration

SiT6700EBB is shipped configured for buffered output allowing connecting it to the instrument input using 50 Ω coax cable. Details on the board assembly for shipment configuration can be found on the schematic (see Figure A1 in Appendix A).

3.2 Waveform Capturing Using Active Probe

SiTime XO is a high-speed logic output device. It is critical that the proper logic and high frequency measurement techniques are used along with the high-quality active probe to ensure best measurement results.

SiTime recommends the following minimum equipment for proper clock waveform measurement.

1) 4 GHz or higher active probe with capacitance <1 pF, such as a Keysight 1134B;
2) Oscilloscope with 4 GHz bandwidth or higher such as a Keysight DSA90604A.

A passive voltage probe should not be used as it adds a high capacitive load to the part and the long ground lead clip is not suitable for high frequency measurement applications. The inductance of the long ground lead coupled with the input capacitance of the probe results in a resonant circuit. The consequence of this resonance results in the distortion of the clock signal. Typical manifestations of this distortion include ringing, overshoot, and undershoot of the clock signal.

Eliminating such distortion requires a probe with the lowest input capacitance and a low inductance ground lead. In addition, SiTime XOs are typically configured for fast rise and fall times with 15 pF load. It is therefore critical that the probe tip ground be as short as possible, lowest inductance, and the return path for the ground be located as close as possible to the trace carrying the RF logic signal.

The buffer can be bypassed, and the output can be directly observed thru J6 2mm pitch pin header connector (Figure 1) or using test point TP1 (see Figures A1-A2 of Appendix A for test points arrangement on the board).

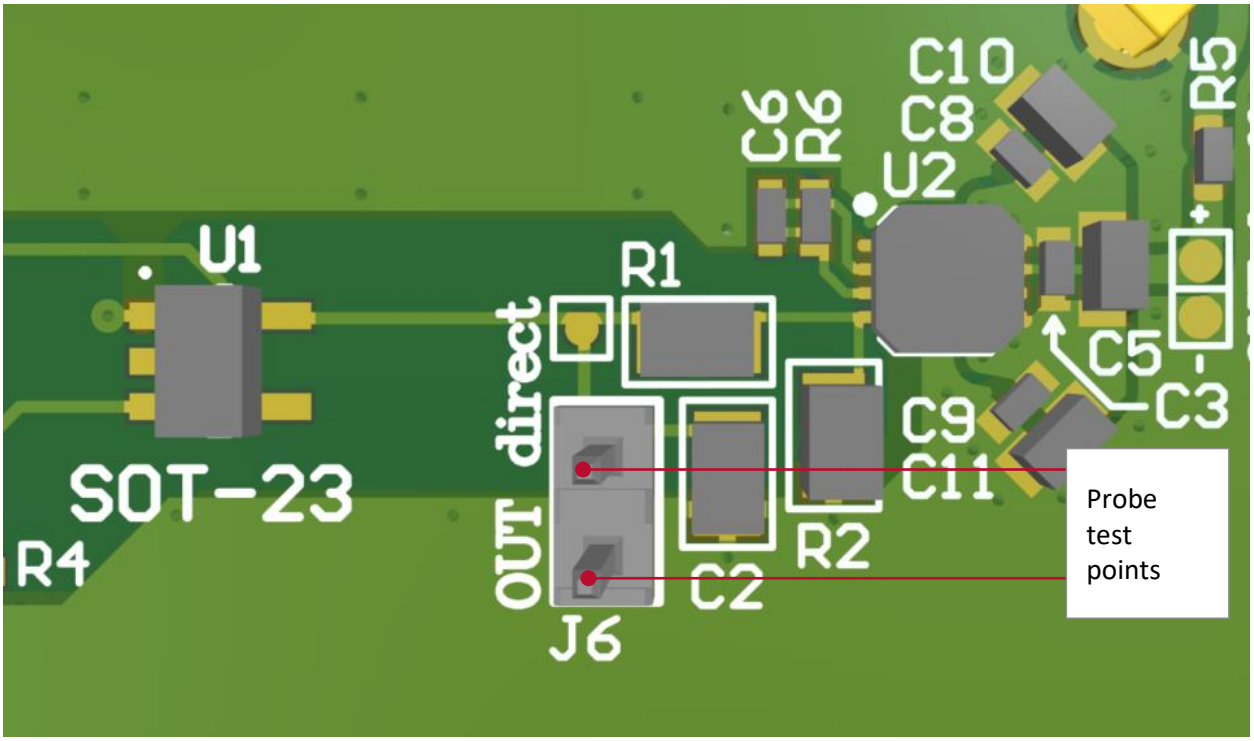

Figure 1: Recommended points for soldering probe head

More details on the SiTime recommendations on the oscillator's output probing can be found in AN10028.

3.3 Measuring Jitter and Phase Noise

For Jitter measurements or phase noise measurements with evaluation boards, SiTime recommends using SMA support Configuration to connect the device output directly to external equipment, such as Time Interval Analyzer (TIA) or high-bandwidth real-time oscilloscope. Jitter measurement technique is described in SiTime AN10007.

The SMA can also be connected through 50 Ω coaxial cable to signal source analyzers or spectrum analyzers to measure phase noise. In such case the use of AC-coupling configuration is recommended because not all measurement instruments can accept DC voltage at their inputs.

3.4 Current Measurement

To measure the current consumption, user need to use ammeter/multi-meter in the power supply circuit. Simply remove jumper resistor R3 across 2-pin connector J4. It is recommended to measure the voltage on DUT VDD and adjust for any drop on the DMM to ensure known VDD voltage on the device. VDD adjustment must be completed before every current measurement.

Appendix A

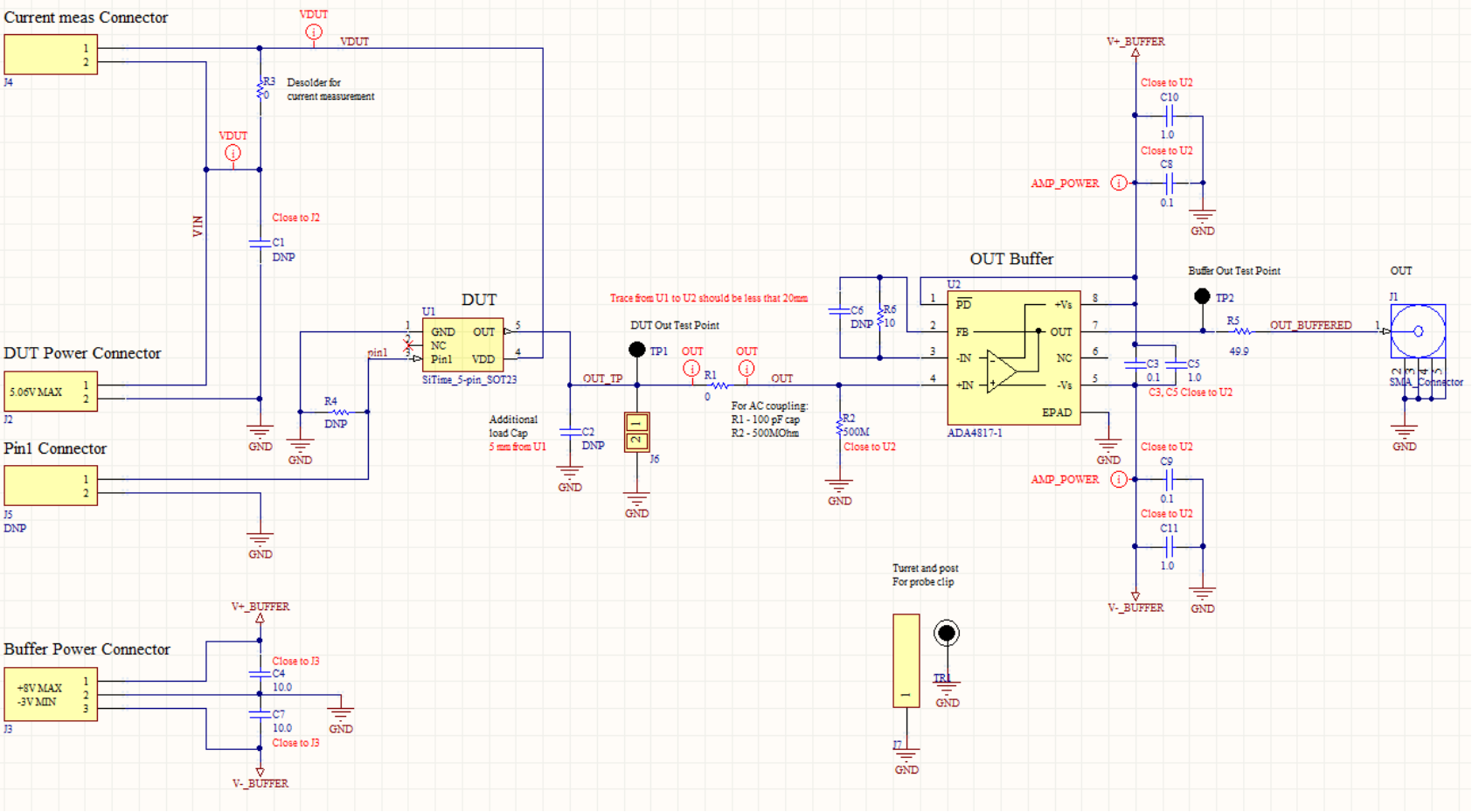

Figure A1: SiT6700EBB Electrical Schematics

Table A1: Bill of Materials (BOM)

#	Reference Designators	Description	Qty	SMD component size	Value
1	C1, C2	Capacitors	2	0805	DNP
2	C3, C8, C9	Capacitors	3	0402	0.1uF
3	C4, C7	Capacitors	2	0805	10.0uF
4	C5, C10, C11	Capacitor	3	0603	1.0uF
5	C6	Capacitor	1	0402	DNP
6	J1	SMA connector	1	-	-
7	J2, J4	2-pin header	2	-	-
8	J3	3-pin headers	1	-	-
9	J5	2-pin header	1	-	-
10	J6	2-pin header	1	-	-
11	J7	1-pin header	2	-	-
12	R1, R3	Resistors	2	0805	0
13	R2	Resistors	1	0805	500M
14	R5	Resistors	1	0402	49.9
15	R4	Resistors	1	0402	DNP
16	R6	Resistors	1	0402	10
17	TR1	TERM TURRET	1	-	-
18	U1	SiTime SE oscillator	1	-	-
19	U2	Buffer	1	-	-

Table A2: Connectors Digi-Key Part Number

Connectors	Digi-Key part number	Digi-Key part number for mating connector	Digi-Key part number for associated products
Current measurement	WM2744-ND	0022013027	WM2312-ND
Power Supply	WM2744-ND	0022013027	WM2312-ND
Buffer power	A30787-ND	WM2626-ND	WM2312-ND
Output	2057-2PH1-02-UA-ND	H2011-ND	H9999-ND

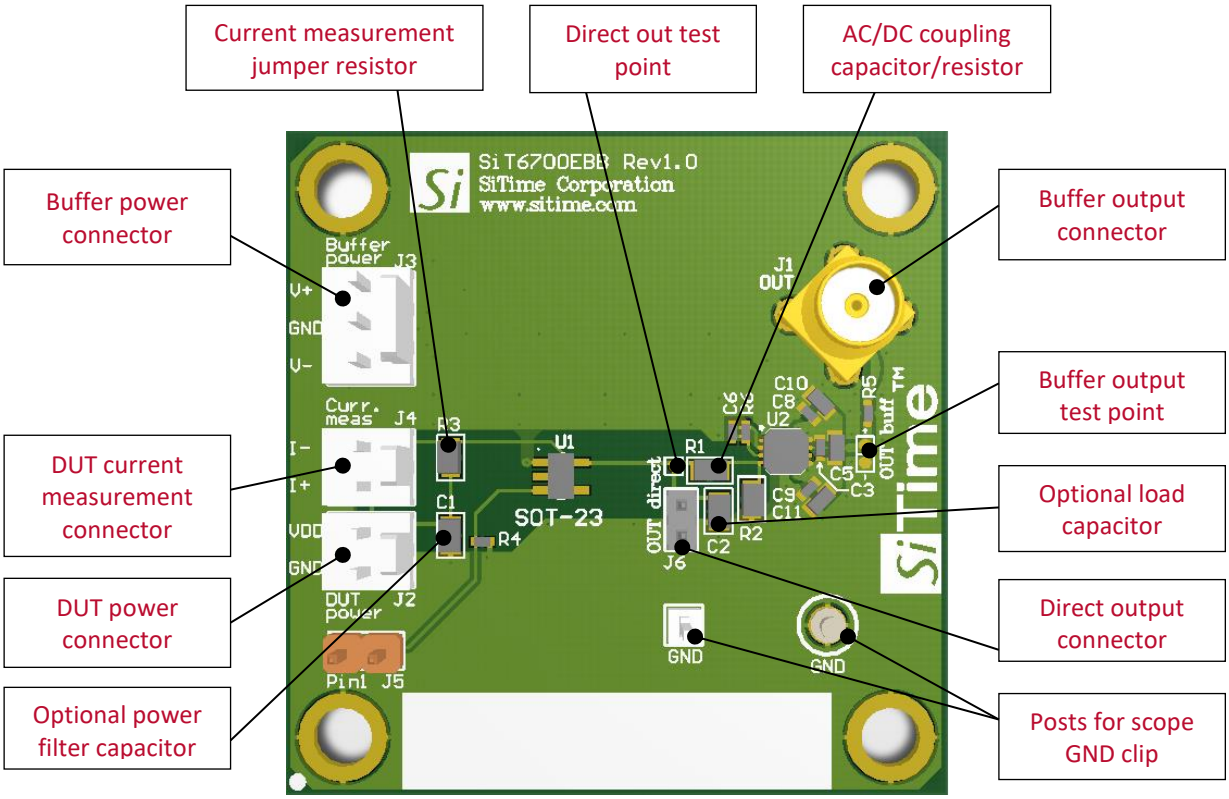

Figure A2: SiT6700EBB layout

Table 2: Revision History

Version	Release Date	Change Summary
1.0	14-Sep-2020	Original doc
1.1	8-Dec-2023	New document revision
1.2	5-Jan-2024	Changed buffer voltage

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