SiT6097EB Evaluation Board User Manual

Contents

1 Introduction

The SiT6097EB evaluation board (EVB) is designed for use with SiTime's XO in the 6-pin, 3.2 x 2.5 mm packages and LVPECL, LVDS or HCSL output type.

The SiT6097EB supports the following products:

Base Part Number	Type	Output frequency	Package
SiT9120	XO-DE	25 MHz to 212.5 MHz	3.2 x 2.5 QFN
SiT9121	XO-DE	1 MHz – 220 MHz	3.2 x 2.5 QFN
SiT9122	XO-DE	220 MHz – 625 MHz	3.2 x 2.5 QFN
SiT9365	XO-DE	25 MHz to 325 MHz	3.2 x 2.5 QFN
SiT9366	XO-DE	1 MHz – 220 MHz	3.2 x 2.5 QFN
SiT9367	XO-DE	220 MHz – 725 MHz	3.2 x 2.5 QFN
SiT9386	Automotive XO-DE	1 MHz – 220 MHz	3.2 x 2.5 QFN
SiT9387	Automotive XO-DE	220 MHz – 725 MHz	3.2 x 2.5 QFN
SiT3372	VCXO-DE	1 MHz – 220 MHz	3.2 x 2.5 QFN
SiT3373	VCXO-DE	220 MHz – 725 MHz	3.2 x 2.5 QFN
SiT3921	DCXO-DE	1 MHz – 220 MHz	3.2 x 2.5 QFN
SiT3922	DCXO-DE	220 MHz – 625 MHz	3.2 x 2.5 QFN
SiT3342	Endura VCXO-DE	1 MHz – 220 MHz	3.2 x 2.5 QFN
SiT3343	Endura VCXO-DE	220 MHz – 725 MHz	3.2 x 2.5 QFN
SiT9346	Endura XO-DE	1 MHz – 220 MHz	3.2 x 2.5 QFN
SiT9347	Endura XO-DE	220 MHz – 725 MHz	3.2 x 2.5 QFN
SiT5021	VCTCXO-DE	1 MHz – 220 MHz	3.2 x 2.5 QFN
SiT5022	VCTCXO-DE	220 MHz – 625 MHz	3.2 x 2.5 QFN

EVB Features

- Support for all device configuration modes: XO, TCXO
- SMA output for direct connection to measurement equipment
- Probing points for accurate waveform measurement
- The PCB is laid out with component loading options to different output termination schemes.

SiTime typically ships the EVB with the XO/SSXO/TCXO mounted using SiTime recommended reflow profile. The device should only be evaluated in its original soldered down state for best signal integrity and frequency stability. The device performance is not guaranteed if it is de-soldered and then re-soldered either manually or via reflow process.

2 I/O Descriptions

Table 1. SiT6097EB I/O

Connector designator	I/O	Description
P1	**Power Supply**	Three-pin connector for DC power supply and power sensing. **VDD is connected to Pin 1, GND – to Pin2 of P1.** **VDD sense is connected to Pin 3, GND – to Pin2 of P1.**
P2	**Pin 1 access**	A Three-pin header (P2) provides access to the pin 1 of the XO in OE mode, Standby (ST), Spread Disable (SD), Voltage Control (VC) or Digital Control (DC) functionality. In OE/ST mode, pin 1 can be left floating as there is an internal pull-up resistor.
P3	**Pin 2 access**	A Three-pin header (P3) provides access to the pin 2
P4	**Current measurement**	Two-pin connector for current measurement.
P5	**VBIAS**	Three-pin connector for supplying bias voltage or supplying negative voltage to DUT ground pin for split ground configuration. See Section 3.1 for detailed information on different termination schemes. **VBIAS is connected to Pin 1, GND – to Pin2 of P5.** **VBIAS sense is connected to Pin 3, GND – to Pin2 of P5.**
J1 and J2	**OUT+ and OUT-**	Oscillator output (Out+ and Out-) can be accessed either using active probe or SMA connector. The test points for active probe are placed closely to the oscillator output for better signal integrity (see Figure A2). Section 3.2 describes in details the recommended measurement configurations.

3 EVB Usage Descriptions

3.1 EVB Configurations

SiT6097EB can be configured to support three configuration modes including XO/TCXO with output enable (OE), XO in Standby (ST), Spread Disabled (SD), Voltage Control (VC) or Digital Control (DC). The test points for active probe are placed closely to the oscillator output for better signal integrity (see Figure A2 and sections 3.1.1, 3.1.3, 3.1.5, 3.1.7).

On the schematic, components used in all configurations described in the following sections have their nominal values assigned. Figure A1 in Appendix A shows the complete electrical schematic of SiT6097EB.

Components labeled “DNP” are not assembled. Any components which nominal are not shown on the schematic will be not populated by default unless it is defined by the specific configuration.

3.1.1 LVPECL, Standard Termination, Active Probe

In this configuration, the LVPECL outputs are terminated to Vbias = VDD – 2 V with 50 Ω resistors (R11 and R24). A high-speed active probe, as shown on Figure 1, is placed on the termination resistor’s pads which are on the OUT+ and OUT- traces. Figure 1 shows the termination scheme for this configuration.

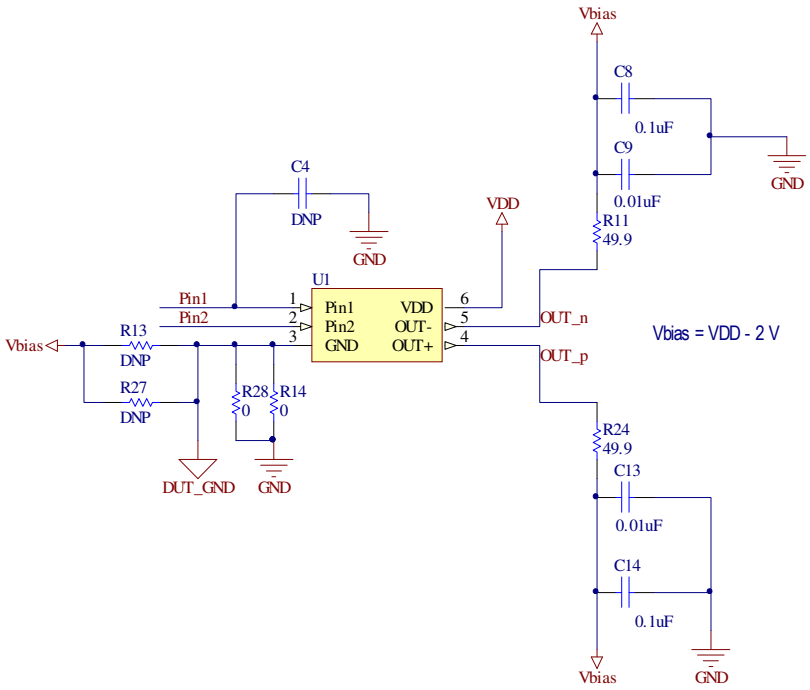

Figure 1. LVPECL output termination with 50 Ω to Vbias and measurement using high impedance and high bandwidth active probe.

3.1.2 LVPECL, AC-coupling Configuration, Direct to Instrument

This is default shipment configuration for evaluation boards with LVPECL devices.

This configuration allows LVPECL output connection to the measurement instrument using 50 Ω coaxial cables. Outputs are terminated with 100 Ω/48.7 Ω (R12 and R25; for 3.3 V and 2.5 V VDD respectively) to GND on the DUT side and connected to SMA connectors through 0.1 uF series capacitors (R16 and R23). Figure 2 shows the termination scheme for this configuration.

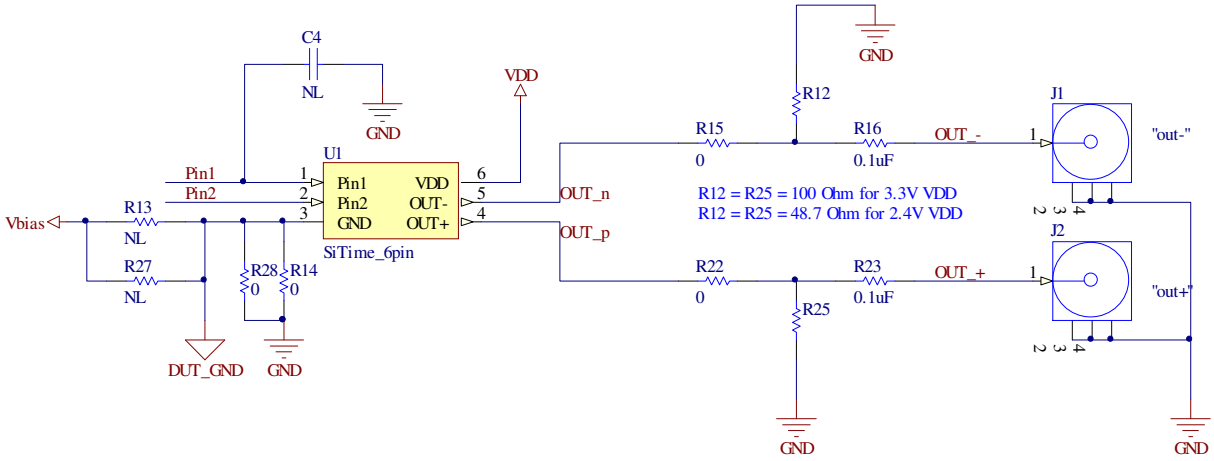

Figure 2. LVPECL output termination with 100 Ω/48.7 Ω to GND and measurement with AC-coupled connection to measurement instrument using 50 Ω SMA cables.

3.1.3 LVPECL, Y-Termination, Active Probe

This configuration is intended for LVPECL output waveform parameters measurement using active probe. Figure 3 shows termination scheme for this configuration. R26 is added to create DC voltage bias for OUT+ and OUT- with R24 (50 Ω) and R11 (50 Ω). R26 is 50 Ω for 3.3 V VDD and 18 Ω for 2.5 V VDD.

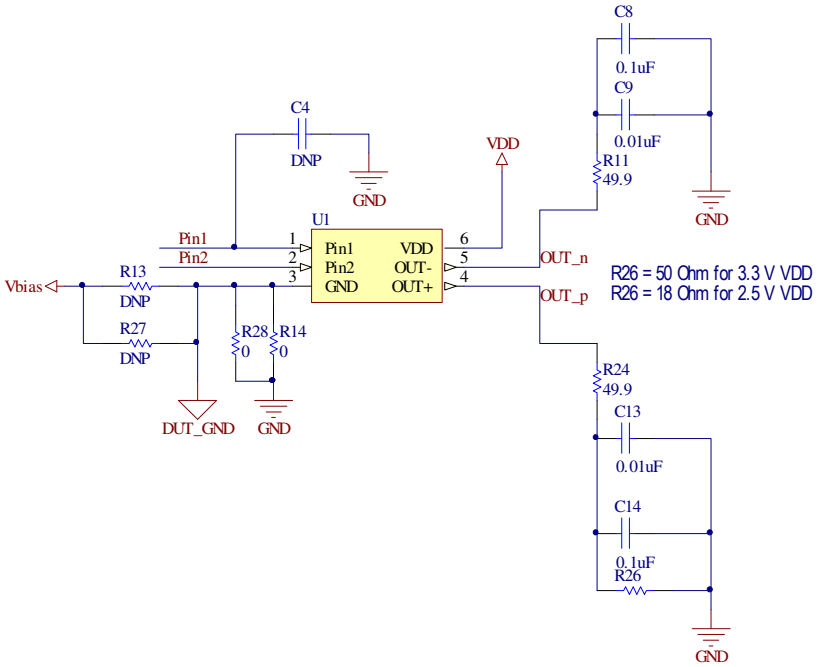

Figure 3. Y-termination scheme for LVPECL output termination for measurement using high impedance and high bandwidth active probe.

3.1.4 LVPECL, Split Ground, Direct to Instrument

By splitting the power supply with VDD set to 2 V referenced to ground and Vbias set to -1.3 V (for 3.3 V across DUT) or -0.5 V (for 2.5 V across DUT) referenced to ground, the OUT+ and OUT- are effectively biased at ground potential. Thus OUT+ and OUT- can be connected to the measurement instrument 50 Ω inputs through DC-coupling and SMA cables. Figure 4 shows termination scheme for this configuration.

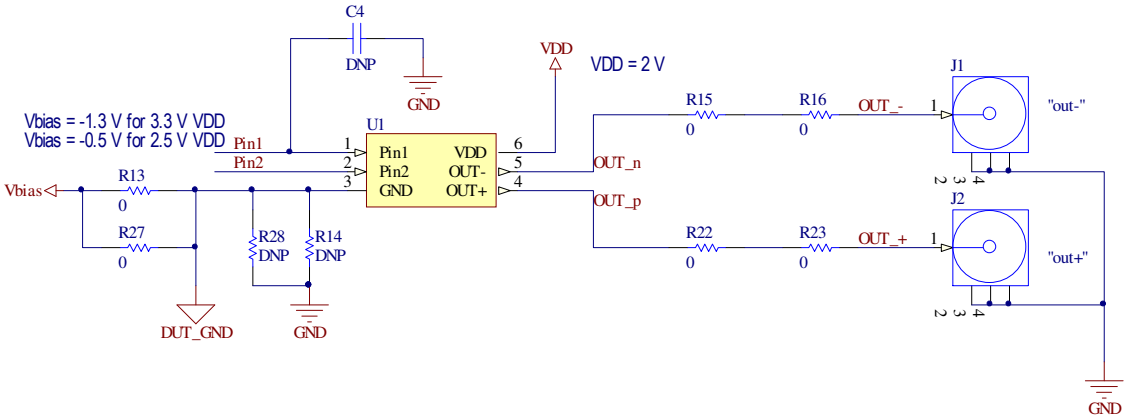

Figure 4. Termination scheme with 2 V VDD and -1.3V/-0.5V VSS and DC-coupled LVPECL outputs to 50 Ω measurement instrument inputs.

3.1.5 LVDS, Standard Termination, Active Probe

This configuration is intended for LVDS output waveform parameters measurement using active probe. A high-speed active probe, as shown on Figure 5, is placed on the termination resistor's pads which are on the OUT+ and OUT- traces. Figure 5 shows differential impedance of 100 Ω (R21) across OUT+ and OUT- for termination.

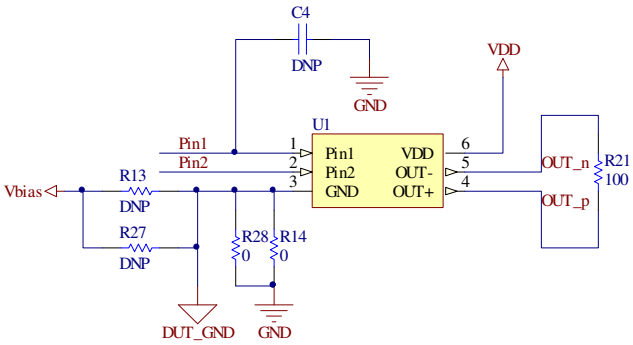

Figure 5. 100 Ω differential impedance across LVDS outputs for measurement using high impedance and high bandwidth active probe.

3.1.6 LVDS, AC-coupling Configuration, Direct to Instrument

This is default shipment configuration for evaluation boards with LVDS devices.

This configuration is useful for connecting LVDS outputs to 50 Ω input channels of the measurement instrument. The AC-coupling capacitors (R16 and R23) block the DC common mode voltage from the LVDS outputs to avoid DC current draw to the 50 Ω inputs. Figure 6 shows termination scheme for this configuration.

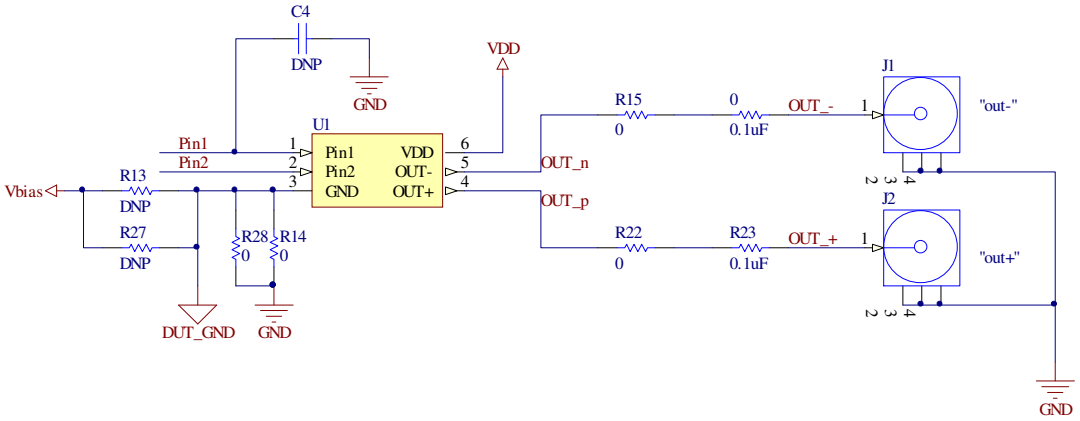

Figure 6. AC-coupled LVDS outputs are terminated by measurement instrument input 50 Ω impedance, equivalent 100 Ω across OUT+ and OUT-.

3.1.7 HCSL, Standard Termination, Active Probe

This configuration is intended for HCSL output waveform parameters measurement using active probe. Output is terminated with 50 Ω (R12 and R25) to GND. Series resistors R15 and R22 are used as overshoot limiter and should be in range from 10 Ω to 30 Ω. A high-speed active probe is placed on the termination resistor's pads which are on the OUT+ and OUT- traces. Figure 7 shows termination scheme for this configuration.

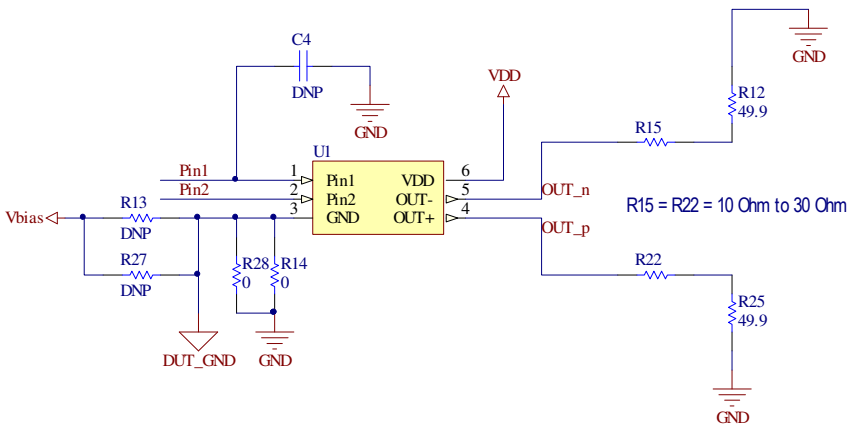

Figure 7. HCSL outputs terminated with 50 Ω to GND through 10 Ω to 30 Ω series resistors for measurement using high impedance and high bandwidth active probe.

3.1.8 HCSL, Standard Termination, Direct to Instrument

This is default shipment configuration for evaluation boards with HCSL devices.

This configuration is intended for HCSL output waveform parameters measurement with direct connection to measurement instrument 50 Ω inputs. Figure 8 shows termination scheme for this configuration. Series resistors R15 and R22 are used as overshoot limiter and should be in range of 10 Ω to 30 Ω.

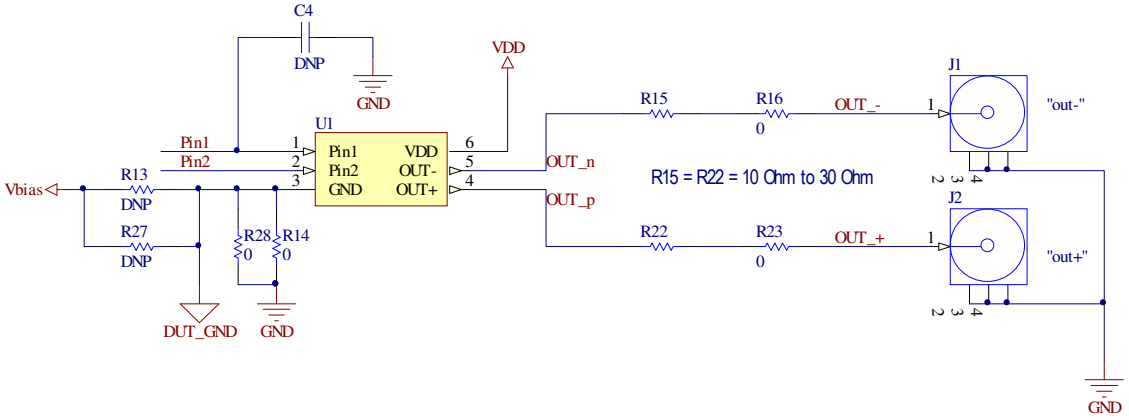

Figure 8. HCSL outputs terminated with 50 Ω to GND at measurement instrument side with 10 Ω to 30 Ω series resistors at source side.

3.2 Waveform Capturing Using Active Probe

SiTime XO/TCXO is a high-speed logic output device. It is critical that the proper logic and high frequency measurement techniques are used along with the high-quality active probe to ensure best measurement results.

SiTime recommends the following minimum equipment for proper clock waveform measurement.

1) 4 GHz or higher active probe with capacitance <1 pF, such as a Keysight 1134B;
2) Oscilloscope with 4 GHz bandwidth or higher such as a Keysight DSA90604A.

A passive voltage probe should not be used as it adds a high capacitive load to the part and the long ground lead clip is not suitable for high frequency measurement applications. The inductance of the long ground lead coupled with the input capacitance of the probe results in a resonant circuit. The consequence of this resonance results in the distortion of the clock signal. Typical manifestations of this distortion include ringing, overshoot, and undershoot of the clock signal.

Please refer to Figure A2 for test point locations on the SiT6097EB. Please refer to Figure 9 for probing example on the EVB using active probe.

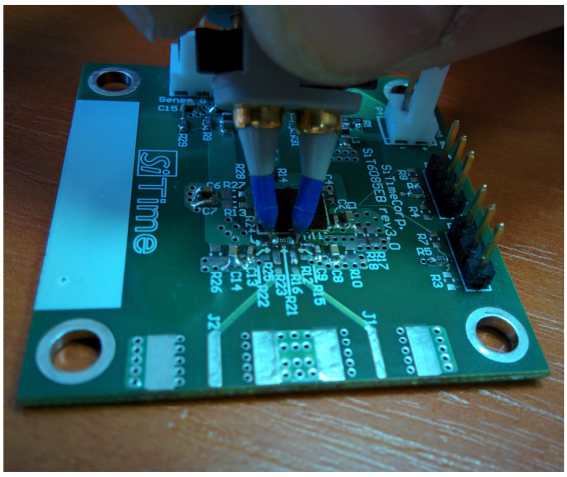

Figure 9. Differential browser (high impedance active probe) on test points for waveform capture on SiT6097EB.

More details on the SiTime recommendations on the oscillator's output probing can be found in AN10028.

3.3 Measuring Jitter and Phase Noise

For Jitter measurements or phase noise measurements with evaluation boards, SiTime recommends using SMA support Configuration to connect the device output directly to external equipment, such as Time Interval Analyzer (TIA) or high-bandwidth real-time oscilloscope. Jitter measurement technique is described in SiTime AN10007.

The SMA can also be connected through 50 Ω coaxial cable to signal source analyzers or spectrum analyzers to measure phase noise. In such case the use of AC-coupling configuration is recommended because not all measurement instruments can accept DC voltage at their inputs.

3.4 Current Measurement

To measure the current consumption, user need to use ammeter/multi-meter in the power supply circuit. To measure the current, remove zero-ohm resistors R1 and R19. It is recommended to measure the voltage on DUT VDD and adjust for any drop on the DMM to ensure known VDD voltage on the device. VDD adjustment must be completed before every current measurement.

Appendix A

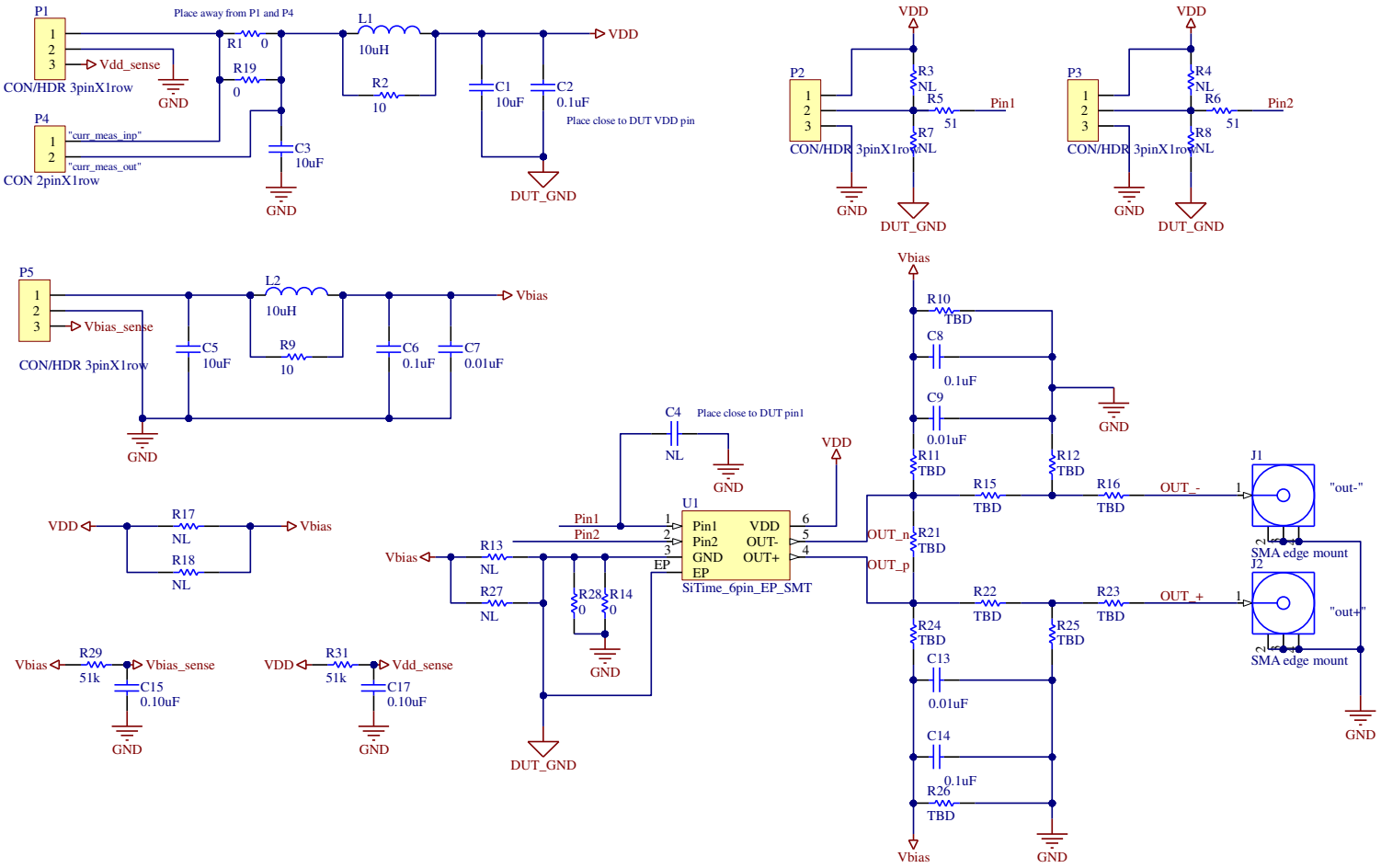

Figure A1: SiT6097EB electrical schematics

Table A1: Bill of Materials (BOM)

#	Reference Designators	Description	Qty	SMD component size	Value
1	R1, R14, R19, R28	Resistor	4	0603	0 Ω
2	R2, R9,	Resistor	2	0603	10 Ω
3	R5, R6	Resistor	2	0603	51 Ω
4	R29, R31	Resistor	2	0603	51 kΩ
5	R3, R4, R7, R8, R13, R17, R18, R27	Resistor	8	0603	DNP
6	R10, R21, R26	Resistor	3	0603	See Figure 1~8 for values
7	R11, R12, R15, R16, R22, R23, R24, R25	Resistor	8	0402	See Figure 1~8 for values
8	L1, L2,	Inductor	2	0805	10 uH
9	C1, C3, C5	Ceramic capacitor	3	0603	10 uF
10	C2	Ceramic capacitor	1	0402	0.1 uF
11	C6, C8, C14, C15, C17	Ceramic capacitor	5	0603	0.1 uF
12	C7, C9, C13	Ceramic capacitor	4	0402	0.01 uF
13	C4	Ceramic capacitor	1	0603	DNP
14	U1	SiTime Oscillator	1	-	-
15	P1, P5	3-pin connector	2	-	-
16	P2, P3	3-pin header	2	-	-
17	P4	2-pin connector	1	-	-
18	J1, J2	SMA connectors	2		

Table A2: Connectors Digi-Key Part Number

Connectors	Digi-Key part number	Digi-Key part number for mating connector	Digi-Key part number for associated products
Power Supply	**WM2701-ND**	**WM2001-ND**	**WM1114TR-ND**
Pin 1 access	**609-3461-ND**	**76341-303LF-ND**	
Pin 2 access	**609-3461-ND**	**76341-303LF-ND**	
Current measurement	**WM2744-ND**	**WM2011-ND**	**WM1114-ND**
VBIAS	**WM2701-ND**	**WM2001-ND**	**WM1114TR-ND**
OUT+ and OUT-	**WM5534-ND**		

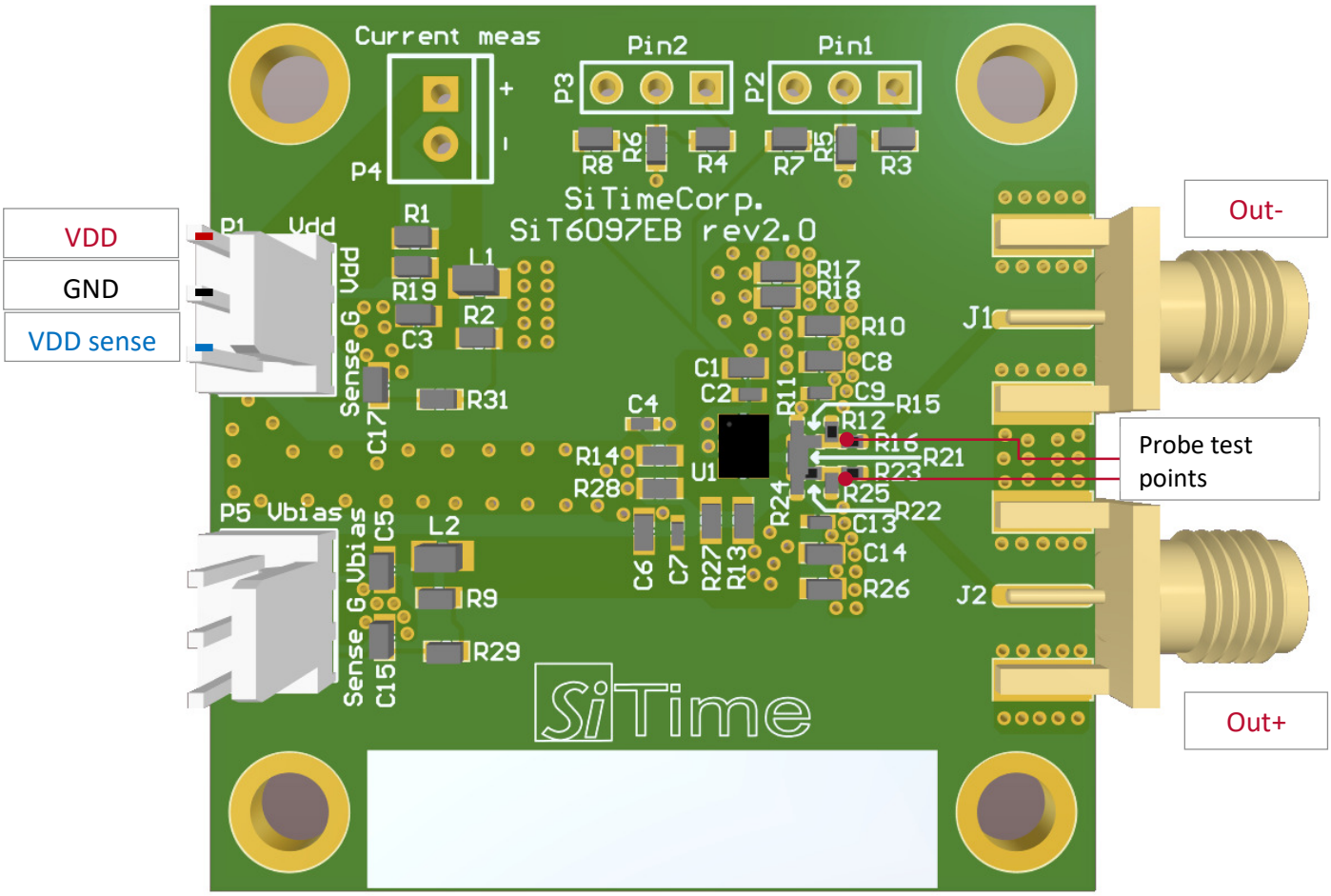

Figure A2: SiT6097EB layout

Table 2: Revision History

Version	Release Date	Change Summary
1.0	14-Sep-2023	Original doc
2.0	15-Dec-2023	New document revision

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