SiT6092EB Evaluation Board User Manual

Contents

1 Introduction

The SiT6092EB evaluation board (EVB) is designed for use with SiTime's VCXO in the 6-pin 7.0 x 5.0 mm packages and LVCMOS output type.

The SiT6092EB supports the following products:

Base Part Number	Type	Output frequency	Package
SiT3807	VCXO	1.544 MHz - 49.152 MHz	7.0 x 5.0 mm
SiT3808	VCXO	1 MHz – 80 MHz	7.0 x 5.0 mm
SiT3809	VCXO	80 MHz – 220 MHz	7.0 x 5.0 mm
SiT3907	DCXO	1 MHz – 220 MHz	7.0 x 5.0 mm

EVB Features

- Support for all device configuration modes: VCXO, DCXO
- SMA output for direct connection to measurement equipment
- Probing points for accurate waveform measurement

SiTime typically ships the EVB with the VCXO/DCXO mounted using SiTime recommended reflow profile. The device should only be evaluated in its original soldered down state for best signal integrity and frequency stability. The device performance is not guaranteed if it is de-soldered and then re-soldered either manually or via reflow process.

2 I/O Descriptions

Table 1. SiT6092EB I/O

Connector designator	I/O	Description
P2	**Power Supply**	A two-pin header for DC power supply.
P5	**Pin 1 access**	A three-pin header provides access to the pin 1 of the XO in Voltage Control (VC) or Digital Control (DC) functionality.
P1	**Pin 2 access**	A three-pin header provides access to the pin 2 of the XO in OE mode, Standby (ST). In OE/ST mode, a pull-up resistor of 10 kΩ or less is recommended if pin 2 is not externally driven. If pin 2 needs to be left floating, use the NC option.
P3	**Pin 5 access**	A three-pin header provides access to the pin 5. No effect on output frequency or other device functions.
P6	**Tri-State Buffer Control**	A three-pin header provides access to on-board tri-state buffer IC. This IC can be used to create a one-wire tri-level return-to-middle waveform which, for example, is required for sending digital data to the DCXO device. Two external digital inputs are required to drive output enable and data input pins of the buffer.
J1	**Output**	Oscillator output can be accessed either using active probe or SMA connector. The test points for active probe are placed closely to the oscillator output for better signal integrity (see Figure A2). Section 3.2 describes in details the recommended measurement configurations.
P4	**Current Measurement**	A two-pin header enables measuring the current consumption of the device.

3 EVB Usage Descriptions

3.1 EVB Configurations

SiT6092EB can be configured to support two configuration modes including XO with output enable (OE), XO in Standby (ST), Voltage Control (VC) or Digital Control (DC).

Oscillator output can be accessed in several ways listed in Table 2. Table 2 describes components configuration to support all output configurations.

Table 2. Components configuration to support all output configurations.

Output configuration	R18	C6	R13	R19
Direct	DNP	DNP*	0.1 uF/ 0 Ω	DNP*
Probe	DNP	DNP*	DNP	DNP*

* The value of the load capacitor C6 and load resistor R19 can be adjusted to match the load conditions in the target application. This enables the user to measure waveform characteristics under similar conditions as close to those on the target board as possible.
The test points for active probe are placed closely to the oscillator output for better signal integrity (see Figure A2).

Figure A1 in Appendix A shows the complete electrical schematic of SiT6092EB. Components labeled "DNP" are not assembled.

Shipment Configuration
SiT6092EB is shipped configured for direct output allowing connecting it to the instrument input using 50 Ω coax cable. Details on the board assembly for shipment configuration can be found on the schematic (see Figure A1 in Appendix A).

VCXO Configuration
Two pin connector P5 is provided for connecting input control voltage to oscillator pin 1 (Vin). Because Pin 1 (Vin) is an analog input and is sensitive to external noise (for example, noise of the instrument that sets the voltage on Pin 1) the RC low-pass filter with 16kHz cutoff frequency is recommended on the board to reduce the external noise impact on the oscillator output performance. Recommended low-pass RC filter implementation: use 62Ω for R14, 0Ω for R12; use 1uF capacitor instead R15 and don't load R11.
Warning! Pin1 (Vin) of VCXO should not be left floating during evaluation. Doing so makes input sensitive to the noise which will get coupled to the pin. This mechanism will impact the output performance.

DCXO Configuration
In DCXO Configuration all components labeled "DNP" are not loaded, schematic part outlined by dashed line is assembled and 0-ohm resistor R15 is loaded instead of resistor R14 (see Figure A1 in Appendix A).

Tri-state buffer IC U1 SN74LVC1G126DBVR can be used to create a one-wire tri-level return-to-middle signaling type compatible with DCXO devices. Two external digital inputs are required to drive output enable and data input pins of the IC. See SiT3907 datasheet for DCXO interfacing details https://www.sitime.com/support/resource-library/datasheets/sit3907-datasheet).

3.2 Waveform Capturing Using Active Probe

SiTime XO is a high-speed logic output device. It is critical that the proper logic and high frequency measurement techniques are used along with the high-quality active probe to ensure best measurement results.

SiTime recommends the following minimum equipment for proper clock waveform measurement.

1) 4 GHz or higher active probe with capacitance <1 pF, such as a Keysight 1134B;
2) Oscilloscope with 4 GHz bandwidth or higher such as a Keysight DSA90604A.

A passive voltage probe should not be used as it adds a high capacitive load to the part and the long ground lead clip is not suitable for high frequency measurement applications. The inductance of the long ground lead coupled with the input capacitance of the probe results in a resonant circuit. The consequence of this resonance results in the distortion of the clock signal. Typical manifestations of this distortion include ringing, overshoot, and undershoot of the clock signal.

Eliminating such distortion requires a probe with the lowest input capacitance and a low inductance ground lead. In addition, SiTime TCXOs are typically configured for fast rise and fall times with 15 pF load. It is therefore critical that the probe tip ground be as short as possible, lowest inductance, and the return path for the ground be located as close as possible to the trace carrying the RF logic signal.

For waveform measurement, it's recommended to remove resistor R13. Please refer to Figure A2 for (Figure 1).

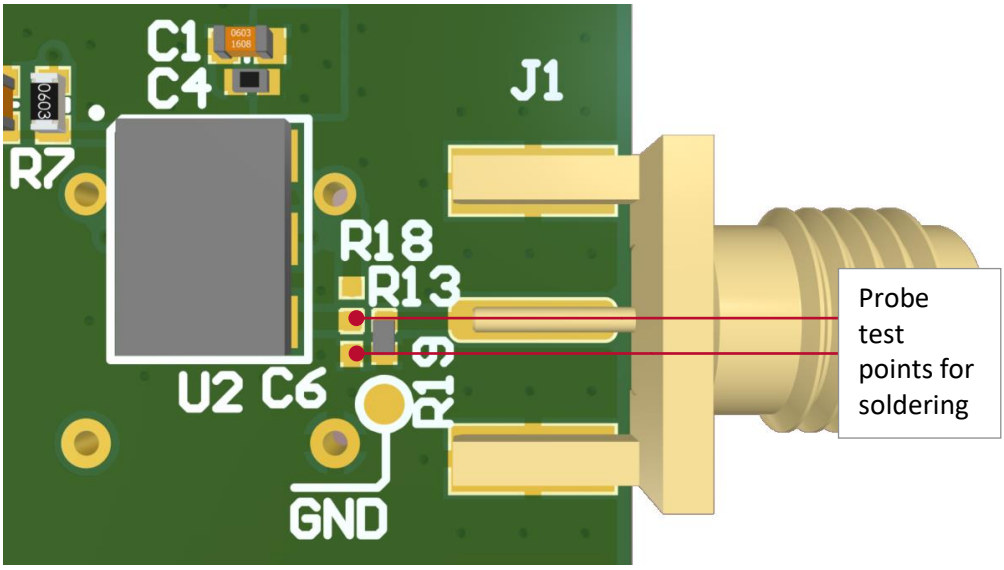

Figure 1: Recommended points for soldering probe head

More details on the SiTime recommendations on the oscillator's output probing can be found in AN10028.

3.3 Measuring Jitter and Phase Noise

For Jitter measurements or phase noise measurements with evaluation boards, SiTime recommends using SMA support Configuration to connect the device output directly to external equipment, such as Time Interval Analyzer (TIA) or high-bandwidth real-time oscilloscope. Jitter measurement technique is described in SiTime AN10007.

The SMA can also be connected through 50 Ω coaxial cable to signal source analyzers or spectrum analyzers to measure phase noise. In such case the use of AC-coupling configuration is recommended because not all measurement instruments can accept DC voltage at their inputs.

3.4 Current Measurement

To measure the current consumption, user need to use ammeter/multi-meter in the power supply circuit. Simply remove jumper resistor R6 across 2-pin connector P4. It is recommended to measure the voltage on DUT VDD and adjust for any drop on the DMM to ensure known VDD voltage on the device. VDD adjustment must be completed before every current measurement.

Appendix A

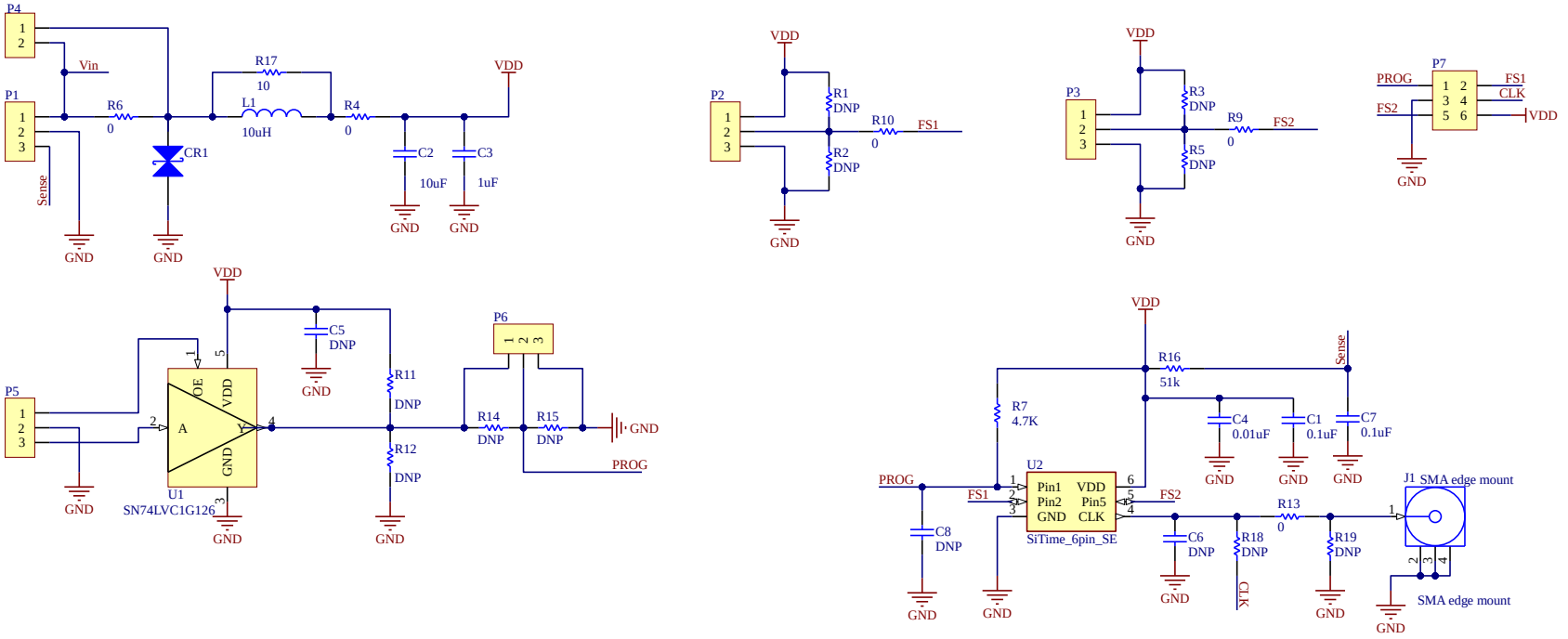

Figure A1: SiT6092EB electrical schematics

Table A1: Bill of Materials (BOM)

#	Reference Designators	Description	Qty	SMD component size	Value
1	C1, C7	Capacitors	2	0603	0.1uF
2	C2	Capacitors	1	0603	10uF
3	C3	Capacitors	1	0603	1uF
4	C4	Capacitor	1	0402	0.01uF
5	C5, C8	Capacitor	2	0603	DNP
6	C6	Capacitor	1	0402	DNP
7	CR1	ESD bidirectional protection diode	1	0603	DNP
8	J1	SMA connector	1	-	-
9	L1	Inductance	1	0805	10 uH
10	R1, R2, R3, R5, R11, R12, R14	Resistor	7	0603	DNP
11	R4, R6, R9, R10	Resistors	4	0603	0
12	R7	Resistors	1	0603	4.7K
13	R13, R19	Resistors	2	0402	DNP
14	R15	Resistor	1	0603	DNP
15	R16	Resistor	1	0603	51k
16	R17	Resistor	1	0603	10
17	R18	Resistor	1	0402	0
18	P4	2-pin header	1	-	-
19	P1, P2, P3, P5, P6	3-pin headers	5	-	-
20	P7	3-pin headers, Dual row		-	DNP
21	U1	SN74LVC1G126	1	-	-
22	U2	SiTime SE oscillator	1	-	-

Table A2: Connectors Digi-Key Part Number

Connectors	Digi-Key part number	Digi-Key part number for mating connector	Digi-Key part number for associated products
Power	A30787-ND	WM2011-ND	WM1114TR-ND
Pin 1	S1012E-03-ND	S7036-ND	-
Pin 2	S1012E-03-ND	S7036-ND	-
Pin 5	S1012E-03-ND	S7036-ND	-
Tri-State Buffer Control	A30787-ND	WM2011-ND	WM1114TR-ND
Current Measurement	WM2744-ND	WM2011-ND	-

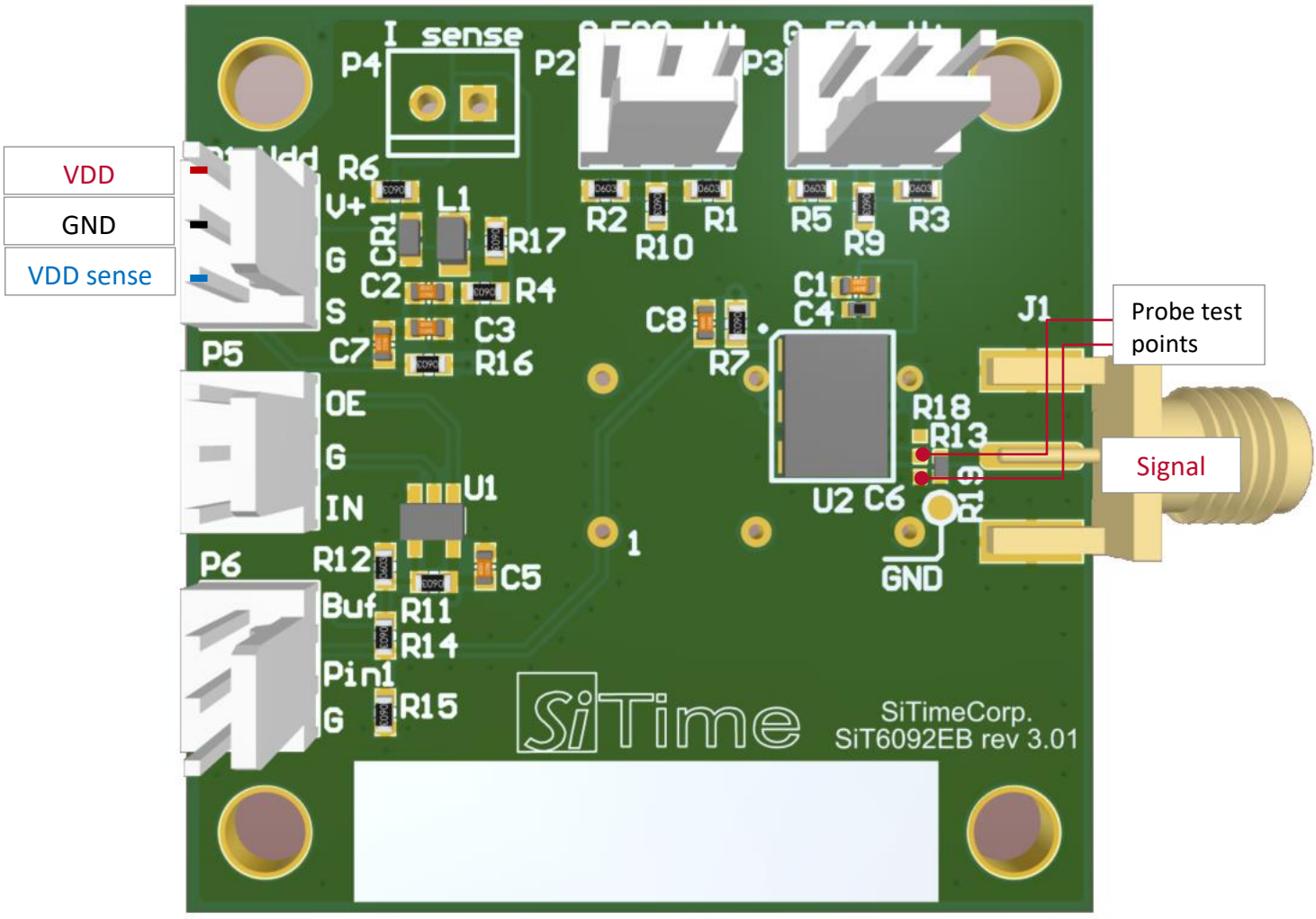

Figure A2: SiT6092EB layout

Table 3: Revision History

Version	Release Date	Change Summary
1.0	22-Jun-2012	Original doc
3.01	12-Dec-2023	New document revision

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