Clocking Texas Instruments FPD-Link

Precision Timing Solutions

1. Introduction

FPD-Link is a serializer-deserializer (SerDes) interface developed by Texas Instruments and is now commonly used for infotainment and ADAS applications. FPD-Link transmits high-definition video from cameras to ADAS computers, as well as from Infotainment systems to LCD displays. It features advanced techniques to enable long cables in harsh EMI environments.

FPD-Link was introduced in 1996 and went through several generations, the most recent one being FPD-Link IV. Starting with FPD-Link II (2006), the interface was specifically designed for automotive infotainment and camera interface applications. FPD-Link III (2010) added a bidirectional communication channel on the same differential pair. This backchannel enables GPIO and I2C communication, as well as uplink clock transmission (see Synchronous clocking below.) FPD-Link IV (2022) represents the latest generation.

2. FPD-Link Clock Requirements

FPD-Link requires a single-ended LVCMOS clock (called "PCLK") between 25 MHz and 100 MHz, provided by an oscillator such as the SiT1625. Clock jitter must be well controlled. Excessive jitter on the clock "closes the eye diagram", resulting in increased bit error rate (BER) on the link. For more details on jitter and its influence on high-speed serial links, see the Timing Essentials learning hub resources [1] and [2].

There are two basic architectures to clock FPD-Link: asynchronous and synchronous. This document will explore both from a clocking perspective. Discussing the overall pros and cons of each architecture is out of the scope of this document. See the TI learning center [3] for information on this topic.

Key considerations for designers are:

- Reliability
- Jitter performance
- Electromagnetic interference (EMI) and electromagnetic compatibility (EMC) compliance
- Small footprint

3. Asynchronous FPD-Link Architecture

Asynchronous mode represents the traditional way of driving serial data interfaces: both clock + data are provided at the input of the serializer. After transmission, both clock and data are recovered at the deserializer. Because multiple, independent links each run with its own independent clock, this mode is called asynchronous.

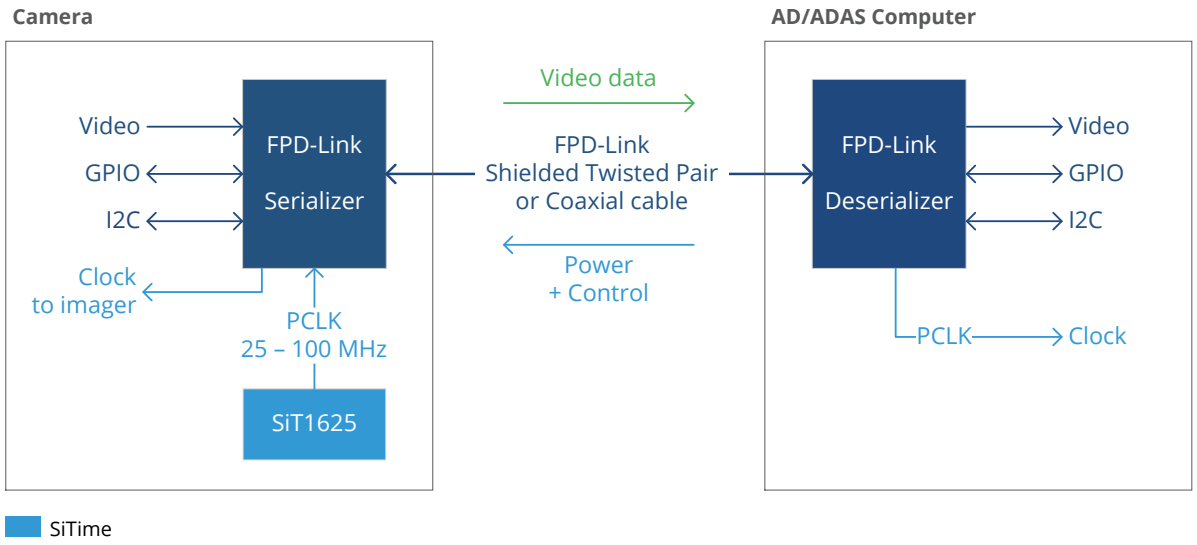

Figure 1: Asynchronous FPD-Link block diagram

FPD-Link serializers offer the possibility to output a clock to the imager, as shown on Figure 1. Another use case consists in driving the imager with an oscillator and using the imager clock as input to the serializer. This mode is explained in more details in the TI learning center [4]; however, this use case presents the disadvantage of higher jitter on the serializer PCLK input, therefore potentially increasing the BER on the link. SiTime recommends providing the PCLK directly from the oscillator to the serializer (as shown in Figure 1) whenever asynchronous mode is desired.

4. Synchronous FPD-Link Architecture

In synchronous mode, the clock is provided from an oscillator to the deserializer side of the FPD-Link. The clock is then transmitted "uplink" through the FPD-Link backchannel to the serializer. This mode is called synchronous because the link runs synchronously to the deserializer and multiple links are therefore synchronized. However, an extra step is required to synchronize multiple links: all deserializers clocks must have the same frequency and phase. This is best achieved with a clock generator (see section 5).

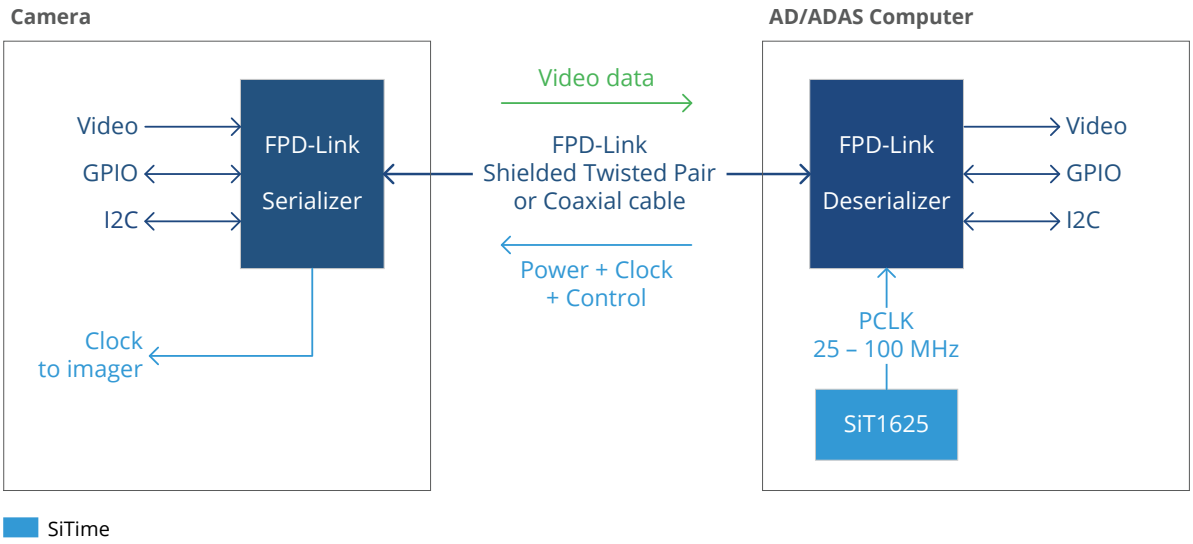

Figure 2: Synchronous FPD-Link block diagram

Per the TI learning center [4], the main advantages of synchronous mode vs. asynchronous are:

- **BOM cost reduction**: No oscillator is needed on the camera module. Instead, a clock source is required on the deserializer side. Is this a wash from a system-level perspective? Not necessarily. Because AD/ADAS computers require many clocks, there is great potential for improvements by consolidating multiple oscillators into one clock generator.
- **EMI reduction**: In asynchronous mode, multiple, independent FPD-Links are clocked with similar, but not exactly identical frequencies. This can create many low-frequency mixing spurs. Synchronous clocking solves this problem – here again with the prerequisite that all clocks come from a single source such as a clock generator.
- **Increased reliability**: Quoting the TI learning center [4], "*crystal oscillators are often one of the weak links in terms of reliability in a camera.*" This couldn't be truer. But why would a crystal oscillator on the deserializer side be more reliable than a crystal oscillator on the serializer side?

The answer to the reliability question is to replace crystal oscillators (or crystal-based clock generators) with something better. SiTime MEMS-based timing devices are up to 50x more reliable than crystal-based oscillators.

5. Synchronizing multiple FPD-Links with a SiTime clock generator

When multiple cameras (e.g., front left, front center, and front right of a vehicle) are synchronized, their frames are aligned. This reduces the need for a RAM buffer on the ADAS computer side, otherwise needed to re-align mismatched video frames.

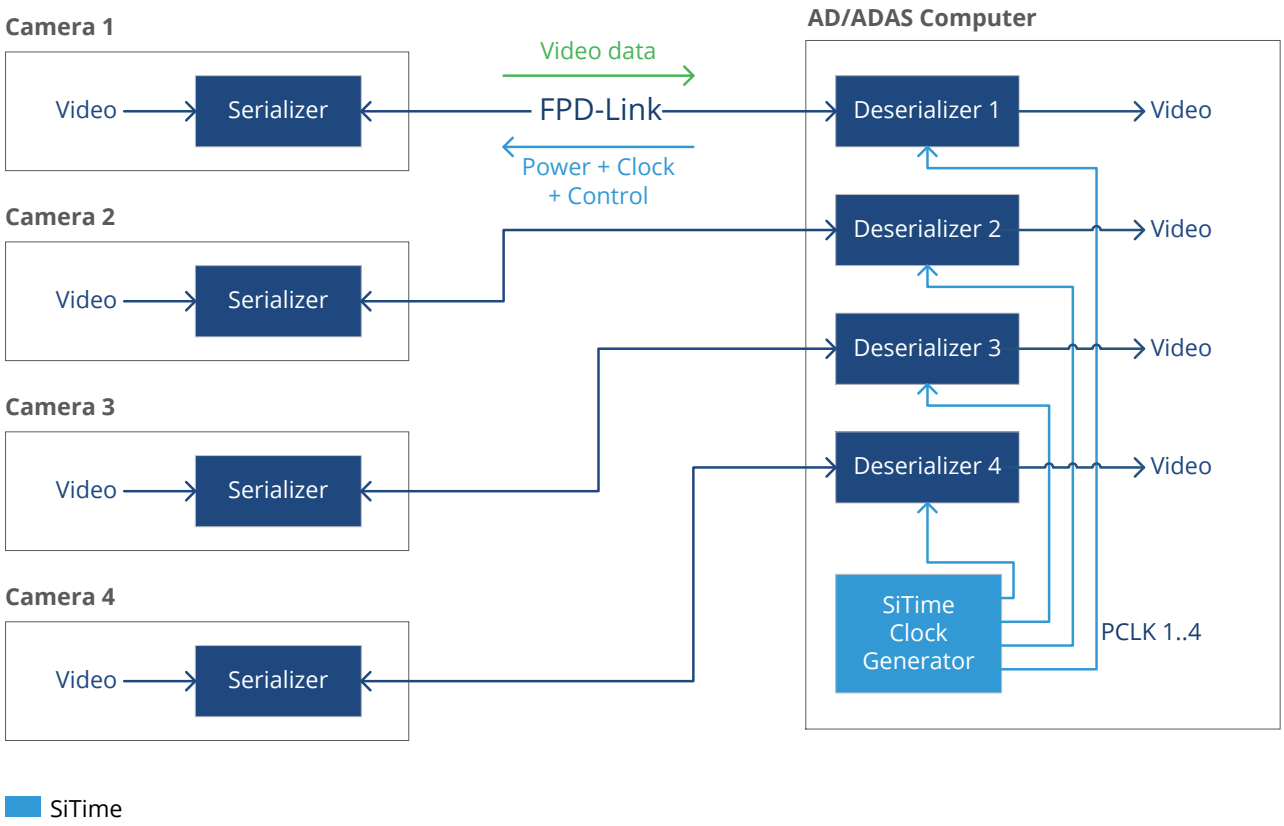

Figure 3: Multiple synchronous FPD-Links

Having all clocks at the same frequency and phase is a prerequisite for synchronizing multiple links. This is best achieved with a clock generator. SiTime automotive clock generators feature an integrated, high-reliability MEMS resonator. Multiple configurable output frequencies enable FPD-Links with different frequencies. The typical use case is multiple cameras having different resolutions. Advanced features for ADAS applications are available too. Please contact SiTime for information on the detailed feature set and product availability.

Clocking multiple FPD-Links with a clock from a single-output SiTime oscillator, distributed with a fanout buffer, is possible too and does not compromise reliability. However, running links at different frequencies is not possible in this case. Fanout buffers also increase jitter on clocks. SiTime recommends using clock generators whenever multiple clocks (identical or not) are needed.

6. EMI Reduction

As FPD-Link is intended to operate in electromagnetic interference (EMI) prone environments, care must be taken to ensure best EMI/EMC compliance. Apart from the usual best practices of circuit and PCB design, EMI can be reduced by using an oscillator with adjustable drive strength via configurable rise/fall times of the clock.

Devices such as the SiT1625 include a programmable drive strength feature. Slowing down rise/fall times reduces harmonic power up to -24.4 dB (Figure 4). Note that slowing edge rates too much can increase jitter, which can be detrimental to BER on the link. Jitter must remain within specified limits.

Odd Harmonic Power Comparison for SiTime LVCMOS Oscillators with FlexEdge™ Outputs, VDD = 3.3 V

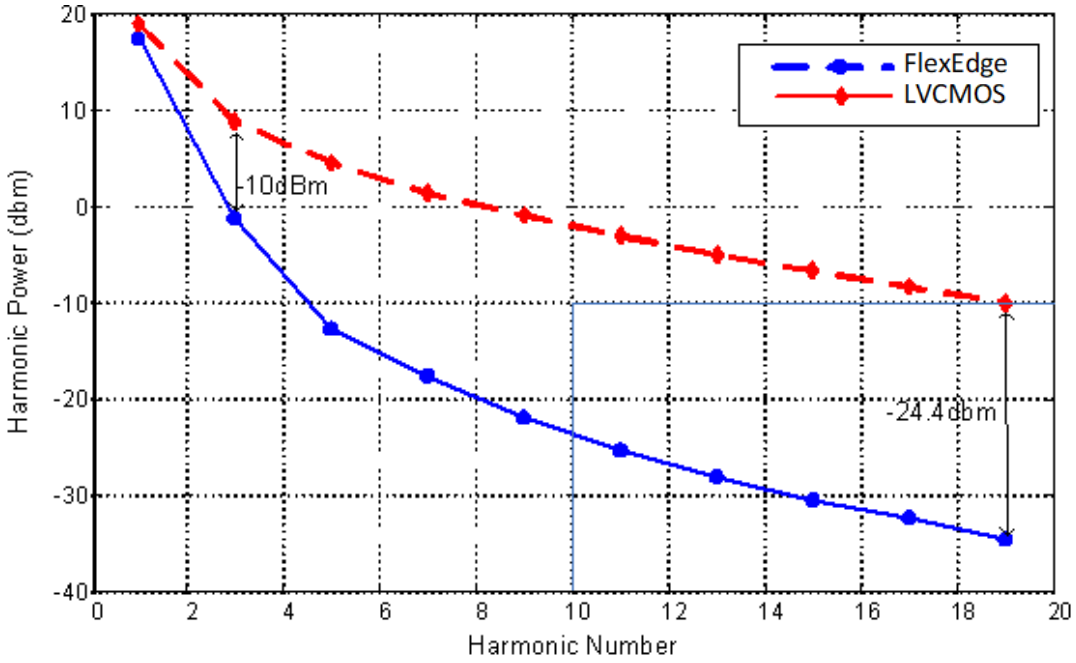

Figure 4: Slowing down rise/fall times improves radiated EMI of clock harmonics

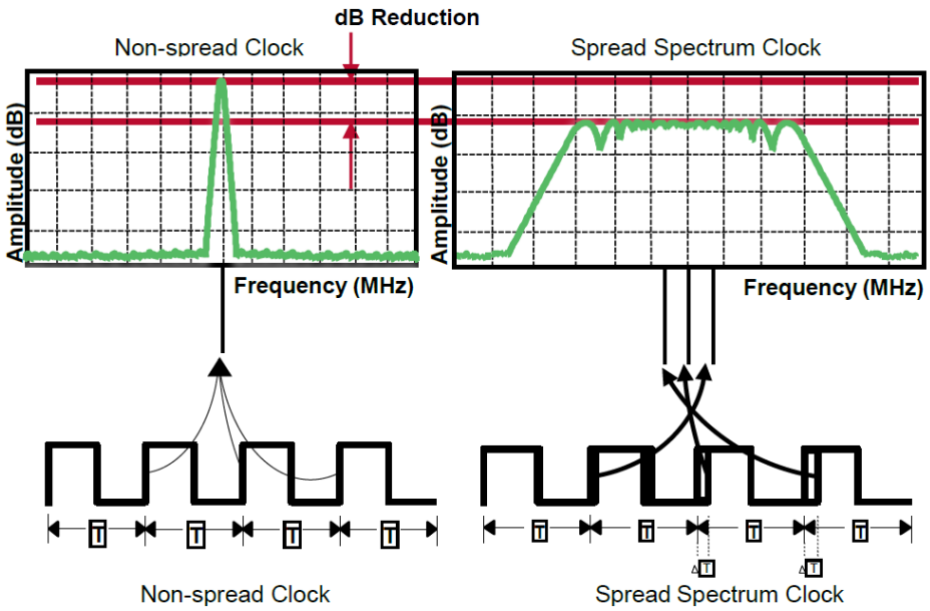

Figure 5: Spread spectrum clocking distributes peak carrier energy over a wider frequency range

Regardless of synchronous or asynchronous mode, FPD-Link is compatible with spread spectrum clocking (SSC) for EMI reduction. SSC spreads the carrier energy over a wide spectrum, hence reducing its peak amplitude. SSC is usually generated by the FPD-Link chipset. Select SiTime devices such as the SiT9025 have the possibility to generate SSC modulation internally.

7. Featured SiTime Products

Type	Product	Frequency	Key Features	Key Values
Low Power Automotive Oscillator (AEC-Q100)	SiT1625	44 standard frequencies incl. 25 MHz (SiT1625A) for FPD-Link IV ADAS and 27 MHz (SiT1625C) for FPD-Link IV Infotainment	• -40°C to +125°C • ±25, ±30, ±50 ppm stability • 1612, 2016, 2520, 3225 packages • 500 fs RMS jitter[1] • 2.3 mA typ. current consumption	• High reliability • Extended temperature range • EMI reduction features • Small footprint • Low power • Low jitter enables highest speed links
Clock Generator	SiT9128x	1 to 1000 MHz	• 4 configurable output pairs: 4 differential pairs or 8 single-ended outputs • ±30, ±50 ppm stability • LVPECL, LVDS, HCSL, Low-power HCSL, FlexSwing™ • < 200 fs RMS jitter[1] • Spread spectrum • -40°C to +125°C • 4x4 mm package	• High reliability • Integration: generates all clocks for multiple FPD-Links as well as more clocks in the system: PCI-Express, Ethernet, SoC clocks, etc. • No external resonator needed • Advanced features for AD/ADAS applications • Please contact SiTime for information on advanced features and product availability

[1] 12 kHz to 20 MHz integration range

8. SiTime Advantages

All SiTime devices offer the following advantages over quartz crystals, which are particularly important for automotive applications:

- Up to 50x better reliability: Apart from reducing the amount of field failures, the better reliability translates into a lower FIT rate. This provides better Hardware Safety metrics in an FMEDA, the quantitative analysis required as part of a Functional Safety assessment.
- Up to 100x better resilience to shock, vibration and electromagnetic interference, due to the smaller size (0.4 x 0.4 mm) and lower mass of MEMS resonators compared to crystals.
- EMI reduction features: drive strength selection, spread spectrum clocking

9. References

[1] Jitter Fundamentals on the Timing Essentials Learning Hub

[2] Clock Jitter in High-Speed Serial Links on the Timing Essentials Learning Hub

[3] FPD-Link III Advanced ADAS Serializer Clocking Mode (TI)

[4] FPD-Link III ADAS Serializer Clocking Mode (TI)

[5] FPD-Link Learning Center (TI)