CS00118

AEC-Q100, Ultra-low Jitter Differential Oscillator

Features

- AEC-Q100 Grade 2 temperature range (-40°C to 105°C). Grade 3 and 4 also available
- Any frequency between 1 MHz and 220 MHz, accurate to 6 decimal places. For frequency between 220 and 725 MHz, see SiT9387
- LVPECL, LVDS and HCSL output signaling types
- 0.23 ps RMS (typ) phase jitter (random, 12 kHz to 20 MHz)
- Frequency stability as low as ±10 ppm – contact SiTime
- Industry-standard packages: 3.2 x 2.5, 7.0 x 5.0 mm. Contact SiTime for 5.0 x 3.2 mm package

Applications

- Automotive, and other high reliability electronics
- Infotainment systems, collision detection devices and in-vehicle 10/40/100 Gbps Ethernet

Electrical Characteristics

Table 1. Electrical Characteristics — Common to LVPECL, LVDS and HCSL

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination show in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	1	–	220	MHz	Accurate to 6 decimal places
Frequency Stability						
Frequency Stability		-10	–	+10	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations. Contact SiTime for ± 10 ppm.
		-20	–	+20	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations. Contact SiTime for ± 10 ppm.
		-25	–	+25	ppm	
		-50	–	+50	ppm	
First Year Aging	F_1y	–	±1	–	ppm	At 25°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	AEC-Q100 Grade 4
		-40	–	+85	°C	AEC-Q100 Grade 3
		-40	–	+105	°C	AEC-Q100 Grade 2
Supply Voltage						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.70	3.0	3.30	V	
		2.52	2.8	3.08	V	
		2.25	2.5	2.75	V	
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE
Input Pull-up Impedance	Z_in	–	100	-	kΩ	Pin 1, OE logic high or logic low
Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Startup and OE Timing						
Start-up Time	T_start	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value.
OE Enable/Disable Time	T_oe	–	–	3.8	µs	f = 156.25 MHz. Measured from the time OE pin reaches rated VIH and VIL to the time clock pins reach 90% of swing and high-Z. See Figure 6 and Figure 7

Table 2. Electrical Characteristics – LVPECL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	89	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	58	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Maximum Output Current	I_driver	–	–	33	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	Vdd-1.15	–	Vdd-0.7	V	See Figure 2
Output Low Voltage	VOL	Vdd-2.0	–	Vdd-1.5	V	See Figure 2
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 3
Rise/Fall Time	Tr, Tf	–	225	310	ps	20% to 80%, see Figure 3
Jitter – 7.0 x 5.0 package						
RMS Period Jitter[1]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.225	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -20 to 70ºC and -40 to 85ºC.
		–	0.225	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature range -40 to 105ºC
		–	0.1		ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.
Jitter – 3.2 x 2.5 package						
RMS Period Jitter[1]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.225	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature range -20 to 70ºC and -40 to 85ºC.
		–	0.225	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature range -40 to 105ºC
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.

Notes:

1. Measured according to JESD65B

Table 3. Electrical Characteristics – LVDS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	79	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	58	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Output Characteristics						
Differential Output Voltage	VOD	250	–	450	mV	See Figure 4
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 4
Offset Voltage	VOS	1.125	–	1.375	V	See Figure 4
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 4
Rise/Fall Time	Tr, Tf	–	400	515	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 5
Jitter – 7.0 x 5.0 package						
RMS Period Jitter[2]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.215	0.265	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -20 to 70ºC and -40 to 85ºC.
		–	0.215	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature range -40 to 105ºC
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.
Jitter – 3.2 x 2.5 package						
RMS Period Jitter[2]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.235	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -20 to 70ºC and -40 to 85ºC
		–	0.235	0.320	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature range -40 to 105ºC
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.

Notes:

2. Measured according to JESD65B

Table 4. Electrical Characteristics – HCSL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	92	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	58	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Maximum Output Current	I_driver	–	–	35	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	0.60	–	0.90	V	See Figure 2
Output Low Voltage	VOL	-0.05	–	0.08	V	See Figure 2
Output Differential Voltage Swing	V_Swing	1.2	1.4	1.80	V	See Figure 3
Rise/Fall Time	Tr, Tf	–	360	495	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 3
Jitter – 7.0 x 5.0 package						
RMS Period Jitter[3]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.220	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature range -20 to 70ºC and -40 to 85ºC.
		–	0.220	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature range -40 to 105ºC
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.
Jitter – 3.2 x 2.5 package						
RMS Period Jitter[3]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.230	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -20 to 70ºC and -40 to 85ºC.
		–	0.230	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature range -40 to 105ºC
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.

Notes:

3. Measured according to JESD65B

Table 5. Pin Description

Pin	Map	Functionality	
1	OE/NC	Output Enable (OE)	H[4]: specified frequency output L: output is high impedance
		Non Connect (NC)	H or L or Open: No effect on output frequency or other device functions
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	Vdd Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	Vdd	Power	Power supply voltage[5]

Top View

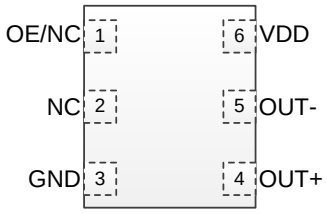


Figure 1. Pin Assignments

Notes:

4. In OE mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
5. A capacitor of value 0.1 µF or higher between Vdd and GND is required. An additional 10 µF capacitor between Vdd and GND is required for the best phase jitter performance

Table 6. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Vdd	-0.5	4.0	V
VIH		Vdd + 0.3V	V
VIL	-0.3		V
Storage Temperature	-65	150	ºC
Maximum Junction Temperature		130	ºC
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	ºC

Table 7. Thermal Considerations[6]

Package	θ_{JA}, 4 Layer Board (°C/W)	θ_{JC}, Bottom (°C/W)
3225, 6-pin	80	30
7050, 6-pin	52	19

Notes:

6. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 8. Maximum Operating Junction Temperature[7]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	95°C
85°C	110°C
105°C	130°C

Notes:

7. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 9. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	*g*
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	*g*
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Waveform Diagrams (continued)

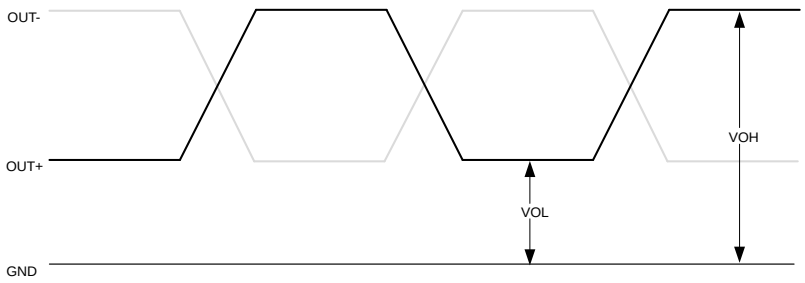


Figure 2. LVPECL/HCSL Voltage Levels per Differential Pin (OUT+/OUT-)

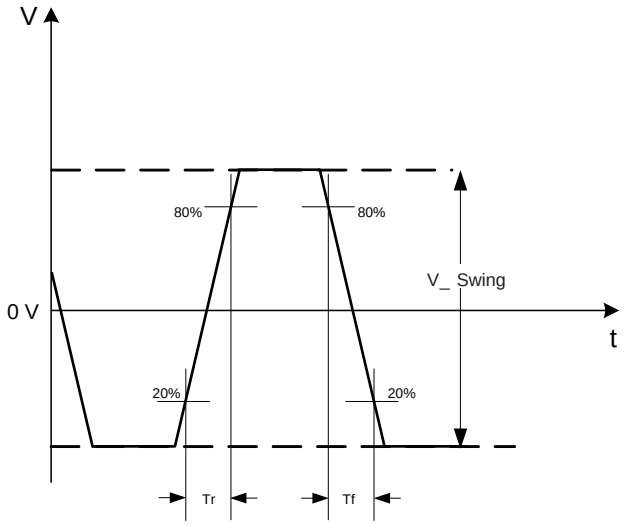


Figure 3. LVPECL/HCSL Voltage Levels across Differential Pair

Waveform Diagrams (continued)

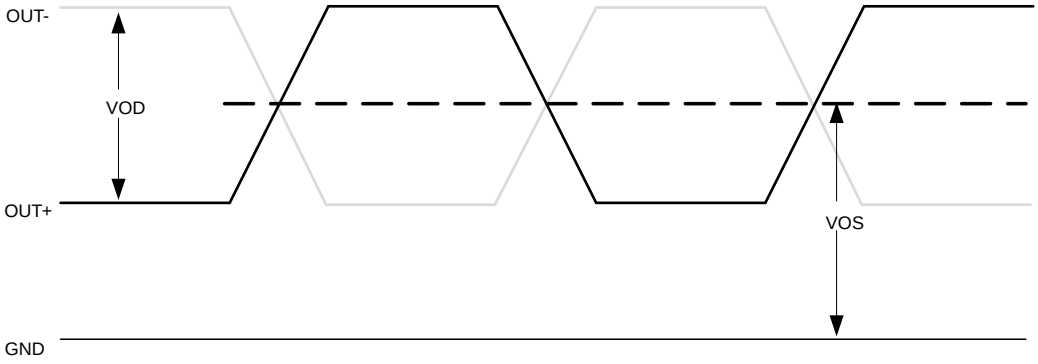


Figure 4. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

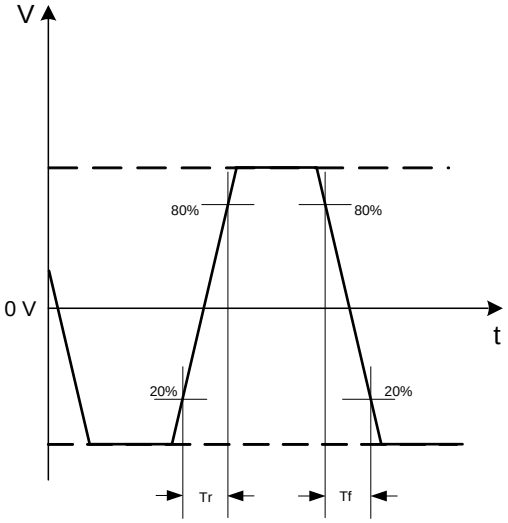


Figure 5. LVDS Differential Waveform

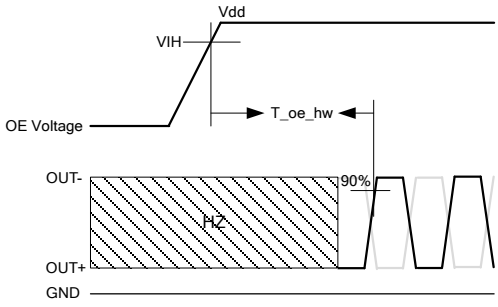


Figure 6. Hardware OE Enable Timing

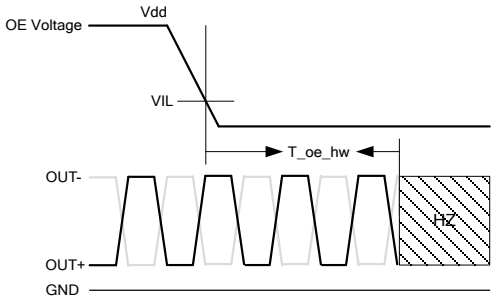


Figure 7. Hardware OE Disable Timing

Termination Diagrams

LVPECL:

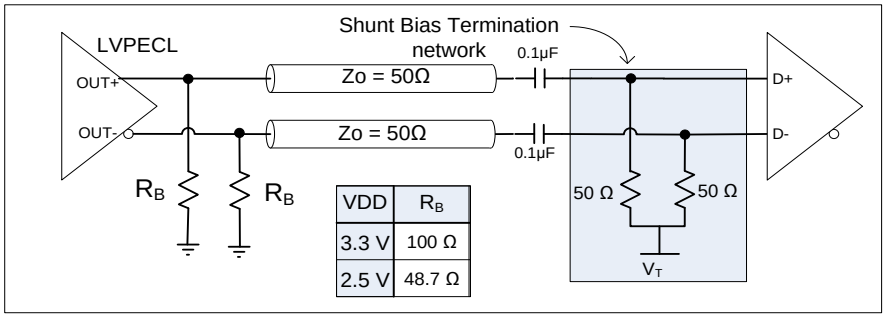


Figure 8. LVPECL with AC-coupled termination

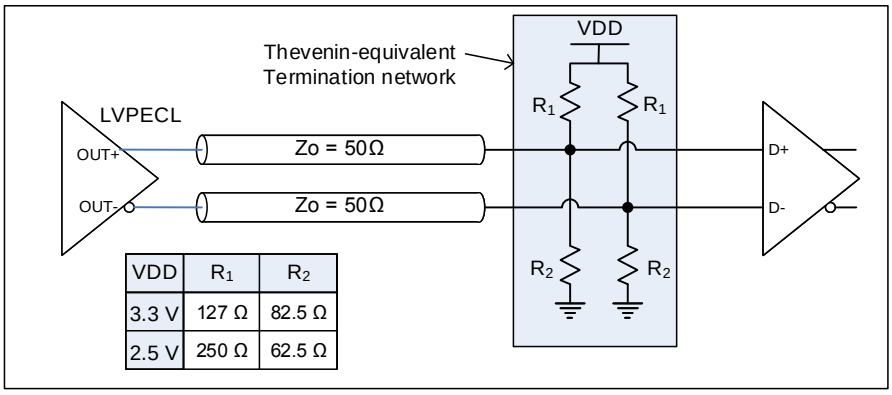


Figure 9. LVPECL DC-coupled load termination with Thevenin equivalent network

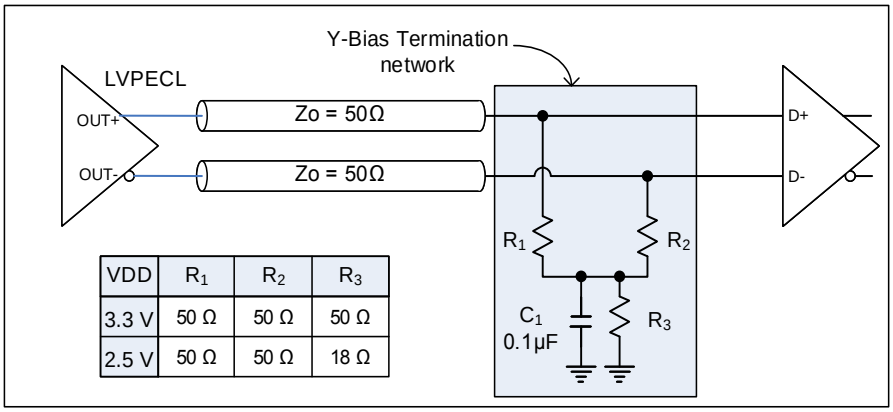


Figure 10. LVPECL with Y-Bias termination

Termination Diagrams (continued)

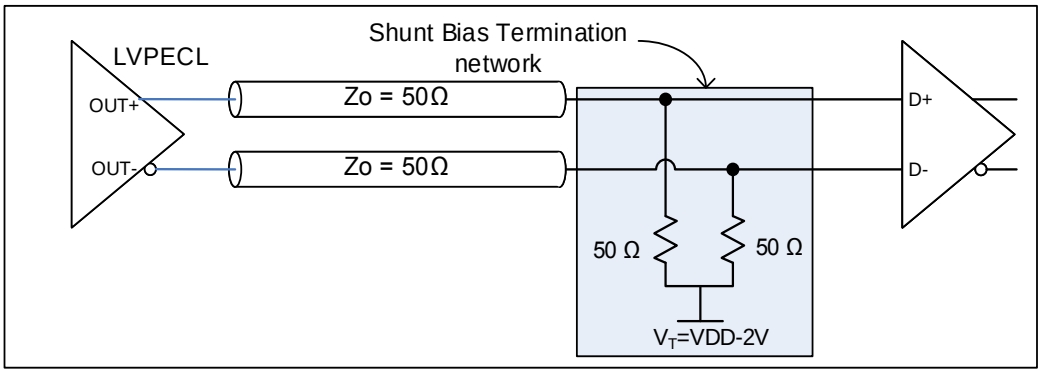


Figure 11. LVPECL with DC-coupled parallel shunt load termination

Termination Diagrams (continued)

LVDS:

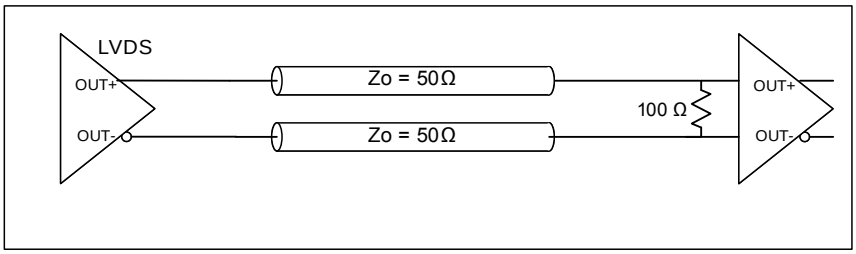


Figure 12. LVDS single DC termination at the load

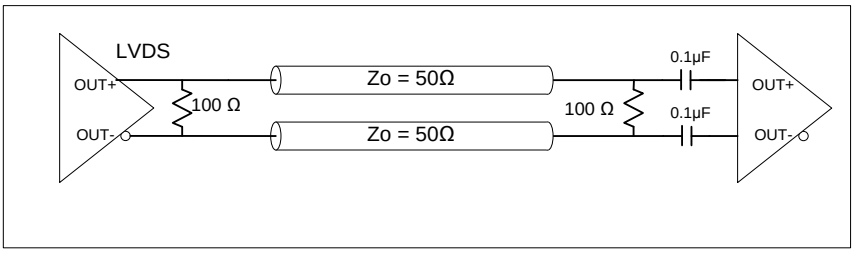


Figure 13. LVDS double AC termination with capacitor close to the load

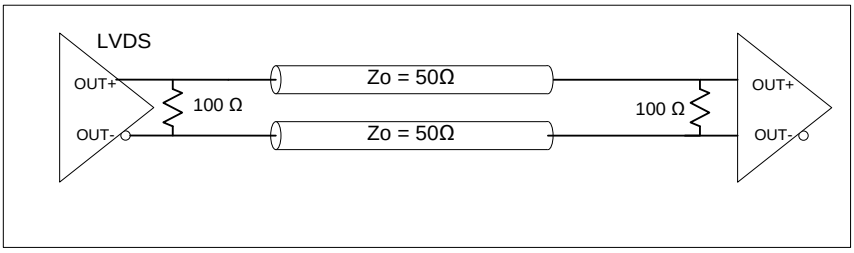


Figure 14. LVDS double DC termination

Termination Diagrams (continued)

HCSL:

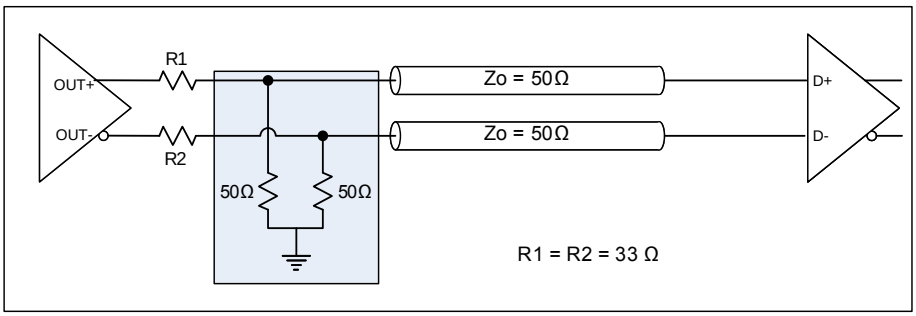
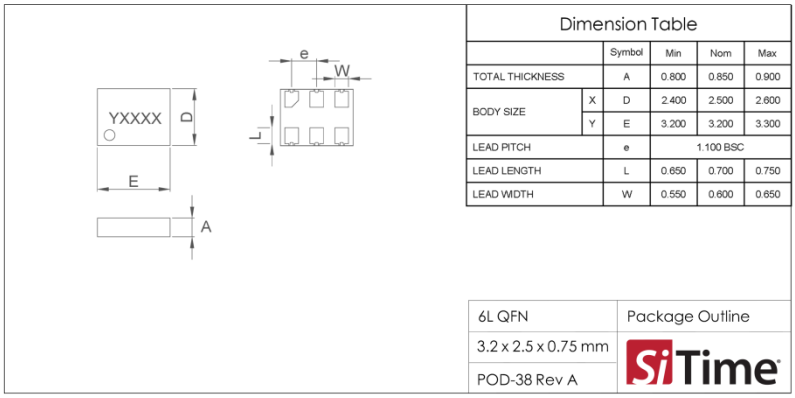


Figure 15. HCSL interface termination

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[8]	Recommended Land Pattern (Unit: mm)[9]
3.2 x 2.5 x 0.85 mm	**3.2 x 2.5 x 0.85 mm**
7.0 x 5.0 x 0.85 mm[10]	**7.0 x 5.0 x 0.85 mm[10]**

3.2 x 2.5 x 0.85 mm

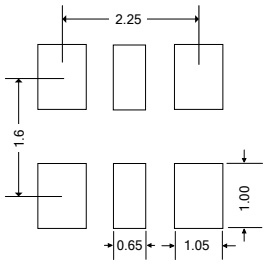


Dimension Table

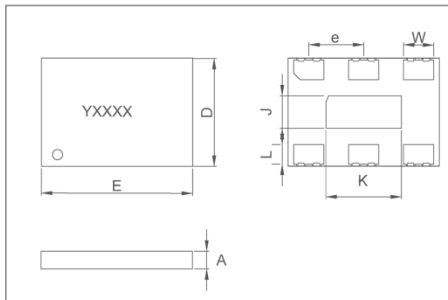
		Symbol	Min	Nom	Max
TOTAL THICKNESS		A	0.800	0.850	0.900
BODY SIZE	X	D	2.400	2.500	2.600
	Y	E	3.200	3.200	3.300
LEAD PITCH		e	1.100 BSC		
LEAD LENGTH		L	0.650	0.700	0.750
LEAD WIDTH		W	0.550	0.600	0.650

6L QFN	Package Outline
3.2 x 2.5 x 0.75 mm	
POD-38 Rev A	

3.2 x 2.5 x 0.85 mm



7.0 x 5.0 x 0.85 mm[10]

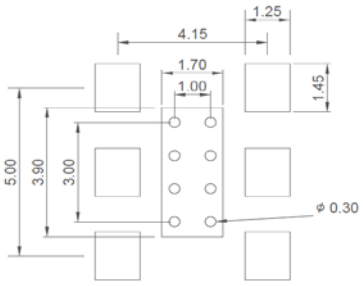


Dimension Table

		Symbol	Min	Nom	Max
TOTAL THICKNESS		A	0.800	0.850	0.900
BODY SIZE	X	D	4.900	5.000	5.100
	Y	E	6.900	7.000	7.100
EP SIZE	X	J	1.400	1.500	1.600
	Y	K	3.400	3.500	3.600
LEAD PITCH		e	2.540 BSC		
LEAD LENGTH		L	0.850	0.900	0.950
LEAD WIDTH		W	1.350	1.400	1.450

6L QFN	Package Outline
7.0 x 5.0 x 0.90 mm	
POD-37 Rev A	

7.0 x 5.0 x 0.85 mm[10]



Note:
Circles in center pad are thermal vias, recommended to improve thermal performance

Notes:

8. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
9. A capacitor of value 0.1 µF or higher between Vdd and GND is required. An additional 10 µF capacitor between Vdd and GND is required for the best phase jitter performance
10. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Marking Specification

The marking contains two lines of information. The first line indicates the frequency, operating voltage and signaling type of the device. The second line is the trace code that includes the assembly location and lot number. This marking option is selected by entering an “M”, “V”, “Z”, “H” or “J” as the last digit of the ordering part number depending on the packing method required.

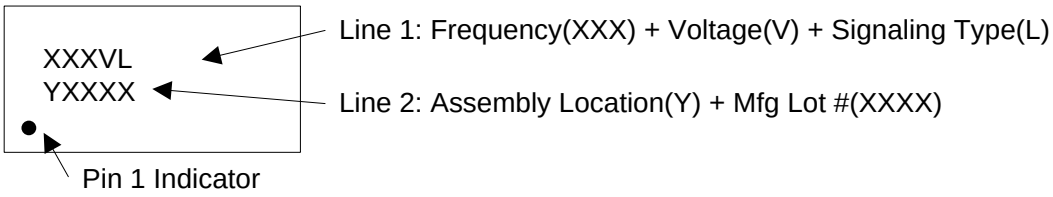


Figure 16. 7050 and 3225 packages 2-line marking

Line 1:

The number of characters for frequency shown in the top mark is limited by package size. The line 1 marking for each package size is shown in the table below.

Table 10. The first line of the mark for different frequencies with examples

Device Size (mm x mm)	# of characters	Example for <10 MHz	Example for <100 MHz	Example for >100 MHz
7.0 x 5.0	5	X.XVL	XX.VL	XXXVL
3.2 x 2.5	5	X.XVL	XX.VL	XXXVL

The alpha characters “VL” in the top mark XXXVL specify the operating voltage and the output signaling type of the device.

“V” can have one of the following values.

A = 3.3V

B = 2.8V

C = 2.5V

D = 1.8V

“L” can have one of the following values.

B = LVPECL

C = LVDS

D = HCSL

Line 2:

The alpha character “Y” in the top mark YXXXX specifies the assembly location and can have one of the following values depending on the assembly location of the device.

“Y” can have one of the following values.

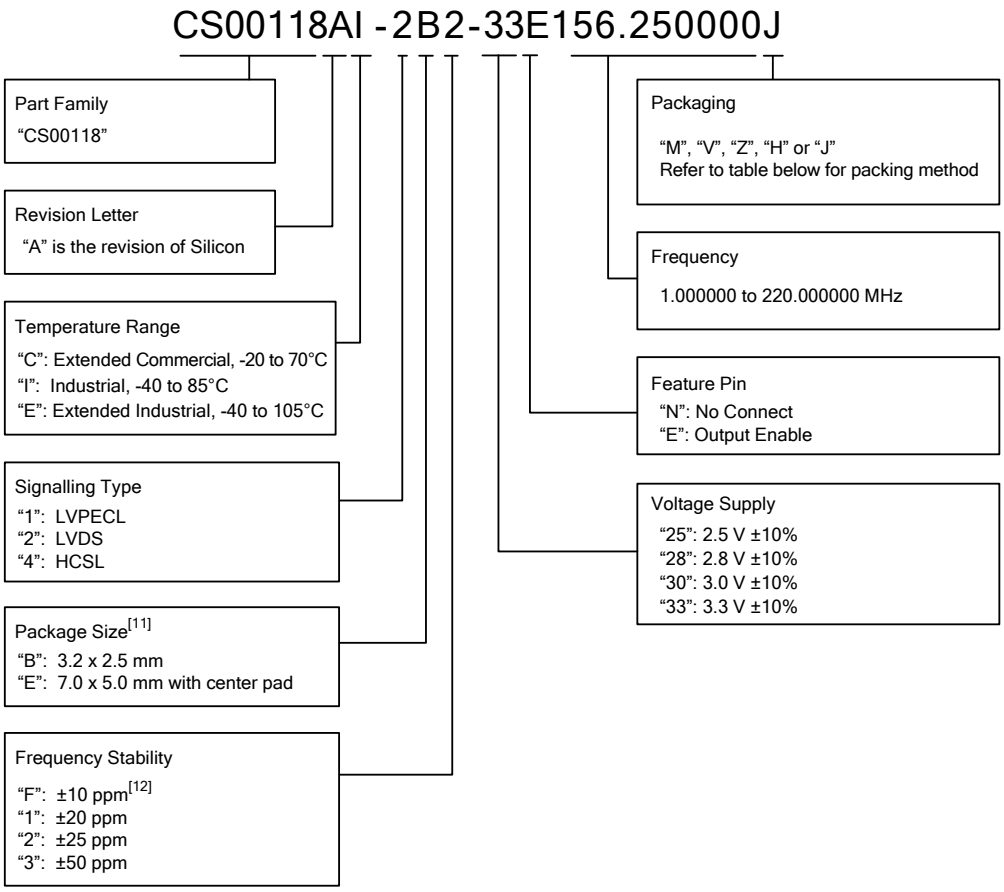
A = Carsem, Malaysia

B = UTAC, Thailand

C = ASE, Taiwan

“XXXX” indicates the last 4 alphanumeric characters of the device lot code.

Ordering Information



Notes:

11. Contact SiTime for 5.0 x 3.2 mm package
12. Contact SiTime for ±10 ppm option.
13. Bulk is available for sampling only.

Table 11. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	Bulk For sampling only	8 mm T&R (3ku)	8 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	M	—	—	V	Z
3.2 x 2.5	M	H	J	—	—

Table 12. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
Part number Generator	Tool used to create the part number based on desired features.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	http://www.sitime.com/manufacturing-notes
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Table 13. Revision History

Revision	Release Date	Change Summary
1.0	06/11/2018	Final release

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