CS00112

Ultra-Small, 1 to 26 MHz Oscillator

Description

The CS00112 is the industry's smallest and the lowest power MHz oscillator. With 0.1 mW of active power consumption at 3.072 MHz output frequency, this µPower oscillator enables longer battery life for a wearable, IoT or mobile device compared to a quartz-based oscillator or resonator.

The device comes in the smallest 1.5 mm x 0.8 mm package. The unique combination of ultra-low power, ultra-small package and flexible output frequency makes it ideal for power sensitive and space constrained applications.

Applications

- Tablets
- Fitness bands
- Health and medical monitoring
- Wearables
- Portable audio
- Input devices
- IoT devices

Features

- Ultra-low current consumption of 60 µA at 3.072 MHz
- Ultra-small 1.5 mm x 0.8 mm package
- 1 to 26 MHz with 6 decimal places of accuracy
- Operating temperature from -40°C to 85°C. Contact SiTime for -40°C to 105°C option
- Frequency stability as low as ±100 ppm. Contact SiTime for ±25 ppm or ±50 ppm options
- Programmable output drive strength for best EMI or driving multiple loads
- Ultra-light weight of 1.28 mg
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

TempFlat MEMS™

Electrical Specifications

Table 1. Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	1.000000		26.000000	MHz	
Frequency Stability and Aging						
Initial Tolerance	f_tol	-15	–	+15	ppm	Frequency offset at 25°C post reflow
Frequency Stability	f_stab	-100	–	+100	ppm	Inclusive of initial tolerance, and variations over operating temperature, rated power supply voltage and output load. Contact SiTime for ±25 or ±50 ppm options.
First Year Aging	f_1year	-3		+3	ppm	At 25°C
Operating Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial. Contact SiTime for -40°C to 105°C option.
Supply Voltage and Current Consumption						
Supply Voltage	VDD	1.62	1.8	1.98	V	
		2.25	–	3.63	V	Any voltage from 2.25 to 3.63V
Current Consumption[1]	IDD	–	60	–	µA	f = 3.072 MHz, Vdd = 1.8V, no load
		–	110	130	µA	f = 6.144 MHz, Vdd = 1.8V, no load
		–	230	270	µA	f = 6.144 MHz, Vdd = 1.8V, 10 pF load
		–	–	160	µA	f = 6.144 MHz, Vdd = 2.25V to 3.63V, no load
		–	160	–	µA	f = 12 MHz, Vdd = 1.8V, no load
Standby Current	I_std	–	0.7	1.3	µA	Vdd = 1.8V, ST pin = LOW, output is weakly pulled down
		–	–	1.5	µA	Vdd = 2.25V to 3.63V, ST pin = LOW, output is weakly pulled down

Table 1. Electrical Characteristics (continued)

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	T_r, T_f	–	4	8	ns	Vdd = 1.8V, 20% - 80%. Contact SiTime for other programmable rise/fall options
		–	–	8	ns	Vdd = 2.25V to 3.63V, 20% - 80%. Contact SiTime for other programmable rise/fall options
Output High Voltage	VOH	90%	–	–	VDD	IOH = -0.5 mA (Vdd = 1.8V) IOH = -1.2 mA (Vdd = 2.25V to 3.63V)
Output Low Voltage	VOL	–	–	10%	VDD	IOL = 0.5 mA (Vdd = 1.8V) IOL = 1.2 mA (Vdd = 2.25V to 3.63V)
Input Characteristics						
Input High Voltage	VIH	80%	–	–	VDD	
Input Low Voltage	VIL	–	–	20%	VDD	
Input Slew Rate	In-slew	10	–	–	V/µs	
Input Pull-down Impedance	Z_in	300	–	–	kΩ	Standby mode (ST pin = LOW), Vdd = 1.8V
		270	–	–	kΩ	Standby mode (ST pin = LOW), Vdd = 2.25V to 3.63V
		2.5	–	–	MΩ	Active mode (ST pin = HIGH), Vdd = 1.8V
		1.3	–	–	MΩ	Active mode (ST pin = HIGH), Vdd = 2.25V to 3.63V
Startup, Standby and Resume Timing						
Startup Time	T_start	–	75	150	ms	Measured from the time VDD reaches 90% of its final value
Standby Time	T_stdby	–	–	20	µs	Measured from the time ST pin crosses 50% threshold
Resume Time	T_resume	–	2	3	ms	Measured from the time ST pin crosses 50% threshold
Jitter						
RMS Period Jitter	T_jitt	–	75	110	ps	f = 6.144 MHz, Vdd = 1.8V
		–	–	110	ps	f = 6.144 MHz, Vdd = 2.25V to 3.63V
RMS Phase Jitter	T_phj	–	0.8	2.5	ns	f = 6.144 MHz, Vdd = 1.8V, Integration bandwidth = 100 Hz to 40 kHz[2]
		–	–	2.5	ns	f = 6.144 MHz, Vdd = 2.25V to 3.63V, Integration bandwidth = 100 Hz to 40 kHz[2]

Notes:

1. Current consumption with load is a function of the output frequency and output load. For any given output frequency, the capacitive loading will increase current consumption equal to C_load*VDD*f(MHz).
2. Max spec inclusive of 25 mV peak-to-peak sinusoidal noise on VDD. Noise frequency 100 Hz to 20 MHz.

Table 2. Pin Description

Pin	Symbol		Functionality
1	nST	Input	L: Output is low (weak pull down). Device goes to the standby mode. Supply current reduces to I_std. H: Specified frequency output
2	OUT	Output	LVCMOS clock output
3	VDD	Power	Supply voltage. Bypass with a 0.01µF X7R capacitor.
4	GND	Power	Connect to ground

Top View

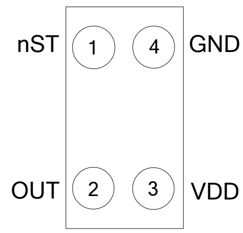


Figure 1. Pin Assignments

Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Condition	Value	Unit
Continuous Power Supply Voltage Range (VDD)		-0.5 to 3.63	V
Short Duration Maximum Power Supply Voltage (VDD)	<30 seconds	4.0	V
Continuous Maximum Operating Temperature		105	°C
Short Duration Maximum Operating Temperature	≤30 seconds	125	°C
Human Body Model (HBM) ESD Protection	JESD22-A115	2000	V
Charge-Device Model (CDM) ESD Protection	JESD22-C101	750	V
Machine Model (MM) ESD Protection	T_A = 25°C	200	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	MIl 883, Method 2002	10,000	*g*
Mechanical Vibration Resistance	MIl 883, Method 2007	70	*g*
1508 CSP Junction Temperature		150	°C
Storage Temperature		-65 to 150	°C
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Block Diagram

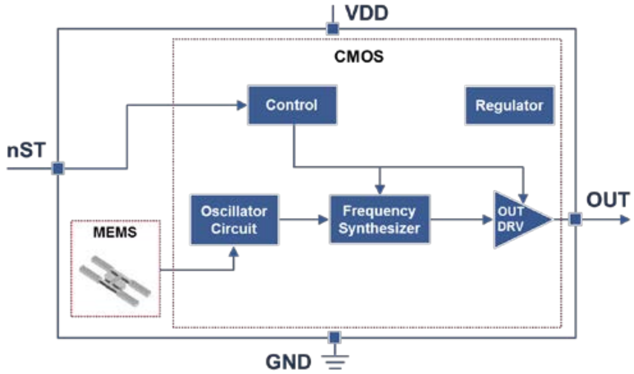


Figure 2. CS00112 Block Diagram

Device Operating Modes and Outputs

The CS00112 supports a ≤0.7 µA standby mode for battery-powered and other power sensitive applications. The switching between the active and standby modes is controlled by the logic level on the ST pin as shown in the table below.

Table 4. Operating Modes and Output States

nST Pin	MODE	OUTPUT	IDD Example
LOW	Standby	Hi-Z, pulled-down with 1 MΩ impedence	1.3 µA
FLOAT	Standby with 200 kΩ internal pull-down	Hi-Z, pulled-down with 1 MΩ impedence	1.3 µA
HIGH	Clock Active	Specified frequency	60 µA @ 3.072 MHz

Clock Active Mode

The CS00112 operates in the clock active mode when the ST pin is at logic HIGH. In the active mode, the device uses the on-chip frequency synthesizer to generate an output from the internal MEMS resonator reference. The frequency of the output is factory programmed based on the device ordering code.

Standby Mode

The CS00112 operates in the standby mode when the ST pin is at logic LOW or FLOAT. In the standby mode, all internal circuits with the exception of the MEMS oscillator circuit and the ST pin detection logic are turned off to reduce power consumption. While in standby mode, the input impedance of the ST pin is increased to further reduce system-level power consumption.

The output driver of the device in the standby mode is pulled-down with 1 MΩ impedance.

Output During Startup and Resume

The CS00112 starts up with the output disabled. The output is enabled once all internal circuit blocks are active, and logic HIGH is detected on the ST pin.

As shown in Table 4, logic LOW or FLOAT at the ST pin forces the CS00112 into the "standby" state, causing the output to disable. Upon pulling the ST pin HIGH, the device enters the "resume" state, keeping the output disabled. Once the "resume" state ends, the device output enables.

The first clock pulse after startup or resume is accurate to the rated stability.

Low Power Design Guidelines

For high EM noise environments, we recommend the following design guidelines:

- Place oscillator as far away from EM noise sources as possible (e.g., high-voltage switching regulators, motor drive control).
- Route noisy PCB traces, such as digital data lines or high di/dt power supply lines, away from the SiTime oscillator.
- Place a solid GND plane underneath the SiTime oscillator to shield the oscillator from noisy traces on the other board layers.

Manufacturing Guidelines

- No Ultrasonic or Megasonic Cleaning: Do not subject the CS00112 to an ultrasonic or megasonic cleaning environment. Permanent damage or long-term reliability issues to the device may occur in such an event.
- Applying board-level underfill (BLUF) to the device is acceptable, but will cause a slight shift of few ppm in the initial frequency tolerance. Tested with UF3810, UF3808, and FP4530 underfill.
- Reflow profile, per JESD22-A113D.
- The CS00112 CSP includes a protective, opaque polymer top-coat. If the CS00112 will see intense light, especially in the 1.0-1.2µm IR spectrum, we recommend a protective "glob-top" epoxy or other cover to keep the light from negatively impacting the frequency stability.
- For additional manufacturing guidelines and marking/ tape-reel instructions, refer to SiTime Manufacturing Notes.

Test Circuit and Waveform

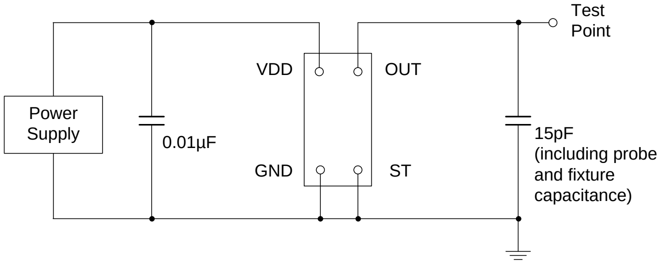


Figure 3. Test Circuit

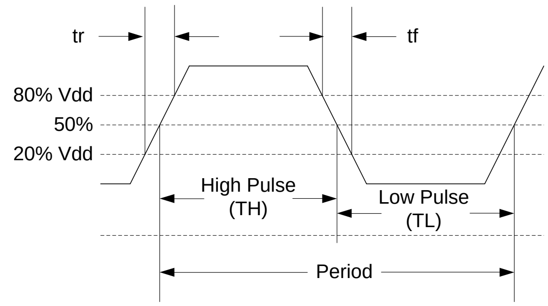
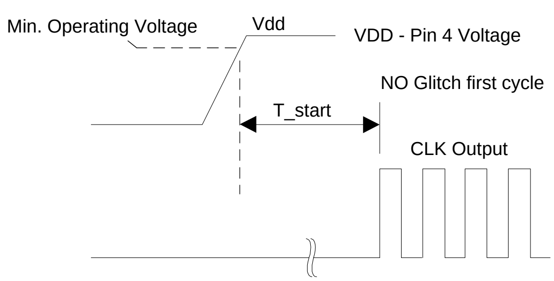


Figure 4. Waveform[3]

Note:

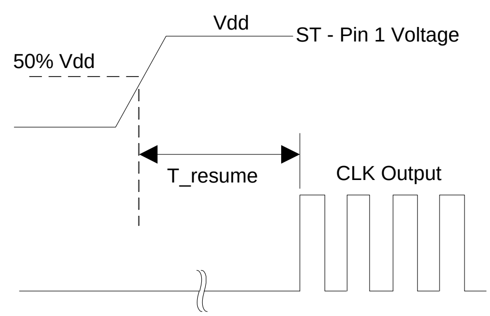
3. Duty Cycle is computed as Duty Cycle =TH/Period.

Timing Diagram



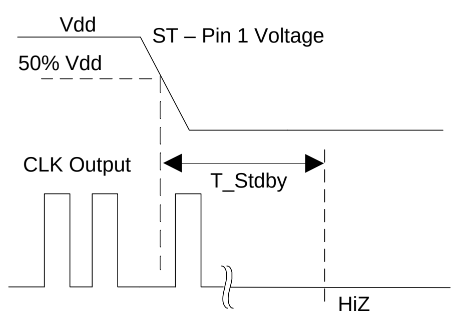
T_start: Time to valid clock output from power on

Figure 5. Startup Timing[4, 5]



T_resume: Time to valid clock output from the time ST pin crosses 50% threshold

Figure 6. Resume Timing[4, 5]



T_Stdby: Time for output to go high-Z from the time ST pin crosses 50% threshold

Figure 7. Standby Timing[4]

Notes:

4. CS00112 supports “no runt” pulses and “no glitch” output during startup or resume.
5. CS00112 supports gated output which is accurate within rated frequency stability from the first cycle.

Performance Plots[6]

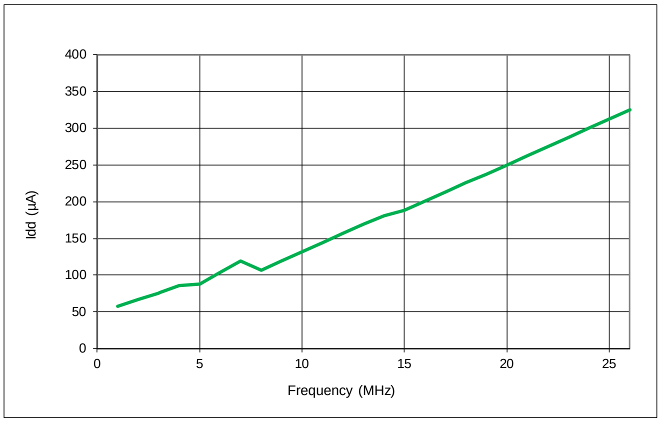


Figure 8. Idd vs Frequency without load

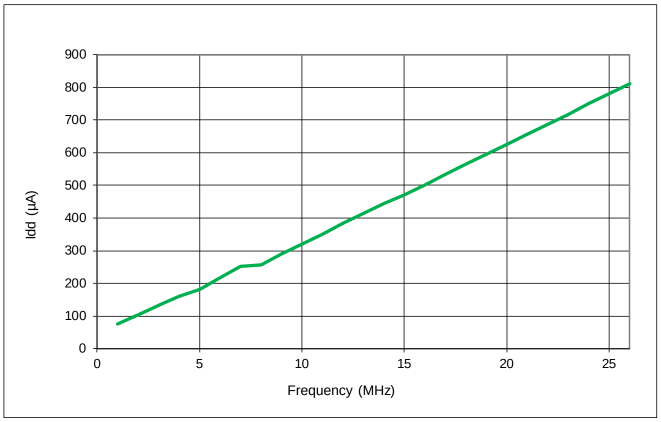


Figure 9. Idd vs Frequency with 10 pF load

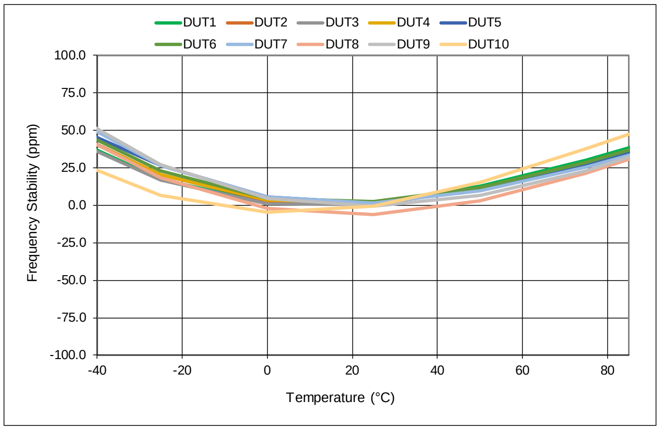


Figure 10. Frequency vs Temperature

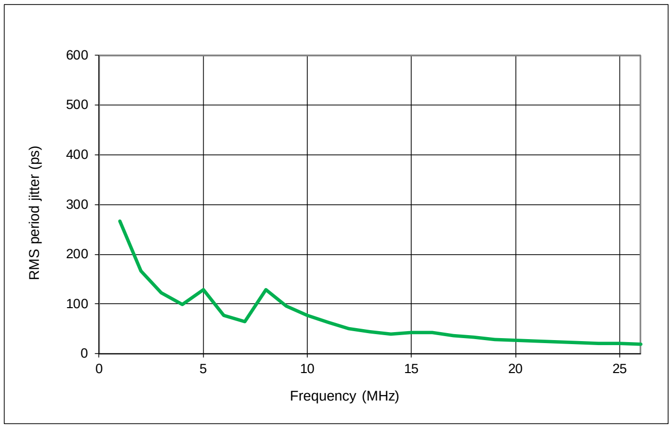


Figure 11. RMS Period Jitter vs Frequency

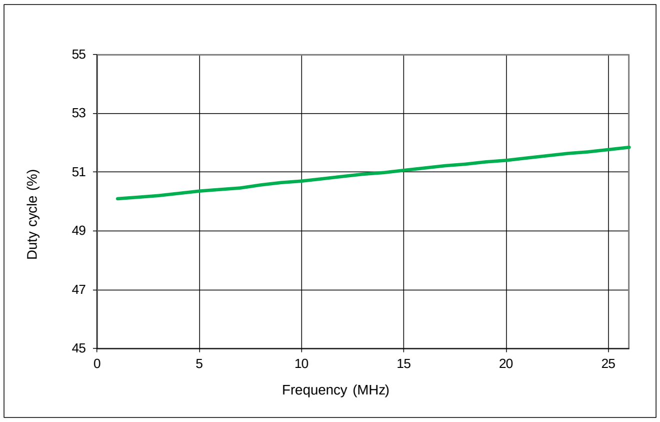


Figure 12. Duty Cycle vs Frequency

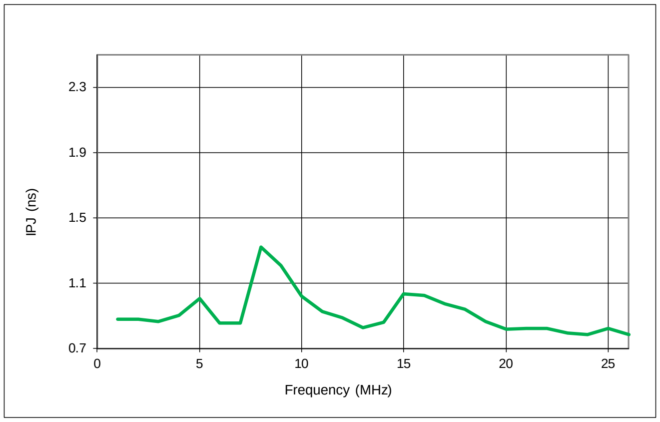


Figure 13. RMS Phase Jitter Random vs Frequency[7]

Performance Plots[6] (continued)

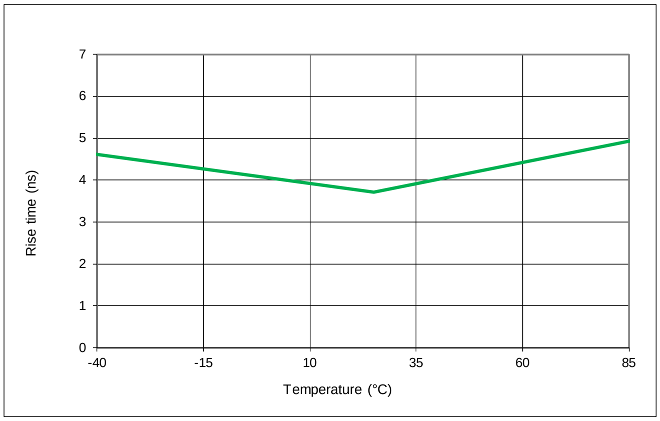


Figure 14. Rise Time vs Temperature[8]

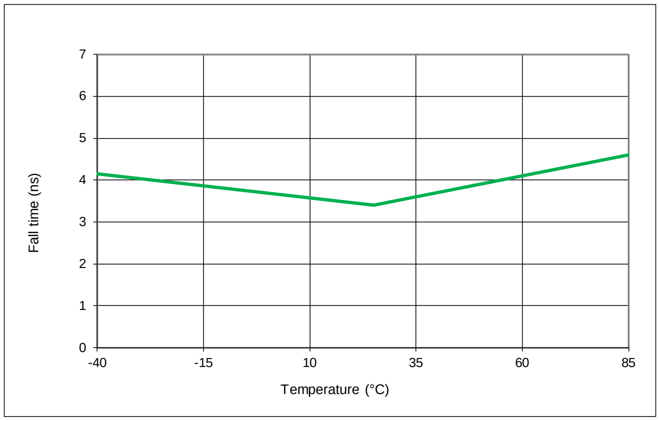


Figure 15. Fall Time vs Temperature[8]

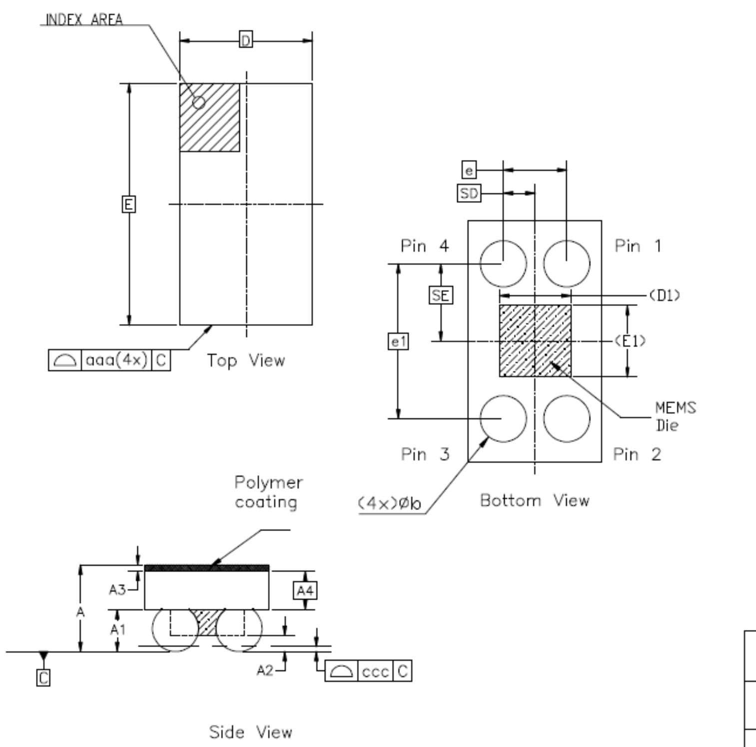
Notes:

6. All data is measured at room temperature, unless otherwise stated.
7. Data is measured with 15 pF load.
8. Integration range is from 100 Hz to 40 kHz.

Dimensions and Patterns

1.5 x 0.8 x 0.54 mm

Package Size – Dimensions (Unit: mm)



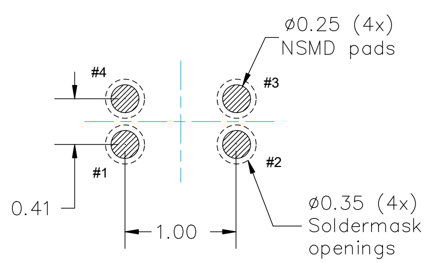
Dimension Table (mm)					
Item		SYMBOL	MINIMUM	NOMINAL	MAXIMUM
Total Thickness		A	0.48	0.54	0.60
Stand Off		A1	0.22		0.28
MEMS Clearance		A2	0.027		0.113
Film Thickness		A3	0.036	0.040	0.044
Wafer Thickness		A4	0.225	0.250	0.275
Ball Diameter		b	0.30	0.315	0.33
Ball Pitch	X	e	0.41 BSC		
	Y	e1	1.00 BSC		
MEMS	X	D1	0.46 REF		
	Y	E1	0.46 REF		
Body Size	X	D	0.84 BSC		
	Y	E	1.54 BSC		
Ball To Center	X	SD	0.205 BSC		
	Y	SE	0.500 BSC		
Package Edge Tolerance		aaa	0.040		
Coplanarity		ccc	0.075		

4 LD – 1.5 x 0.8 x 0.55 mm

Package Outline

POD-35 Rev A

Recommended Land Pattern (Unit: mm)



(soldermask openings shown with dashed line around NSMD pad)

Recommended 4-mil (0.1mm) stencil thickness

Ordering Information

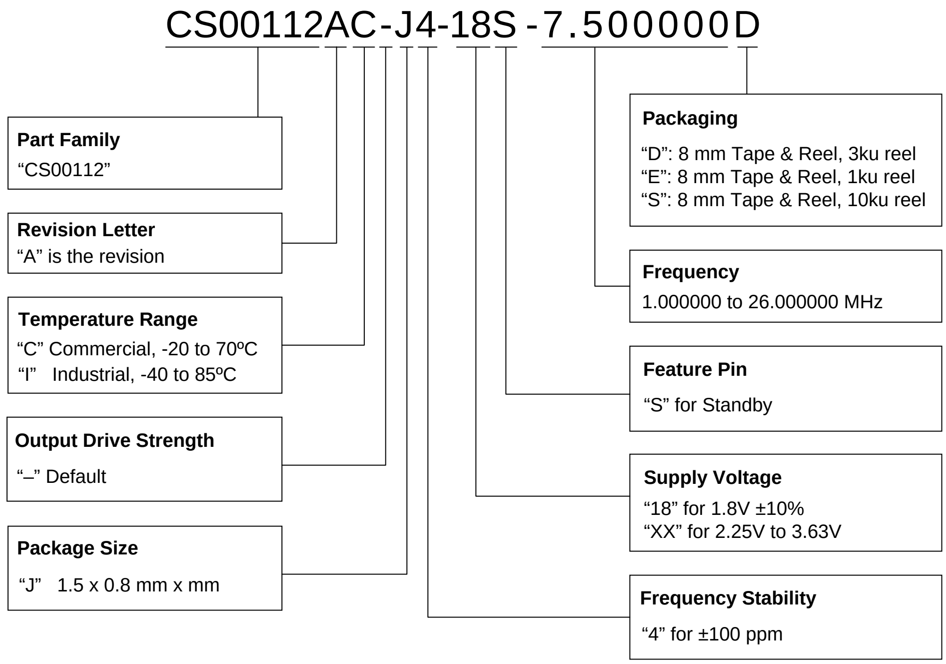


Table 5. Revision History

Version	Release Date	Change Summary
1.0	05/10/2017	Final production release
1.01	10/30/2017	Correct an example of full part number at ordering information
1.02	08/23/2018	Updated Manufacturing Guidelines Updated logo and company address, other page layout changes
1.1	09/06/2019	Added 2.25 to 3.63V supply voltage option Added package dimension table to the dimensions and patterns section

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