

CS00088

Low Power, Standard Frequency Oscillator



Features

- 51 standard frequencies between 3.75 MHz and 77.76 MHz
- 100% pin-to-pin drop-in replacement to quartz-based XO
- Excellent total frequency stability as low as ± 20 ppm
- Low power consumption of 3.6 mA typical
- Standby mode for longer battery life
- Fast startup time of 5 ms
- LVCMOS/HCMOS compatible output
- Industry-standard packages: 2.0 x 1.6, 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm
- Instant samples with [Time Machine II](#) and [field programmable oscillators](#)
- Pb-free, RoHS and REACH compliant

Applications

- Ideal for DSC, DVC, DVR, IP CAM, Tablets, e-Books, SSD, GPON, EPON, etc
- Ideal for high-speed serial protocols such as: USB, SATA, SAS, Firewire, 100M / 1G / 10G Ethernet, etc.



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Electrical Characteristics^[1]

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	(Refer to the frequency list page 10)			MHz	51 standard frequencies between 3.75 MHz and 77.76 MHz
Frequency Stability and Aging						
Frequency Stability	F_stab	-20	-	+20	ppm	Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature, rated power supply voltage and load.
		-25	-	+25	ppm	
		-50	-	+50	ppm	
Operating Temperature Range						
Operating Temperature Range	T_use	-20	-	+70	°C	Extended Commercial
		-40	-	+85	°C	Industrial
Supply Voltage and Current Consumption						
Supply Voltage	Vdd	1.62	1.8	1.98	V	Contact SiTime for 1.5V support
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
		2.25	-	3.63	V	
Current Consumption	Idd	-	3.8	4.5	mA	No load condition, f = 20 MHz, Vdd = 2.8V to 3.3V
		-	3.6	4.2	mA	No load condition, f = 20 MHz, Vdd = 2.5V
		-	3.4	3.9	mA	No load condition, f = 20 MHz, Vdd = 1.8V
OE Disable Current	I_OD	-	-	4	mA	Vdd = 2.5V to 3.3V, OE = GND, output is Weakly Pulled Down
		-	-	3.8	mA	Vdd = 1.8 V. OE = GND, output is Weakly Pulled Down
Standby Current	I_std	-	2.6	4.3	µA	ST = GND, Vdd = 2.8V to 3.3V, Output is Weakly Pulled Down
		-	1.4	2.5	µA	ST = GND, Vdd = 2.5V, Output is Weakly Pulled Down
		-	0.6	1.3	µA	ST = GND, Vdd = 1.8V, Output is Weakly Pulled Down
LVC MOS Output Characteristics						
Duty Cycle	DC	45	-	55	%	All Vdds
Rise/Fall Time	Tr, Tf	-	1	2	ns	Vdd = 2.5V, 2.8V, 3.0V or 3.3V, 20% - 80%
		-	1.3	2.5	ns	Vdd = 1.8V, 20% - 80%
		-	-	2	ns	Vdd = 2.25V - 3.63V, 20% - 80%
Output High Voltage	VOH	90%	-	-	Vdd	IOH = -4 mA (Vdd = 3.0V or 3.3V) IOH = -3 mA (Vdd = 2.8V and Vdd = 2.5V) IOH = -2 mA (Vdd = 1.8V)
Output Low Voltage	VOL	-	-	10%	Vdd	IOL = 4 mA (Vdd = 3.0V or 3.3V) IOL = 3 mA (Vdd = 2.8V and Vdd = 2.5V) IOL = 2 mA (Vdd = 1.8V)
Input Characteristics						
Input High Voltage	VIH	70%	-	-	Vdd	Pin 1, OE or ST
Input Low Voltage	VIL	-	-	30%	Vdd	Pin 1, OE or ST
Input Pull-up Impedance	Z_in	-	87	100	kΩ	Pin 1, OE logic high or logic low, or ST logic high
		2	-	-	MΩ	Pin 1, ST logic low

Note:

1. All electrical specifications in the above table are specified with 15 pF output load and for all Vdd(s) unless otherwise stated.

Electrical Characteristics^[1] (continued)

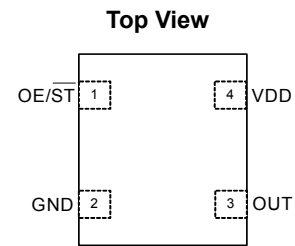
Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
Startup and Resume Timing						
Startup Time	T_start	–	–	5	ms	Measured from the time Vdd reaches its rated minimum value
Enable/Disable Time	T_oe	–	–	130	ns	f = 110 MHz. For other frequencies, T_oe = 100 ns + 3 * cycles
Resume Time	T_resume	–	–	5	ms	Measured from the time ST pin crosses 50% threshold
Startup Time	T_start	–	–	5	ms	Measured from the time Vdd reaches its rated minimum value
Jitter						
RMS Period Jitter	T_jitt	–	1.76	3	ps	f = 75 MHz, Vdd = 2.5V, 2.8V, 3.0V or 3.3V
		–	1.78	3	ps	f = 75 MHz, Vdd = 1.8V
RMS Phase Jitter (random)	T_phj	–	0.5	0.9	ps	f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz
		–	1.3	2	ps	f = 75 MHz, Integration bandwidth = 12 kHz to 20 MHz

Note:

- All electrical specifications in the above table are specified with 15 pF output load and for all Vdd(s) unless otherwise stated.

Pin Description

Pin	Symbol		Functionality
1	OE/ST	Output Enable	H or Open ^[2] : specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby	H or Open ^[2] : specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.
2	GND	Power	Electrical ground ^[3]
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage ^[3]



Notes:

- A pull-up resistor of <10 kΩ between OE/ST pin and Vdd is recommended in high noise environment.
- A capacitor value of 0.1 μF between Vdd and GND is required.

Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Junction Temperature	–	150	°C

Thermal Consideration

Package	θJA, 4 Layer Board (°C/W)	θJA, 2 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050	191	263	30
5032	97	199	24
3225	109	212	27
2520	117	222	26
2016	124	227	26

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

Test Circuit and Waveform^[4]

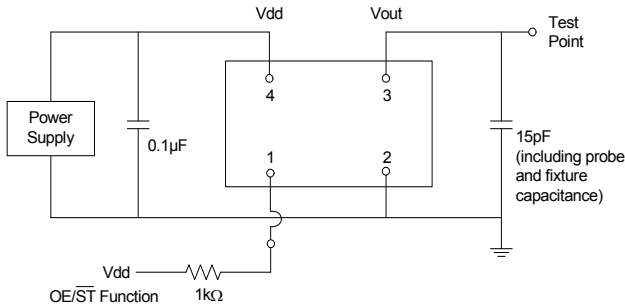


Figure 1. Test Circuit

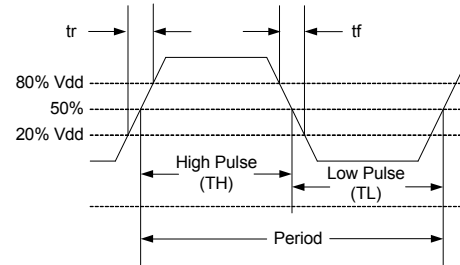


Figure 2. Waveform

Note:

4. Duty Cycle is computed as $Duty\ Cycle = TH/Period$.

Timing Diagram



Figure 3. Startup Timing (OE/ST Mode)

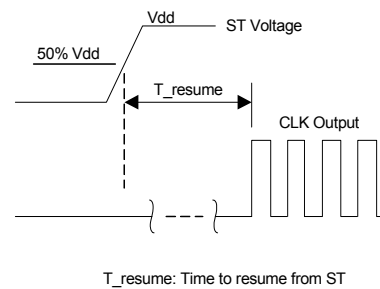


Figure 4. Standby Resume Timing (ST Mode Only)

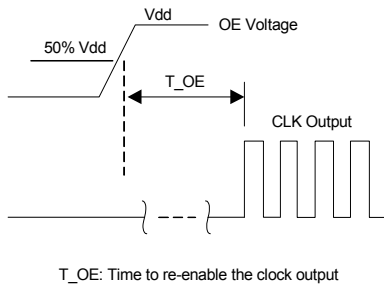


Figure 5. OE Enable Timing (OE Mode Only)



Figure 5. OE Disable Timing (OE Mode Only)

Notes:

- 5. CS00088 supports “no runt” pulses and “no glitch” output during startup or resume.
- 6. CS00088 supports gated output which is accurate within rated frequency stability from the first cycle.

Performance Plots



Figure 7. IDD vs Frequency

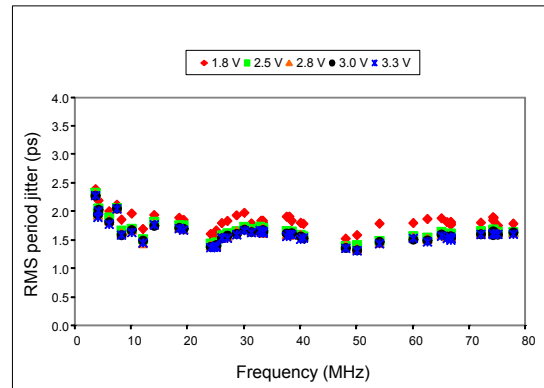
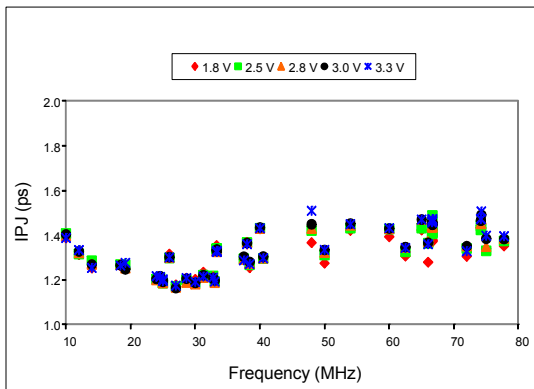
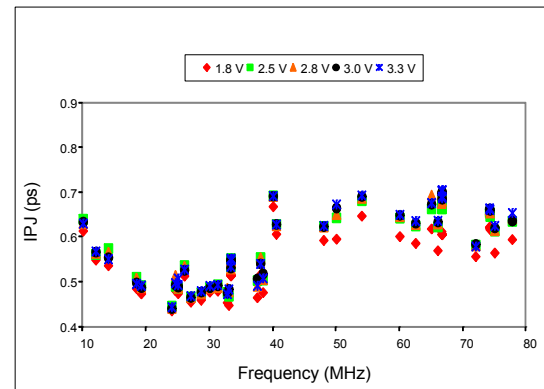


Figure 8. RMS Period Jitter vs Frequency



**Figure 9. RMS Phase Jitter vs Frequency
 (12 kHz to 20 MHz Integration Bandwidth)**



**Figure 10. RMS Phase Jitter vs Frequency
 (900 kHz to 20 MHz Integration Bandwidth)**



Figure 11. Duty Cycle vs Frequency

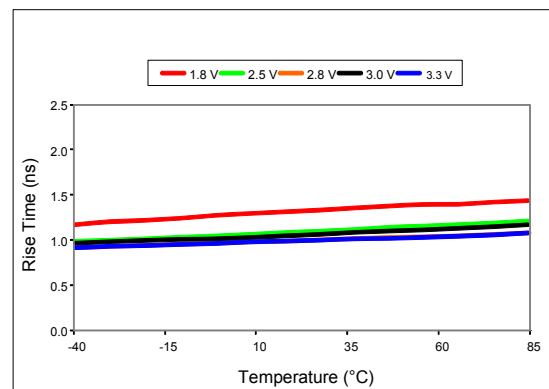


Figure 12. Rise Time vs Temperature, 20 MHz Output

Note:

7. All plots are measured with 15 pF load at room temperature, unless otherwise stated.

Programmable Drive Strength

The CS00088 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the SiTime Applications Note section; <http://www.sitime.com/support/application-notes>.

EMI Reduction by Slowing Rise/Fall Time

Figure 13 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

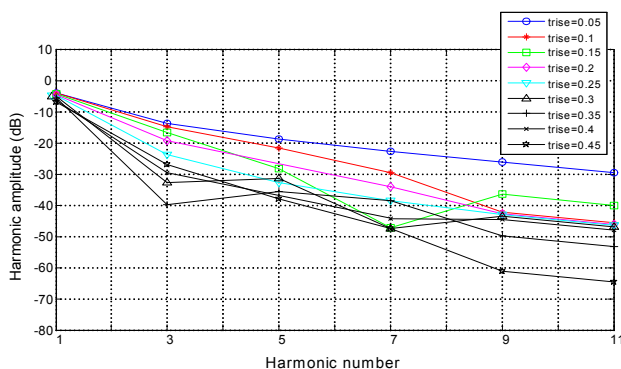


Figure 13. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to increase rise/fall time (edge rate) of the input clock. Some chipsets would require faster rise/fall time in order to reduce their sensitivity to this type of jitter. The CS00088 provides up to 3 additional high drive strength settings for very fast rise/fall time. Refer to the [Rise/Fall Time Tables](#) to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V CS00088 device with default drive strength setting, the typical rise/fall time is 1ns for 15 pF output load. The typical rise/fall time slows down to 2.6ns when the output load increases to 45 pF. One can

choose to speed up the rise/fall time to 1.68 ns by then increasing the drive strength setting on the CS00088.

The CS00088 can support up to 60 pF or higher in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the [Rise/Fall Time Tables](#) to determine the proper drive strength for the desired combination of output load vs. rise/fall time

CS00088 Drive Strength Selection

Tables 1 through 5 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the CS00088 nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 1 through 4, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max Frequency} = \frac{1}{5 \times \text{Trf}_{20/80}}$$

Where $\text{Trf}_{20/80}$ is the typical rise/fall time at 20% to 80% Vdd

Example 1

Calculate f_{MAX} for the following condition:

- Vdd = 1.8V (Table 1)
- Capacitive Load: 30 pF
- Desired Tr/f time = 3 ns (rise/fall time part number code = E)

Part number for the above example:

CS00088AIE12-18E-66.666660



Drive strength code is inserted here. Default setting is “-”

Rise/Fall Time (20% to 80%) vs C_{LOAD} Tables

Rise/Fall Time Typ (ns)					
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	6.16	11.61	22.00	31.27	39.91
A	3.19	6.35	11.00	16.01	21.52
R	2.11	4.31	7.65	10.77	14.47
B	1.65	3.23	5.79	8.18	11.08
T	0.93	1.91	3.32	4.66	6.48
E	0.78	1.66	2.94	4.09	5.74
U	0.70	1.48	2.64	3.68	5.09
F or "-": default	0.65	1.30	2.40	3.35	4.56

Table 1. V_{dd} = 1.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	4.13	8.25	12.82	21.45	27.79
A	2.11	4.27	7.64	11.20	14.49
R	1.45	2.81	5.16	7.65	9.88
B	1.09	2.20	3.88	5.86	7.57
T	0.62	1.28	2.27	3.51	4.45
E or "-": default	0.54	1.00	2.01	3.10	4.01
U	0.43	0.96	1.81	2.79	3.65
F	0.34	0.88	1.64	2.54	3.32

Table 2. V_{dd} = 2.5V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	3.77	7.54	12.28	19.57	25.27
A	1.94	3.90	7.03	10.24	13.34
R	1.29	2.57	4.72	7.01	9.06
B	0.97	2.00	3.54	5.43	6.93
T	0.55	1.12	2.08	3.22	4.08
E or "-": default	0.44	1.00	1.83	2.82	3.67
U	0.34	0.88	1.64	2.52	3.30
F	0.29	0.81	1.48	2.29	2.99

Table 3. V_{dd} = 2.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	3.60	7.21	11.97	18.74	24.30
A	1.84	3.71	6.72	9.86	12.68
R	1.22	2.46	4.54	6.76	8.62
B	0.89	1.92	3.39	5.20	6.64
T or "-": default	0.51	1.00	1.97	3.07	3.90
E	0.38	0.92	1.72	2.71	3.51
U	0.30	0.83	1.55	2.40	3.13
F	0.27	0.76	1.39	2.16	2.85

Table 4. V_{dd} = 3.0V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	3.39	6.88	11.63	17.56	23.59
A	1.74	3.50	6.38	8.98	12.19
R	1.16	2.33	4.29	6.04	8.34
B	0.81	1.82	3.22	4.52	6.33
T or "-": default	0.46	1.00	1.86	2.60	3.84
E	0.33	0.87	1.64	2.30	3.35
U	0.28	0.79	1.46	2.05	2.93
F	0.25	0.72	1.31	1.83	2.61

Table 5. V_{dd} = 3.3V Rise/Fall Times for Specific C_{LOAD}

Instant Samples with Time Machine and Field Programmable Oscillators

SiTime supports a field programmable version of the CS00088 low power oscillator for fast prototyping and real time customization of features. The [field programmable devices](#) (FP devices) are available for all five standard CS00088 package sizes and can be configured to one's exact specification using the [Time Machine II](#), an USB powered MEMS oscillator programmer.

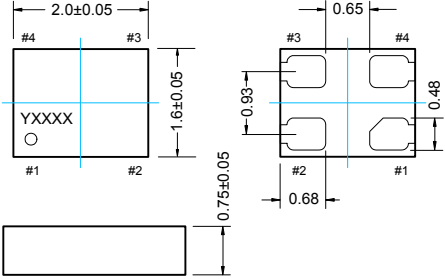
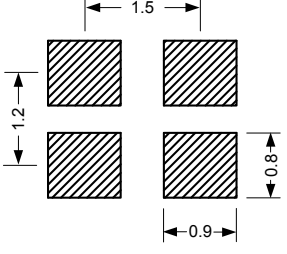
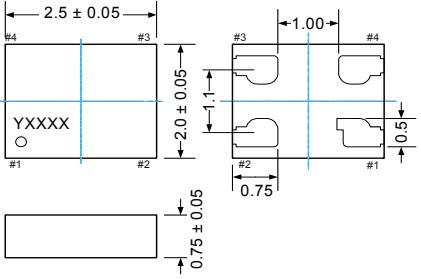
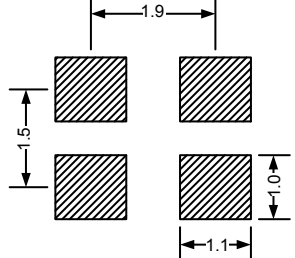
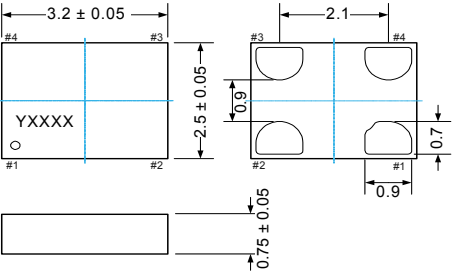
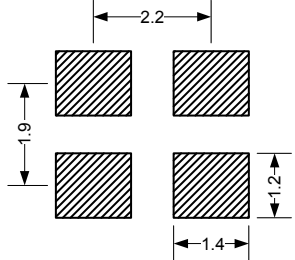
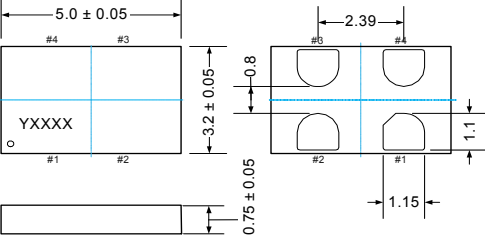
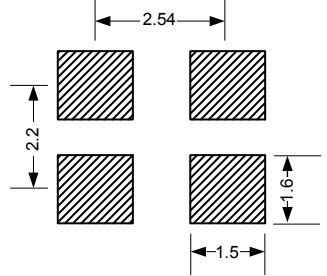
Customizable Features of the CS00088 FP Devices Include

- 51 standard frequencies between 3.75 MHz and 77.76MHz ([Refer to the frequency list page 10](#))
- Three frequency stability options, ± 20 ppm, ± 25 ppm, ± 50 ppm
- Two operating temperatures, -20 to 70°C or -40 to 85°C
- Five supply voltage options, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V and 2.25 to 3.65V continuous
- Output drive strength

For more information regarding SiTime's field programmable solutions, visit <http://www.sitime.com/time-machine> and <http://www.sitime.com/fp-devices>.

CS00088 is typically factory-programmed per customer ordering codes for volume delivery.

Dimensions and Patterns

Package Size – Dimensions (Unit: mm) ^[8]	Recommended Land Pattern (Unit: mm) ^[9]
<p>2.0 x 1.6 x 0.75 mm</p>  <p>Top view dimensions: 2.0 ± 0.05 mm (width), 1.6 ± 0.05 mm (height). Pin locations: #1, #2, #3, #4. Marking: YXXXX, ○. Bottom view dimensions: 0.75 ± 0.05 mm (height), 0.68 mm (pin width), 0.93 mm (pin pitch), 0.65 mm (pin width), 0.48 mm (pin height).</p> <p>Recommended Land Pattern: 1.5 mm (width), 1.2 mm (height), 0.9 mm (pitch), 0.8 mm (height).</p>	 <p>Land pattern dimensions: 1.5 mm (width), 1.2 mm (height), 0.9 mm (pitch), 0.8 mm (height).</p>
<p>2.5 x 2.0 x 0.75 mm</p>  <p>Top view dimensions: 2.5 ± 0.05 mm (width), 2.0 ± 0.05 mm (height). Pin locations: #1, #2, #3, #4. Marking: YXXXX, ○. Bottom view dimensions: 0.75 ± 0.05 mm (height), 0.75 mm (pin width), 1.1 mm (pin pitch), 1.00 mm (pin width), 0.5 mm (pin height).</p> <p>Recommended Land Pattern: 1.9 mm (width), 1.5 mm (height), 1.1 mm (pitch), 1.0 mm (height).</p>	 <p>Land pattern dimensions: 1.9 mm (width), 1.5 mm (height), 1.1 mm (pitch), 1.0 mm (height).</p>
<p>3.2 x 2.5 x 0.75 mm</p>  <p>Top view dimensions: 3.2 ± 0.05 mm (width), 2.5 ± 0.05 mm (height). Pin locations: #1, #2, #3, #4. Marking: YXXXX, ○. Bottom view dimensions: 0.75 ± 0.05 mm (height), 0.9 mm (pin width), 0.9 mm (pin pitch), 2.1 mm (pin width), 0.7 mm (pin height).</p> <p>Recommended Land Pattern: 2.2 mm (width), 1.9 mm (height), 1.4 mm (pitch), 1.2 mm (height).</p>	 <p>Land pattern dimensions: 2.2 mm (width), 1.9 mm (height), 1.4 mm (pitch), 1.2 mm (height).</p>
<p>5.0 x 3.2 x 0.75 mm</p>  <p>Top view dimensions: 5.0 ± 0.05 mm (width), 3.2 ± 0.05 mm (height). Pin locations: #1, #2, #3, #4. Marking: YXXXX, ○. Bottom view dimensions: 0.75 ± 0.05 mm (height), 1.15 mm (pin width), 1.1 mm (pin pitch), 2.39 mm (pin width), 0.8 mm (pin height).</p> <p>Recommended Land Pattern: 2.54 mm (width), 2.2 mm (height), 1.5 mm (pitch), 1.6 mm (height).</p>	 <p>Land pattern dimensions: 2.54 mm (width), 2.2 mm (height), 1.5 mm (pitch), 1.6 mm (height).</p>

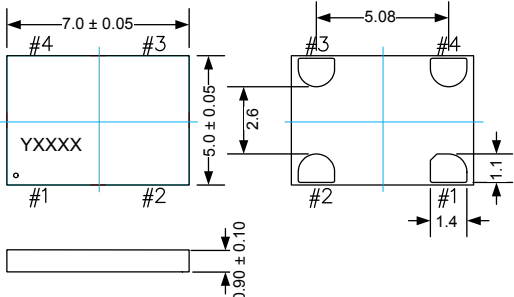
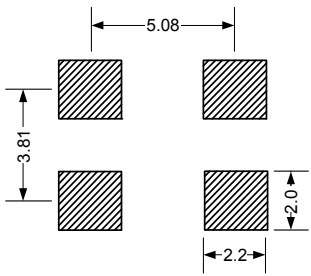
Notes:

- Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
- A capacitor of value 0.1 μF between Vdd and GND is required.

CS00088

Low Power, Standard Frequency Oscillator

Dimensions and Patterns

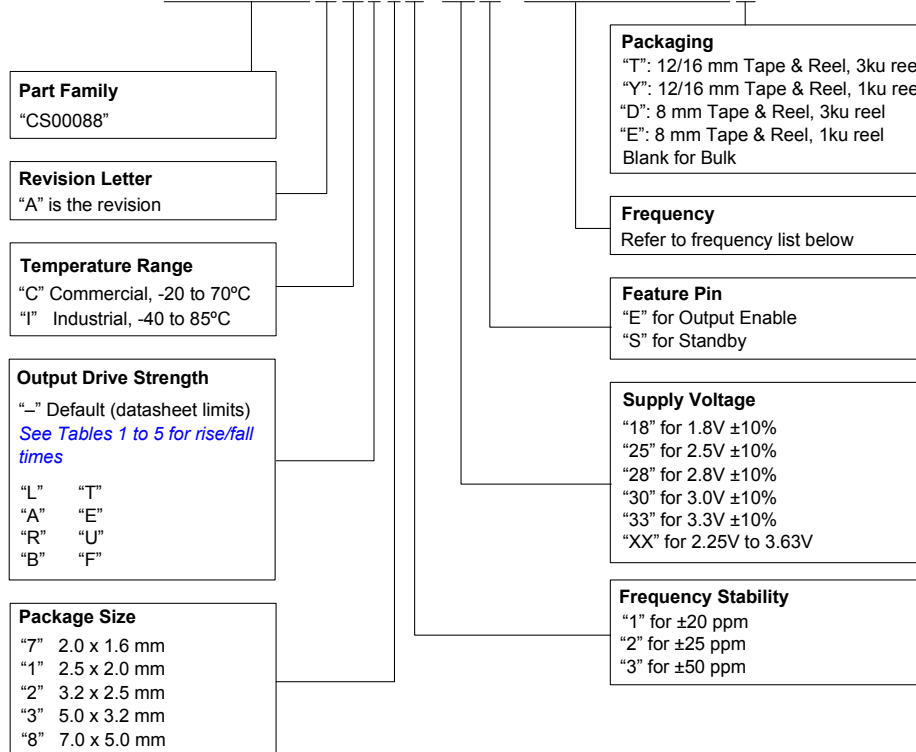
Package Size – Dimensions (Unit: mm) ^[10]	Recommended Land Pattern (Unit: mm) ^[11]
<p>7.0 x 5.0 x 0.90 mm</p> 	

Notes:

- 10. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
- 11. A capacitor of value 0.1 μ F between Vdd and GND is required.

Ordering Information

CS00088AC-12-18E-66.666660T



Supported Frequencies^[12]

3.57 MHz	4 MHz	4.096 MHz	6 MHz	7.3728 MHz	8.192 MHz	10 MHz	12 MHz	14 MHz
18.432 MHz	19.2 MHz	20 MHz	24 MHz	24.576 MHz	25 MHz	25.000625 MHz	26 MHz	27 MHz
28.6363 MHz	30 MHz	31.25 MHz	32.768 MHz	33 MHz	33.3 MHz	33.33 MHz	33.333 MHz	33.3333 MHz
33.33333 MHz	37.5 MHz	38 MHz	38.4 MHz	40 MHz	40.5 MHz	48 MHz	50 MHz	54 MHz
60 MHz	62.5 MHz	65 MHz	66 MHz	66.6 MHz	66.66 MHz	66.666 MHz	66.6666 MHz	66.66666 MHz
72 MHz	74.175824 MHz	74.176 MHz	74.25 MHz	75 MHz	77.76 MHz			

Note:

12. Contact [SiTime](http://www.sitime.com) for frequencies that are not listed in the above table.

Ordering Codes for Supported Tape & Reel Packing Method^[13]

Device Size	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
2.0 x 1.6 mm	D	E	-	-	-	-
2.5 x 2.0 mm	D	E	-	-	-	-
3.2 x 2.5 mm	D	E	-	-	-	-
5.0 x 3.2 mm	-	-	T	Y	-	-
7.0 x 5.0 mm	-	-	-	-	T	Y

Note:

13. For "-", contact [SiTime](http://www.sitime.com) for availability.

Additional Information

Document	Description	Download Link
Time Machine II	MEMS oscillator programmer	http://www.sitime.com/support/time-machine-oscillator-programmer
Field Programmable Oscillators	Devices that can be programmable in the field by Time Machine II	http://www.sitime.com/products/field-programmable-oscillators
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	http://www.sitime.com/component/docman/doc_download/85-manufacturing-notes-for-sitime-oscillators
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Revision History

Version	Release Date	Change Summary
1.0	7/21/15	Final production release

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