CS00071AI-1D3-XXE133.330000

Standard Frequency Differential Oscillator

The Smart Timing Choice™

Features

- 31 standard frequencies from 25 MHz to 212.5 MHz
- LVPECL and LVDS output signaling types
- 0.6 ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- Frequency stability as low as ±20 PPM
- Industrial and extended commercial temperature ranges
- Industry-standard package: 7.0x5.0 mmxmm
- Programmable drive strength to reduce EMI
- For any other frequencies between 1 to 625 MHz, refer to SiT9121 and SiT9122 datasheet

Applications

- 10GB Ethernet, SONET, Synchronous Ethernet, SATA, SAS, Fibre Channel, PCI-Express
- Telecom, networking, broadband, instrumentation

EXPRESS SAMPLES | GREEN SOLUTIONS | QUARTZ FREE

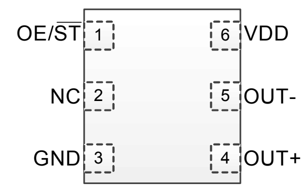
Electrical Characteristics

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVPECL AC Characteristics						
Output Frequency Range	f	25	133.330000	212.5	MHz	See page 7 for list of standard frequencies
Frequency Stability	F_stab	-20	–	+20	PPM	Inclusive of initial tolerance, operating temperature, rated power supply voltage, and load variations
		-25	–	+25	PPM	
		-50	–	+50	PPM	
First Year Aging	F_aging1	-2	–	+2	PPM	25°C
10-year Aging	F_aging10	-5	–	+5	PPM	25°C
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial
		-20	–	+70	°C	Extended Commercial
Start-up Time	T_start	–	6	10	ms	Measured from the time Vdd reaches its rated minimum value.
Resume Time	T_resume	–	6	10	ms	In Standby mode, measured from the time $\overline{ST}$ pin crosses 50% threshold.
Duty Cycle	DC	45	–	55	%	Contact SiTime for tighter duty cycle
LVPECL, DC and AC Characteristics						
Supply Voltage	Vdd	2.5	3.3	3.63	V	Termination schemes in Figure 1
Current Consumption	Idd	–	61	69	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	35	mA	OE = Low
Output Disable Leakage Current	I_leak	–	–	1	µA	OE = Low
Standby Current	I_std	–	–	100	µA	$\overline{ST}$ = Low, for all Vdds
Maximum Output Current	I_driver	–	–	30	mA	Maximum average current drawn from OUT+ or OUT-
Output High Voltage	VOH	0.55	–	2.4	V	See Figure 1
Output Low Voltage	VOL	0.25	–	2.2	V	See Figure 1
Output Differential Voltage Swing	V_Swing	400	575	800	V	See Figure 1
Rise/Fall Time	Tr, Tf	–	450	1000	ps	20% to 80%
OE Enable/Disable Time	T_oe	–	–	123	ns	
RMS Period Jitter	T_jitt	–	1.2	1.7	ps	f = 133 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.6	0.85	ps	f = 133 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds

Pin Description

Pin	Map	Functionality	
1	OE	Input	H or Open: specified frequency output L: output is high impedance
	$\overline{ST}$	Input	H or Open: specified frequency output L: Device goes to sleep mode. Supply current reduces to I_std.
2	NC	NA	Not Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage

Top View



Absolute Maximum

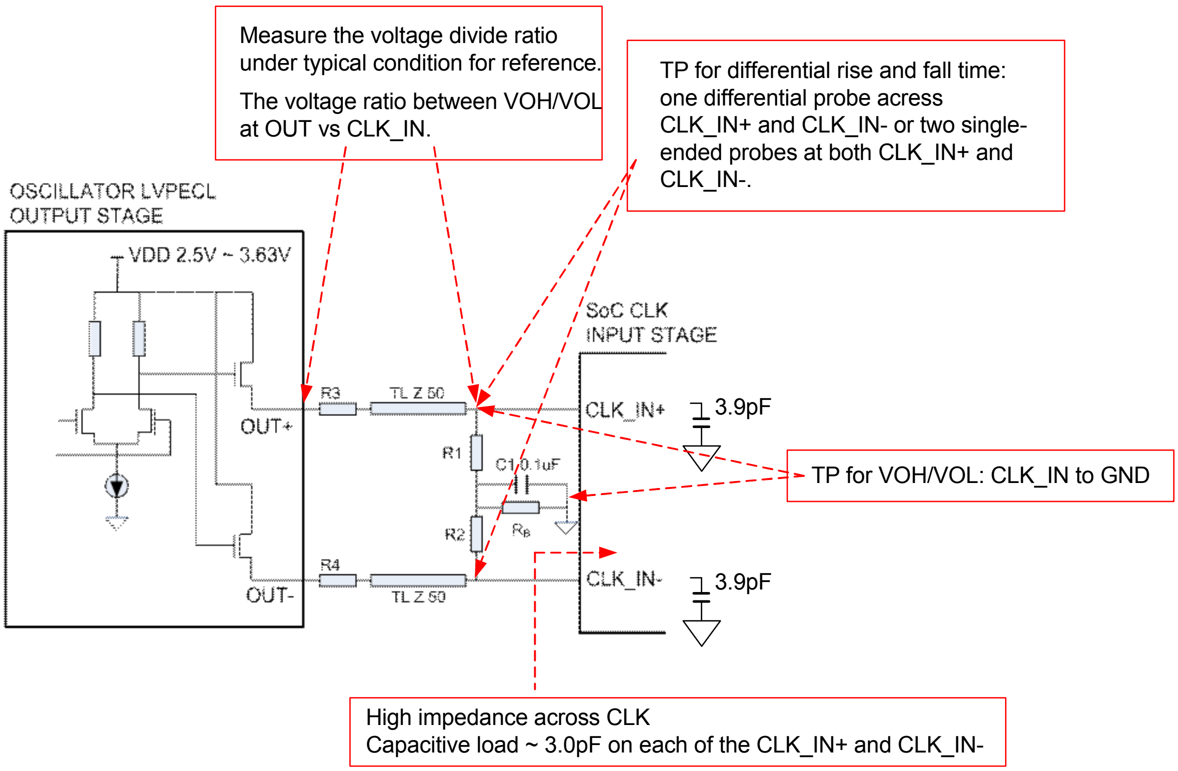
Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge (HBM)	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

Termination Diagram



* Customize termination circuit uses R1=R2=R3=R4=R_B=51 ohms with operating VDD from 2.5V to 3.63V.

Figure 1. Custom Termination Scheme and Test Points (TP)

Programmable Drive Strength

The CS00071 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the SiTime Applications Note section; http://www.sitime.com/support/application-notes.

EMI Reduction by Slowing Rise/Fall Time

Figure 2 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

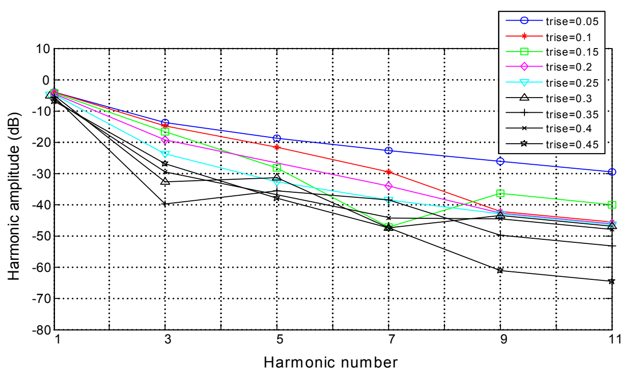


Figure 2. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to increase rise/fall time (edge rate) of the input clock. Some chipsets would require faster rise/fall time in order to reduce their sensitivity to this type of jitter. The CS00071 provides up to 3 additional high drive strength settings for very fast rise/fall time. Refer to the Rise/Fall Time Tables to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V CS00071 device with default drive strength setting, the typical rise/fall time is 1.15ns for 15 pF output load. The typical rise/fall time slows down to 2.72ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.41ns by then increasing the drive strength setting on the CS00071.

The CS00071 can support up to 60 pF or higher in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the Rise/Tall Time Tables to determine the proper drive strength for the desired combination of output load vs. rise/fall time

CS00071 Drive Strength Selection

Tables 1 through 5 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the CS00071 nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 1 through 4, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max Frequency} = \frac{1}{3.5 \times Trf\_10/90}$$

Where Trf_10/90 is the typical rise/fall time at 10% to 90% Vdd.

Example 1

Calculate f_{MAX} for the following condition:

- Vdd = 1.8V (Table 1)
- Capacitive Load: 30 pF
- Typical Tr/f time = 5 ns (rise/fall time part number code = G)

Part number for the above example:

CS00071AIT**G**2-33E-125.000000

Drive strength code is inserted here. Default setting is "-"

Rise/Fall Time (10% to 90%) vs C_{LOAD} Tables

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	12.45	17.68	19.48	46.21	57.82
A	6.50	10.27	16.21	23.92	30.73
R	4.38	7.05	11.61	16.17	20.83
B	3.27	5.30	8.89	12.18	15.75
S	2.62	4.25	7.20	9.81	12.65
D	2.19	3.52	6.00	8.31	10.59
T	1.76	3.01	5.14	7.10	9.15
E	1.59	2.59	4.49	6.25	7.98
U	1.49	2.28	3.96	5.55	7.15
F	1.22	2.10	3.57	5.00	6.46
W	1.07	1.88	3.23	4.50	5.87
G	1.01	1.64	2.95	4.12	5.40
X	0.96	1.50	2.74	3.80	4.98
K	0.92	1.41	2.56	3.52	4.64
Y	0.88	1.34	2.39	3.25	4.32
Q	0.86	1.29	2.24	3.04	4.06
Z or "-": Default	0.82	1.24	2.07	2.89	3.82
M	0.77	1.20	1.94	2.72	3.61
N	0.66	1.15	1.84	2.58	3.41
P	0.51	1.09	1.76	2.45	3.24

Table 1. Vdd = 1.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	8.68	13.59	18.36	32.70	42.06
A	4.42	7.18	11.93	16.60	21.38
R	2.93	4.78	8.15	11.19	14.59
B	2.21	3.57	6.19	8.55	11.04
S	1.67	2.87	4.94	6.85	8.80
D	1.50	2.33	4.11	5.68	7.33
T	1.06	2.04	3.50	4.84	6.26
E	0.98	1.69	3.03	4.20	5.51
U	0.93	1.48	2.69	3.73	4.92
F	0.90	1.37	2.44	3.34	4.42
W	0.87	1.29	2.21	3.04	4.02
G or "-": Default	0.67	1.20	2.00	2.79	3.69
X	0.44	1.10	1.86	2.56	3.43
K	0.38	0.99	1.76	2.37	3.18
Y	0.36	0.83	1.66	2.20	2.98
Q	0.34	0.71	1.58	2.07	2.80
Z	0.33	0.65	1.51	1.95	2.65
M	0.32	0.62	1.44	1.85	2.50
N	0.31	0.59	1.37	1.77	2.39
P	0.30	0.57	1.29	1.70	2.28

Table 2. Vdd = 2.5V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	7.93	12.69	17.94	30.10	38.89
A	4.06	6.66	11.04	15.31	19.80
R	2.68	4.40	7.53	10.29	13.37
B	2.00	3.25	5.66	7.84	10.11
S	1.59	2.57	4.54	6.27	8.07
D	1.19	2.14	3.76	5.21	6.72
T	1.00	1.79	3.20	4.43	5.77
E	0.94	1.51	2.78	3.84	5.06
U	0.90	1.38	2.48	3.40	4.50
F	0.87	1.29	2.21	3.03	4.05
W	0.62	1.19	1.99	2.76	3.68
G or "-": Default	0.41	1.08	1.84	2.52	3.36
X	0.37	0.96	1.72	2.33	3.15
K	0.35	0.78	1.63	2.15	2.92
Y	0.33	0.67	1.54	2.00	2.75
Q	0.32	0.63	1.46	1.89	2.57
Z	0.31	0.60	1.39	1.80	2.43
M	0.30	0.57	1.31	1.72	2.30
N	0.30	0.56	1.22	1.63	2.22
P	0.29	0.54	1.13	1.55	2.13

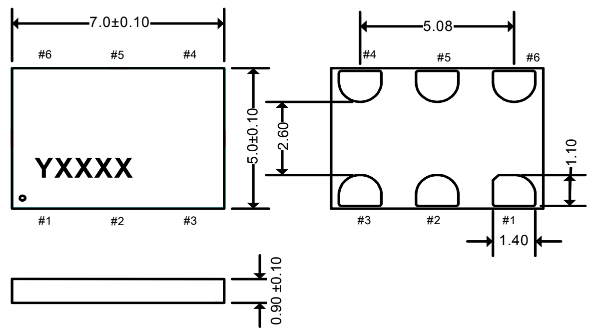
Table 3. Vdd = 2.8V Rise/Fall Times for Specific C_{LOAD}

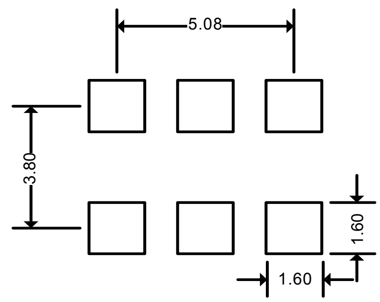
Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	7.18	11.59	17.24	27.57	35.57
A	3.61	6.02	10.19	13.98	18.10
R	2.31	3.95	6.88	9.42	12.24
B	1.65	2.92	5.12	7.10	9.17
S	1.43	2.26	4.09	5.66	7.34
D	1.01	1.91	3.38	4.69	6.14
T	0.94	1.51	2.86	3.97	5.25
E	0.90	1.36	2.50	3.46	4.58
U	0.86	1.25	2.21	3.03	4.07
F or "-": Default	0.48	1.15	1.95	2.72	3.65
W	0.38	1.04	1.77	2.47	3.31
G	0.36	0.87	1.66	2.23	3.03
X	0.34	0.70	1.56	2.04	2.80
K	0.33	0.63	1.48	1.89	2.61
Y	0.32	0.60	1.40	1.79	2.43
Q	0.32	0.58	1.31	1.69	2.28
Z	0.30	0.56	1.22	1.62	2.17
M	0.30	0.55	1.12	1.54	2.07
N	0.30	0.54	1.02	1.47	1.97
P	0.29	0.52	0.95	1.41	1.90

Table 4. Vdd = 3.3V Rise/Fall Times for Specific C_{LOAD}

Dimensions and Patterns

<table>
<tr><th>Package Size – Dimensions (Unit: mm)[1]</th><th>Recommended Land Pattern (Unit: mm)[2]</th></tr>
<tr><td>7.0 x 5.0x 0.90 mm



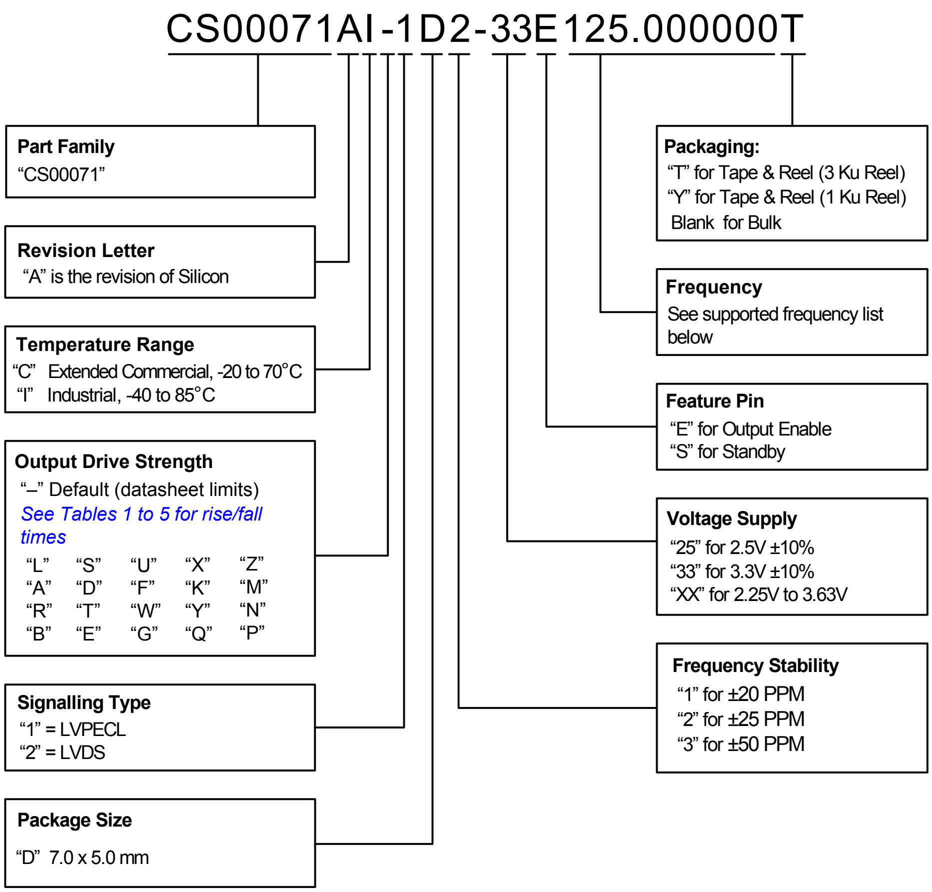
</td><td>


</td></tr>
</table>

Notes:

1. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
2. A capacitor of value 0.1 µF between Vdd and GND is recommended.

Ordering Information



Supported Frequencies

25.000000 MHz	50.000000 MHz	74.175824 MHz	74.250000 MHz	75.000000 MHz	98.304000 MHz	100.000000 MHz	106.250000 MHz
125.000000 MHz	133.000000 MHz	133.300000 MHz	133.330000 MHz	133.333000 MHz	133.333300 MHz	133.333330 MHz	133.333333 MHz
148.351648 MHz	148.500000 MHz	150.000000 MHz	155.520000 MHz	156.250000 MHz	161.132800 MHz	166.000000 MHz	166.600000 MHz
166.660000 MHz	166.666000 MHz	166.666600 MHz	166.666660 MHz	166.666666 MHz	200.000000 MHz	212.500000 MHz	