

# CS00064-2B2-33E100.000000

## Standard Frequency Differential Oscillator



### Features

- 100 MHz LVDS compatible output
- 0.6 ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- ±25 PPM Frequency stability

### Applications

- 10GB Ethernet, SONET, Synchronous Ethernet, SATA, SAS, Fibre Channel, PCI-Express
- Telecom, networking, broadband, instrumentation



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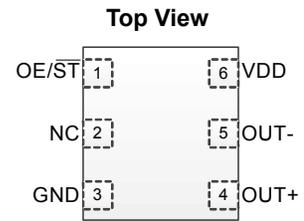
QUARTZ  
FREE

### Electrical Characteristics

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>LVDS, Common AC Characteristics</b>						
Output Frequency Range	f		100.000		MHz	
Frequency Stability	F_stab	-25	–	+25	PPM	Inclusive of initial tolerance, operating temperature, rated power supply voltage, and load variations
First Year Aging	F_aging1	-2	–	+2	PPM	25°C
10-year Aging	F_aging10	-5	–	+5	PPM	25°C
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial
Start-up Time	T_start	–	6	10	ms	Measured from the time Vdd reaches its rated minimum value.
Resume Time	T_resume	–	6	10	ms	In Standby mode, measured from the time ST pin crosses 50% threshold.
Duty Cycle	DC	45	–	55	%	Contact SiTime for tighter duty cycle
<b>LVDS, DC and AC Characteristics</b>						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
Current Consumption	Idd	–	47	55	mA	Excluding Load Termination Current
OE Disable Supply Current	I_OE	–	–	35	mA	OE = Low
Output Disable Leakage Current	I_leak	–	–	1	µA	OE = Low
Standby Current	I_std	–	–	100	µA	ST = Low, for all Vdds
Differential Output Voltage	VOD	200	350	500	mV	See Figure 1
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 1
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 1
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 1
Rise/Fall Time	Tr, Tf	–	495	600	ps	20% to 80%
OE Enable/Disable Time	T_oe	–	–	100+3	ns	T_oe = 100 ns + 3 period
RMS Period Jitter	T_jitt	–	1.2	1.7	ps	f = 100.00 MHz
RMS Phase Jitter (random)	T_phj	–	0.6	0.85	ps	f = 100.00 MHz, Integration bandwidth = 12 kHz to 20 MHz

### Pin Description

Pin	Map		Functionality
1	OE	Input	H or Open: specified frequency output L: output is high impedance
	$\overline{ST}$	Input	H or Open: specified frequency output L: Device goes to sleep mode. Supply current reduces to $I_{std}$ .
2	NC	NA	Not Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage



### Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
<b>Storage Temperature</b>	-65	150	°C
<b>VDD</b>	-0.5	4	V
<b>Electrostatic Discharge (HBM)</b>	–	2000	V
<b>Soldering Temperature (follow standard Pb free soldering guidelines)</b>	–	260	°C

### Environmental Compliance

Parameter	Condition/Test Method
<b>Mechanical Shock</b>	MIL-STD-883F, Method 2002
<b>Mechanical Vibration</b>	MIL-STD-883F, Method 2007
<b>Temperature Cycle</b>	JESD22, Method A104
<b>Solderability</b>	MIL-STD-883F, Method 2003
<b>Moisture Sensitivity Level</b>	MSL1 @ 260°C

Termination Diagram

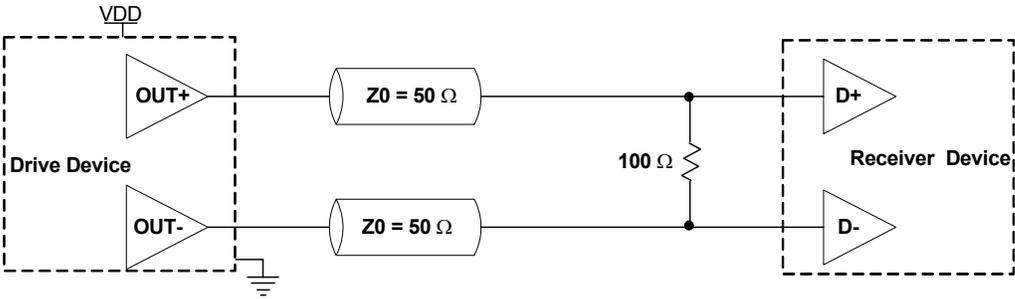
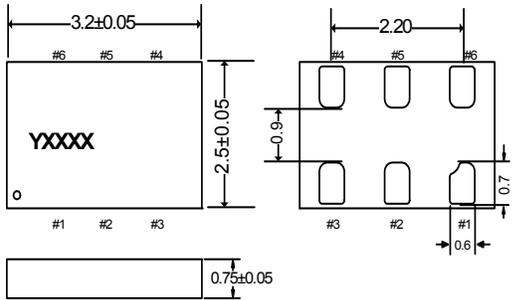
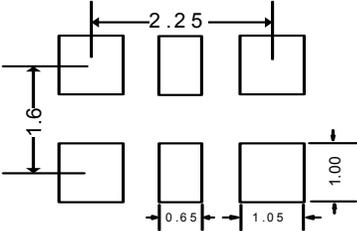


Figure 1. LVDS Single Termination (Load Terminated)

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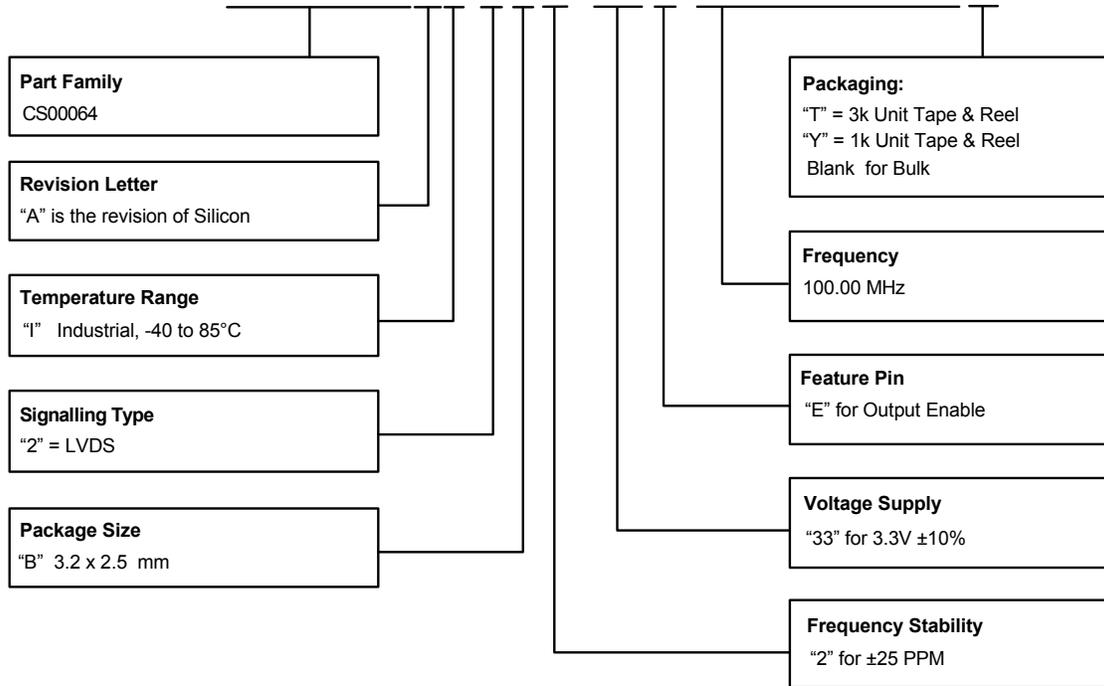
### Dimensions and Patterns

Package Size – Dimensions (Unit: mm) <sup>[1]</sup>	Recommended Land Pattern (Unit: mm) <sup>[2]</sup>
<p>3.2 x 2.5 x 0.75 mm</p> 	

1. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
2. A capacitor of value 0.1  $\mu$ F between Vdd and GND is recommended.

**Ordering Information**

**CS00064AI-2B2-33E100.000000T**



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