CS00052AC-C2-33NZ

Preliminary

Serially Programmable Oscillator with FS and DCXO

The Smart Timing Choice™

Features

- Selectable output frequency through serial pin, 45.1584 or 49.152 MHz
- Digitally controlled pull range of ±1600 PPM
- The DCXO function eliminates the need for an external DAC
- Superior pull range linearity of <= 0.1%
- LVCMOS/LVTTL compatible output
- industry-standard packages: 5.0 mm x 3.2 mm (6-pin)
- Outstanding silicon reliability of 2 FIT (10x improvement over quartz-based devices)

Applications

- Ideal for Audio applications

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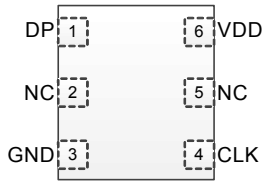
Electrical Characteristics

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	–	45.1584 49.152	–	MHz	Serially selectable output frequency between 45.1584 MHz and 49.152 MHz
Frequency Stability	F_stab	-25	–	+25	PPM	Inclusive of initial tolerance, operating temperature, rated power, supply voltage and load change
Aging	F_aging	–	–	±5	PPM	10 years
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
Supply Voltage	Vdd	2.97	3.3	3.63	V	
Pull Range	PR		±1600		PPM	See the last page for Absolute Pull Range, APR value
Linearity	Lin	–	–	0.1	%	
Frequency Change Polarity	–		Positive Slope		–	
Frequency Update Rate	F_update	–	–	25	KU / S	Frequency control mode 1, see table 1
		–	–	12.5	KU / S	Frequency control mode 2, see table 2
Current Consumption	Idd	–	31	–	mA	No load condition
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	–	1.0	2.2	ns	
Output Voltage High	VOH	90%	–	–	Vdd	OH = -7 mA, IOL = 7 mA
Output Voltage Low	VOL	–	–	10%	Vdd	
Output Load	Ld	–	–	15	pF	
Set-up Time	T_start	–	6	10	ms	Measured from the time Vdd reaches its rated minimum value
Input Low Voltage	VIL	–	–	0.2xVdd	V	
Input Middle Voltage	VIM	0.4xVdd	–	0.6xVdd	V	
Input High Voltage	VIH	0.8xVdd	–	–	V	
Input High or Low Pulse Width	T_logic	500	–	–	ns	
Input Middle Pulse Width	T_middle	500	–	–	ns	
Input Impedance	Zin	TBD	–	–	k?	
Input Capacitance	Cin	–	–	TBD	pF	20% to 80%
RMS Period Jitter	T_jitt	–	2	–	ps	
RMS Phase Jitter (random)	T_phj	–	0.6	–	ps	Integration bandwidth = 12 kHz to 20 MHz

Notes:
1. Absolute Pull Range (APR) is defined as the guaranteed pull range over temperature and voltage.
2. APR = pull range (PR) - frequency stability (F_stab) - Aging (F_aging)

Pin Description

Pin	Map	Functionality
1	Digital Programming Pin (DPpin)	See “Frequency Control Protocol Description” section
2	NC	No connect
3	GND	Vdd power supply ground
4	CLK	Oscillator output
5	NC	No connect
6	Vdd	Power supply voltage



Top View

Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	**MIL-STD-883F, Method 2002**
Mechanical Vibration	**MIL-STD-883F, Method 2007**
Temperature Cycle	**JESD22, Method A104**
Solderability	**MIL-STD-883F, Method 2003**
Moisture Sensitivity Level	**MSL1 @ 260°C**

Description

CS00052 device a serially programmable frequency select, digitally-controlled oscillator. User can set internal registers of the device through a 1-pin tri-level serial interface to switch frequency between two pre-set values in the device and pull the frequency dynamically around the selected one by ±1600ppm with resolution of up to 1 part-per-billion (ppb). Writing to the "FS" registers will initiate out put frequency switching by disabling the output for some time and enabling it once new frequency is switched. This allow glitch-free switching from one frequency to the other frequency. The FS frequencies are pre-programmed into the device at the production time and are not require to be related in any way.

The CDXO feature allows pulling the output frequency dynamically around the selected output frequency. This is achieved by writing to one or both of the DCXO register inside the device. Writing into the DCXO register does not cause any interruptions of output oscillations; the frequency will switch from one value to the new one smoothly, as shown in *Figure 4*.

Default Startup Condition

The CS00052 starts up at its factory programmed frequency and settings. The control register values are initialized all zeros, effectively setting the frequency to the middle of the control range. Also, the default start up frequency is 45.1584 MHz.

Frequency Control Protocol Description for DCXO Function (pulling the frequency)

The device includes two DCXO registers; writing to these registers controls the output frequency. Data for each register is written to the device using a data frame.

Data Frame Format

Each frame consists of 40 bits. A frame has 3 parts:

- The header, 16 bit

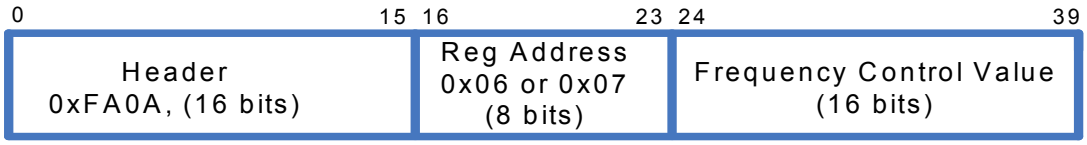
- Register address, 8 bit

- The data word (represented as 2's complement numbers), 16 bit.

Bits are sent MSB first.

Frames are sent LS word first in mode 2.

The header allows the devices to recognize that the master is initiating communication. The header includes the device address, which is factory programmable. The valid header is 0xFAIA, where "I" can be a hex digits from 0 to F. If not specified at the order time, it will be defaulted to zero. In this document in all examples and text, the device address is considered to be zero (default).



Frequency Control Mode 1

In this resolution mode, only one frame per frequency update is required, and the output frequency is updated at the end of each frame. The length of the frequency control data is 16 bits, and is written to the device as shown below:

Figure 1. Frequency Control Mode 1

Frequency Control Mode 2

In this mode, two frames per frequency update are required, and frequency is only updated at the end of the second frame. The frequency control value in this mode is 23 bits. This value is written to the device in two frames as follows:

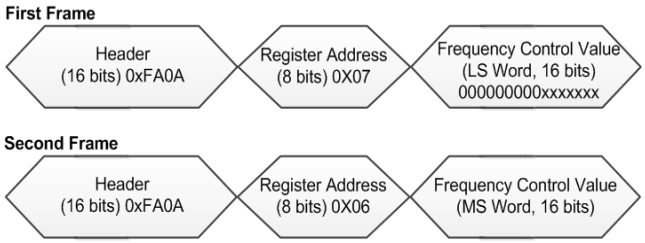


Figure 2. Frequency Control Mode 2

Resolution and Update Rate for Mode 1

Pull Range (PPM)	Step Resolution (ppb)	Max Update Rate (Updates Per Second)
±25	1	25 K
±50	1.5	25 K
±100	3	25 K
±200	6	25 K
±400	12	25 K
±800	25	25 K
±1600	49	25 K

Resolution and Update Rate for Mode 2

Pull Range (PPM)	Step Resolution (ppb)	Max Update Rate (Updates Per Second)
±25	1	12.5 K
±50	1	12.5 K
±100	1	12.5 K
±200	1	12.5 K
±400	1	12.5 K
±800	1	12.5 K
±1600	1	12.5 K

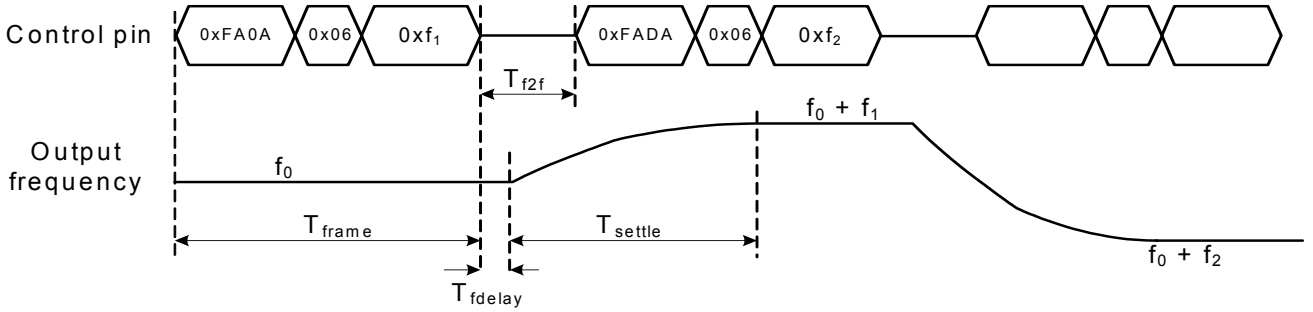


Figure 3. Mode 1 Frame Timing

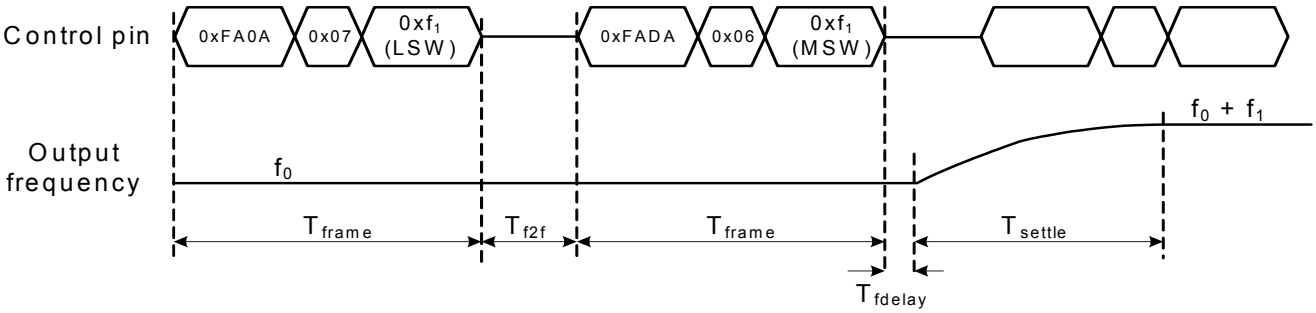


Figure 4. Mode 2 Frame Timing

Frame Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Frame Length	T_{frame}	40	—	µS
Frame to Frame Delay	T_{f2f}	2	—	µS
Frequency Settling Time	T_{settle}	—	30	µS
Frame to Frequency Delay	T_{fdelay}	—	8	µS

Calculating Pull Range PPM offset

The frequency control value must be encoded as a 2's complement number (16-bit in mode 1 and 23-bit in mode 2), representing the full scale range of the device. For example, for a ±1600ppm device in mode 2, the 23-bit number represents the full ±1600ppm range.

The upper 16 bits of the value are written to address 0x06. If the high-resolution register (address 0x07) is used, the other 7 bits are written to the lowest seven bits of address 0x07.

Here are the steps to calculate the frequency control value:

1. Find the scale factor (calculated for half of the pull range) from the tables below where PR is the Pull Range:

K (scale)Factor

Mode	K = Scale Factor
1	(2^15-1) / (PR*1.00135625)
2	(2^22-1) / (PR*1.00135625)

2. Enter the desired_PPM in equation below:
   Frequency control (decimal value) = round (desired_PPM * K).
3. For any frequency shifts (positive or negative PPM), convert the frequency control value to a 2's complement binary number.

Two examples follow:

Example 1

This example shows how to shift the frequency by +245.6 ppm in a device with ±1600 pull range using Mode 2 (23-bit):

Decimal value: round(245.6 * K) = 642954
23-bit value = 0x09CF8A

LS Word value = 0x000A (to be written to address 0x07)
MS Word value = 0x139F (to be written to address 0x06)
Write LS Word: 0xFA0A 07 000A (Frequency will not update)
Write MS Word: 0xFA0A 06 139F (Frequency updates after write)

Example 2

This example shows how to shift the frequency by -831.2 ppm in a device with ±1600 pull range using Mode 2 (23-bit):

Decimal value: round(abs(831.2 * K) = 2175989
23-bit abs binary value: 010000100110011111110101
23-bit 2's comp binary value: 1011110110011000 0001011
LS Word value = 0x 000B
MS Word value = 0x BD98
Write LS Word: 0xFA0A 07 000B (Frequency will not update)
Write MS Word: 0xFA0A 06 BD98 (Frequency updates after write)

Physical Interface

The SiTime DCMO uses a serial input interface to adjust the frequency control value. The interface uses a one-wire tri-level return-to-middle signaling format. *Figure 5* below shows the signal waveform of the interface.

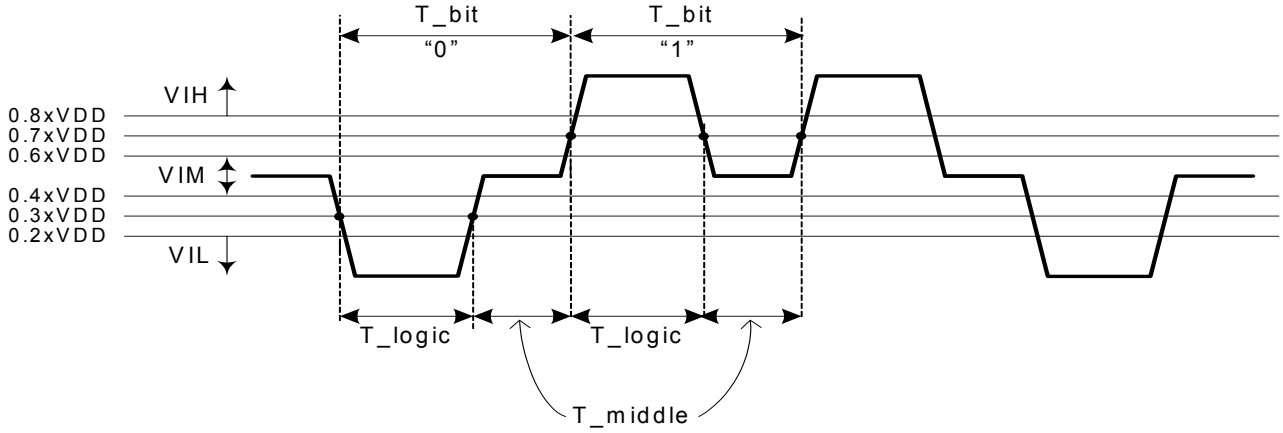


Figure 5. Serial 1-Wire Tri-Level Signaling

A logical bit "1" is defined by a high-logic followed by mid-logic. A logical bit "0" is defined by a low-logic followed by mid-logic. The voltage ranges and time durations corresponding to low-logic, high-, and mid-logic are illustrated in *Figure 5* and specified in electrical specification table.

The overall baud rate is computed as below:

$$baud\_rate = \frac{1}{T\_bit}$$

Figure 6 shows a simple circuit to generate tri-level circuit with a general purpose IO (GPIO) with tri-state capability. Most FPGAs and micro controllers/processors include such GPIOs. If the GPIO does not support tri-state output, two IO s may be used in combination with external tri-state buffer to generate the tri-level signal; an example of such buffer is the SN74LVC1G126. The waveform at the output of the tri-state buffer is shown in *Figure 7*. When the GPIO drives Low or High voltage, the rise/fall times are typically fast (sub-5ns range). When the output is set to Hi-Z, the output settles at middle voltage with a RC response. The time constant is determined based on the total capacitance on frequency control pin and the parallel resistance of the pull-up and pull-down resistors. The time constant in most practical situations will be less than 50ns; this necessitate choosing longer T_middle to allow the RC waveform to settle within 5% or so.

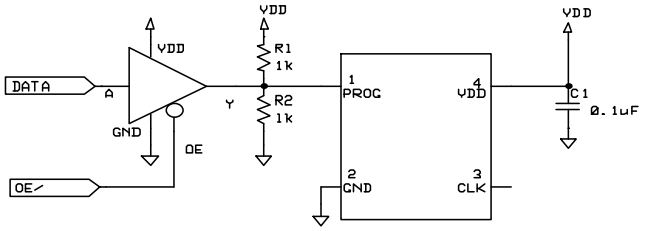


Figure 6. Circuit Diagram for Generating Tri-Level Signal with Tri-State Buffer

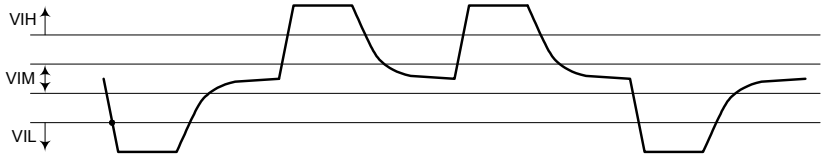


Figure 7. Tri-State Signal Generated with Tri-State Buffer

When using a tri-state buffer as shown above, care must be taken if the DATA and OE lines transition at the same time that there are no glitches. A glitch might occur, for example, if the OE line enables the output slightly before the data line has finished its logical transition. One way around this, albeit at the cost of some data overhead, is to use an extra OE cycle on every bit, as shown in *Figure 8*. Note that the diagram assumes an SN74LVC125, which has a low-true OE/ line (output is enabled when OE/ is low). For a high-true OE part, such as the SN74LVC126, the polarity of that signal would be reversed.

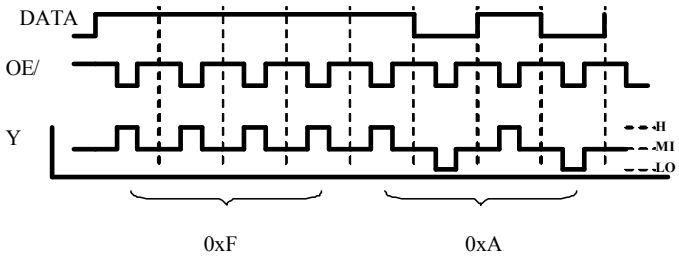


Figure 8. Signal Polarity

Frequency Select Operation

The CS00052 device allows switching the output from one frequency to another frequency by writing to the internal FS register of the device. Figure 9 shows the timing diagram of the frequency select operation. Switching frequency can be initiated by sending a data frame to the device. The frequency select frame (FS frame) includes three section:

- Header: The header is a 16 bit sequence in the form of 0xFAIA. "I" is a hexadecimal number form 0 to F that is the specific address of the device. A device address is "0" by default, but different address can be requested at the time of ordering. Connecting up to 16 devices with different address to the same control pin allow programming them with a single control pin.

- FS register address. This 8-bit number value is '0x08".

- FS register value: <Shouvik to provide format. We need a table that shows which address corresponds fro FS0 to FS8>

Upon completion of the frame, the internal FS register of the device is updated and the device initiates the operation of switching the output to a new frequency. The output clock continues for T_delay and then switches to Hi-Z state (no oscillation) for the duration of T_out_off. During this time, the device performs internal operations to switch the frequency. At the end of his period, the output clock with the new frequency appears. Note that a subsequent FS frequency switching can only be initiated T_FS_min time after the output Hi-Z state. The clock signal with new frequency is stable within rated stability from the first cycle.

Upon power-up, the frequency corresponding to FS0 will be outputted form the device.

The data frames are communicated to the device using a tri-level signaling scheme, as explained in section XXXX.

Once the FS frequency switching is complete, the new frequency can dynamically pulled with high resolution by writing into a different register in the device, as explained in section XXXX. This operation is referred to as "digitally-controlled oscillator (DCXO)" operation.

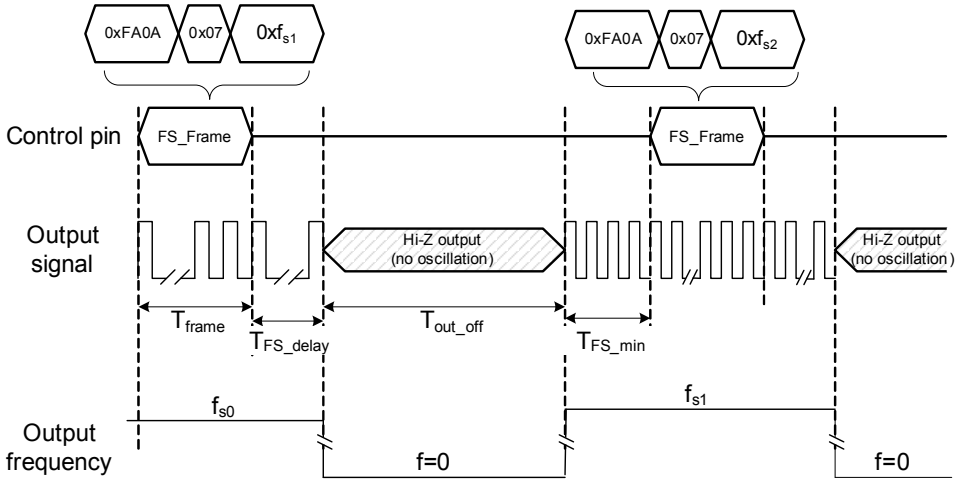


Figure 9. Frequency Select Timing Diagram

Shouvik: Please provide the following information

1. Max numbers for T_{FS_delay}, T_{FS_delay}, T_{out_off}, and T_{FS_min}. At this time, we just need numbers expected from design until full char is complete:

Parameter	Symbol	Min.	Max.	Unit
	T_frame	40	—	µS
	T_FS_delay	—	2	µS
	T_out_off	—	0.5	µS
	T_fs_min	—	0	µS

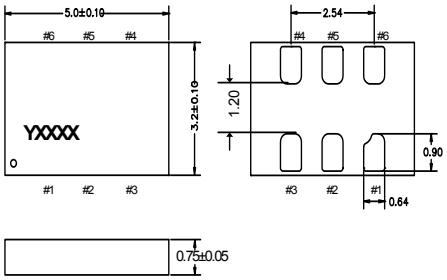
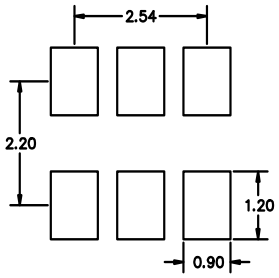
2. Check to ensure the header (0xFA0A) and FS register address (0x07) are correct:
   sm: DCXO is reg6 & 7, FS9_reg mode uses reg8[3:0]
3. What is the format for "fs1" value? Which bit in the register control the FS frequency?
   sm: See cutout from reg8[3:0] spec at the end.

Is there any inaccuracy or missing information in the above diagram? sm: looks ok

Register 8

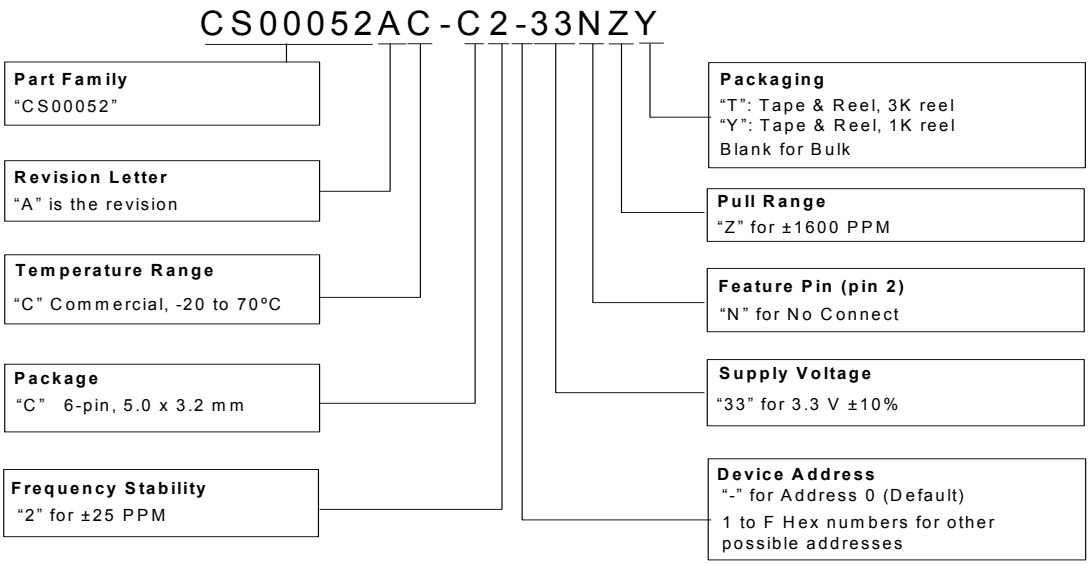
Reg0 [14]	Reg8 [3:2]	Reg8 [1:0]	NVM Registers Use
	00	00	45.1584 MHz (First Frequency)
	00	01	49.5 MHz (Second Frequency)

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[3]	Recommended Land Pattern (Unit: mm)[4]
5.0 x 3.2 x 0.75 mm 	

3. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
4. A capacitor of value 0.1 µF between Vdd and GND is recommended.

Ordering Information



APR Definition

Absolute pull range (APR) = Norminal pull range (PR) - frequency stability (F_stab) - Aging (F_aging)

APR

Nominal Pull Range	Frequency Stability
	APR (PPM)
± 1600	± 1570