### Precision Timing in V3Link

V3Link is a serializer/deserializer (SerDes) interface developed by Texas Instruments, commonly used for industrial applications. V3Link transmits high-definition video from cameras to image processing devices in applications such as factory automation, medical imaging, and security/surveillance.

Key Considerations

- Reliability
- Jitter performance
- EMI
- Small footprint

V3Link requires a single-ended LVCMOS clock, provided by an oscillator such as **SiT8208**. The clock frequency depends on various factors such as image resolution, frame rate, or V3Link clocking mode. Clock jitter must be well controlled. Excessive jitter on the clock "closes the eye diagram", resulting in increased bit error rate (BER) on the link.
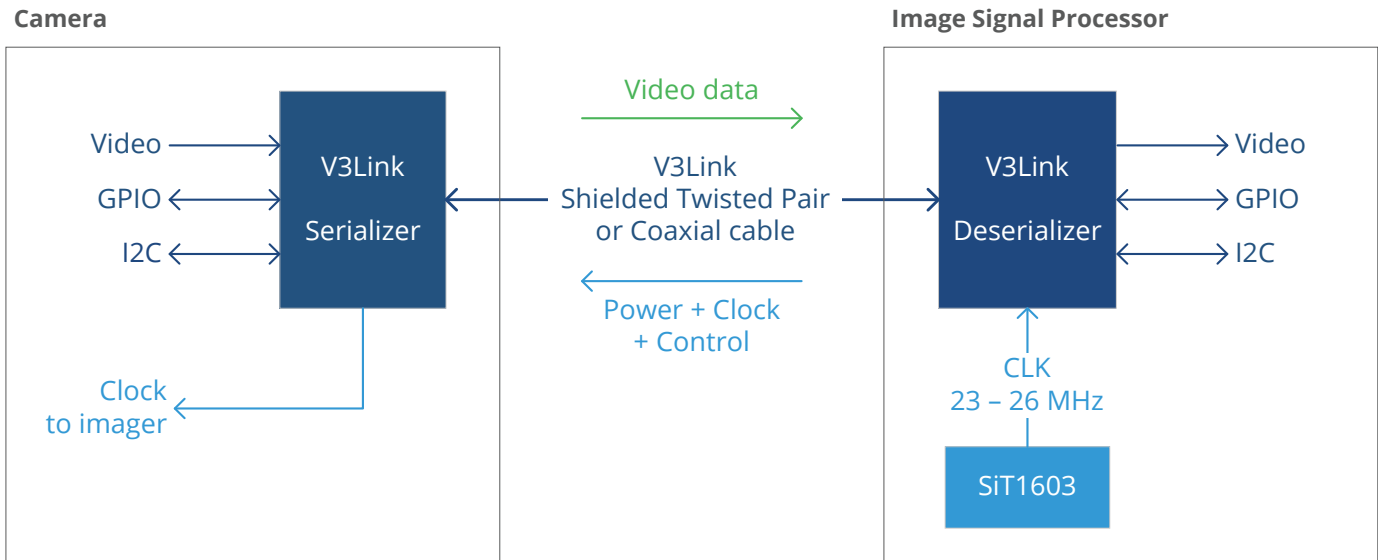
Asynchronous V3Link clocking
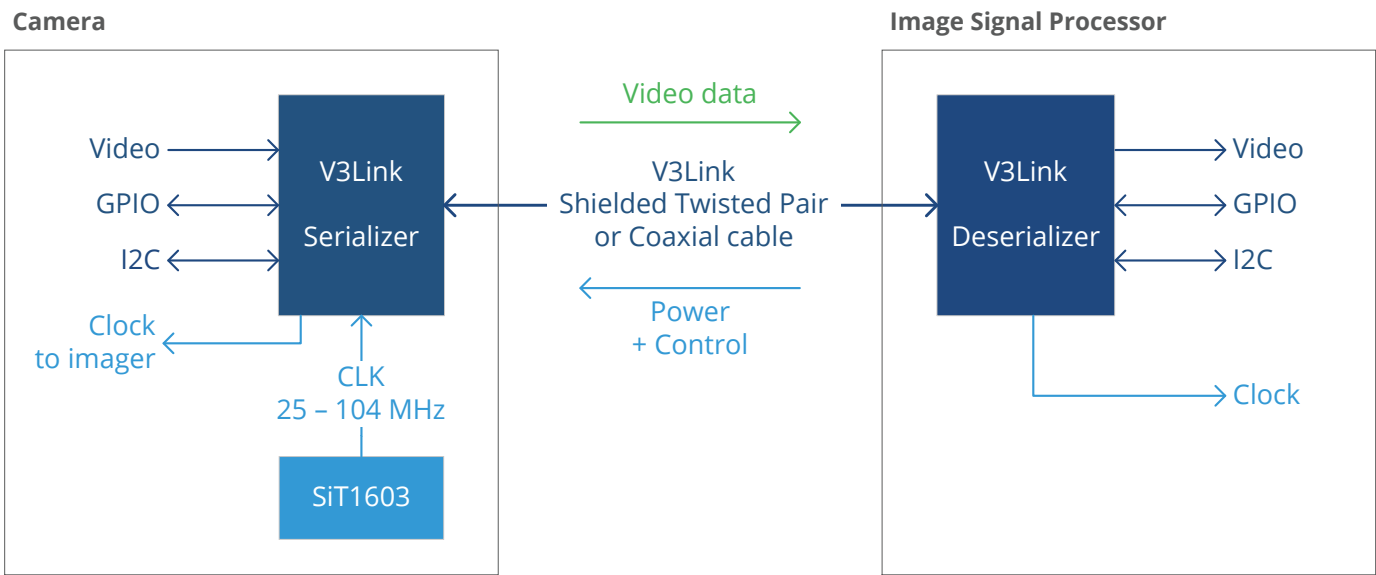
Figure 1. Asynchronous V3Link block diagram

Asynchronous mode represents the traditional way of driving serial data interfaces: both clock + data are provided at the input of the serializer. After transmission, both clock and data are recovered at the deserializer. Because multiple, independent links each run with its own independent clock, this mode is called asynchronous.

Synchronous V3Link clocking

In synchronous mode, the clock is provided from an oscillator to the deserializer side of the V3Link. The clock is then transmitted "uplink" through the V3Link backchannel to the serializer. This mode is called synchronous because the link runs synchronously to the deserializer and multiple links are therefore synchronized.

Figure 2. Synchronous V3Link block diagram

Synchronizing multiple V3Link with a SiTime clock generator

When multiple cameras are synchronized, their frames are aligned. This reduces the need for a RAM buffer on the image signal processor side, otherwise needed to re-align mismatched video frames. Having all clocks at the same frequency and phase is a prerequisite for synchronizing multiple links.

Up to four cameras can be connected to a V3Link deserializer. When more cameras are needed in a system, a SiTime clock generator can be used to synchronize all clocks toward multiple deserializers. Clock generators can also provide other clocks in a system (such as PCI-Express, Ethernet, etc.), offering all advantages of integration.

SiTime Advantages

SiTime devices offer the following advantages over quartz crystals:

• Up to 50x better reliability.

• Up to 100x better resilience to shock, vibration and electromagnetic interference, due to the smaller size (0.4 x 0.4 mm) and lower mass of MEMS resonators compared to crystals.

• EMI reduction features including drive strength selection and spread spectrum clocking (select devices).

• Small footprint, enabled by the small size of the MEMS resonator.

• Factory-programmed devices from standard parts enable short lead time and security of supply

• Reliable semiconductor supply chain

Featured Products

Type	Product	Frequency	Key Features	Key Values
MHz Oscillator	SiT8208A-G3-001	27 MHz	• -40°C to +85°C • ±20 ppm stability • Standard package sizes • Low jitter	• High reliability • Flexible frequency options • Excellent stability over temperature • Featured on V3Link Reference Designs: TSER4905 TSER953 TSER954 TSER960
	SiT8208	1 to 80 MHz		
	SiT1602	52 std freqs from 3.57 to 77.76 MHz		
	SiT8021	1 to 26 MHz	• -40°C to +85°C • ±50 ppm stability • 1.5 x 0.8 CSP package	• High reliability • Small footprint
	SiT1603[2]	8 to 76.8 MHz (various specific frequencies)	• -40°C to +85°C • ±25 ppm stability • 2 mA current consumption • 0.75 fs RMS phase jitter • 1612, 2016, 2520, 3225 packages	• High reliability • Low power • Various standard package options
Clock Generator	SiT9121x family[2]	1 to 750 MHz	• 4 and 8 output options • ±20 ppm stability • LVPECL, LVDS, HCSL, Low-power HCSL, FlexSwing™ • < 200 fs RMS jitter[1] • Spread spectrum • -40°C to +105°C • 4x4, 5x5 and 6x6 mm packages	• High reliability • Simplifies clock tree design with multiple low jitter clocks • Programmable clocks add flexibility to complex clocking architectures • Integrated solution generates all clocks for multiple V3Link as well as more clocks in the system: PCI-Express, Ethernet, SoC clocks, etc. • No external resonator needed • Small PCB footprint, compact layout

[1] 12 kHz to 20 MHz integration range
[2] Contact SiTime for availability

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Version 1.0 – June 2023