

Precision Timing in FPD-Link

FPD-Link is a serializer/deserializer (SerDes) interface developed by Texas Instruments and is now commonly used for infotainment and ADAS applications. FPD-Link transmits high-definition video from cameras to ADAS computers, as well as from Infotainment systems to LCD displays. It features advanced techniques to enable long cables in harsh EMI environments.

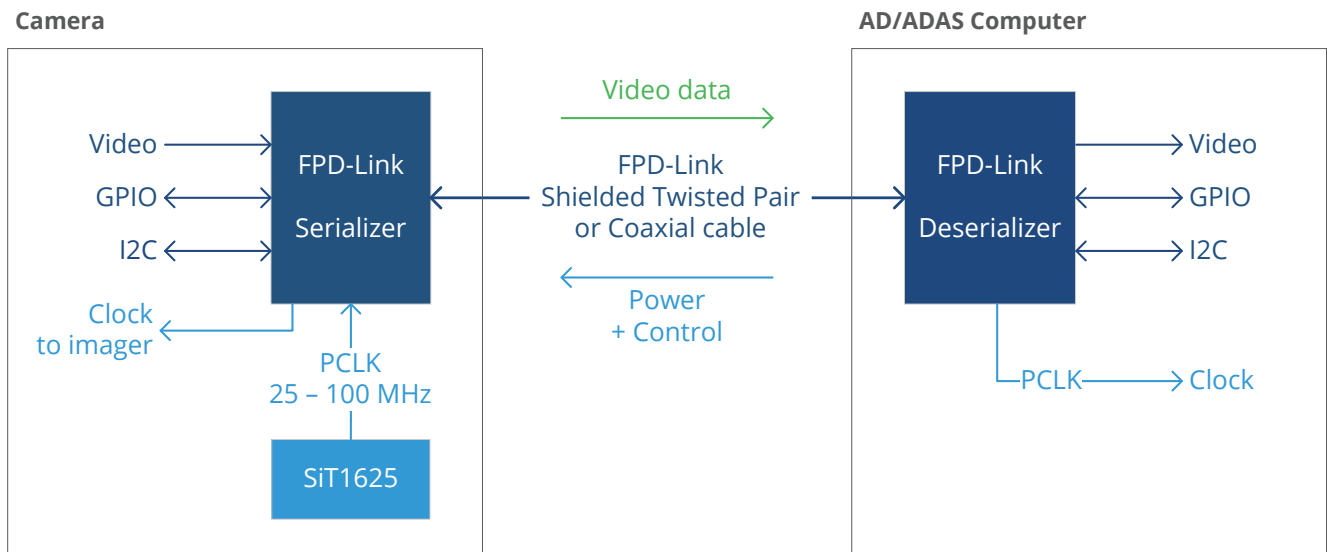
Key Considerations

- Reliability
- Jitter performance
- EMI
- Small footprint

FPD-Link requires a single-ended LVCMOS clock (called "PCLK") between 25 MHz and 100 MHz, provided by an oscillator such as **SiT1625**. Clock jitter must be well controlled. Excessive jitter on the clock "closes the eye diagram", resulting in increased bit error rate (BER) on the link.

For more details, please refer to the [White Paper on FPD-Link Clocking](#).

Asynchronous FPD-Link clocking



SiTime

Figure 1. Asynchronous FPD-Link block diagram

Asynchronous mode represents the traditional way of driving serial data interfaces: both clock + data are provided at the input of the serializer. After transmission, both clock and data are recovered at the deserializer. Because multiple, independent links each run with its own independent clock, this mode is called asynchronous.

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Synchronous FPD-Link clocking

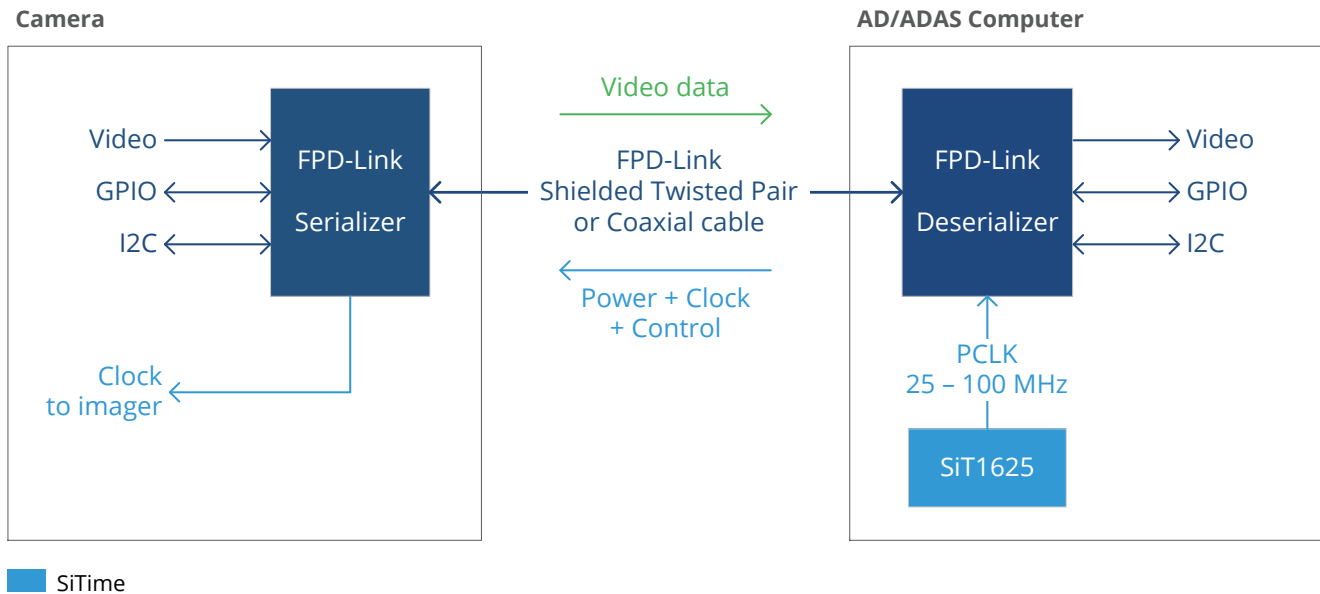


Figure 2. Synchronous FPD-Link block diagram

In synchronous mode, the clock is provided from an oscillator to the deserializer side of the FPD-Link. The clock is then transmitted "uplink" through the FPD-Link backchannel to the serializer. This mode is called synchronous because the link runs synchronously to the deserializer and multiple links are therefore synchronized. However, an extra step is required to synchronize multiple links: all deserializers clocks must have the same frequency and phase. A clock generator is the best device to achieve this, as described in the next section.

Synchronizing multiple FPD-Links with a SiTime clock generator

When multiple cameras (e.g., front left, front center, and front right of a vehicle) are synchronized, their frames are aligned. This reduces the need for a RAM buffer on the ADAS computer side, otherwise needed to re-align mismatched video frames.

Having all clocks at the same frequency and phase is a prerequisite for synchronizing multiple links. This is best achieved with a clock generator – see Fig. 3. SiTime automotive clock generators feature an integrated, high-reliability MEMS resonator. Multiple configurable output frequencies enable FPD-Links with different frequencies. The typical use case is multiple cameras having different resolutions. Advanced features for ADAS applications are available too. Please [contact SiTime](#) for information on the detailed feature set and product availability.

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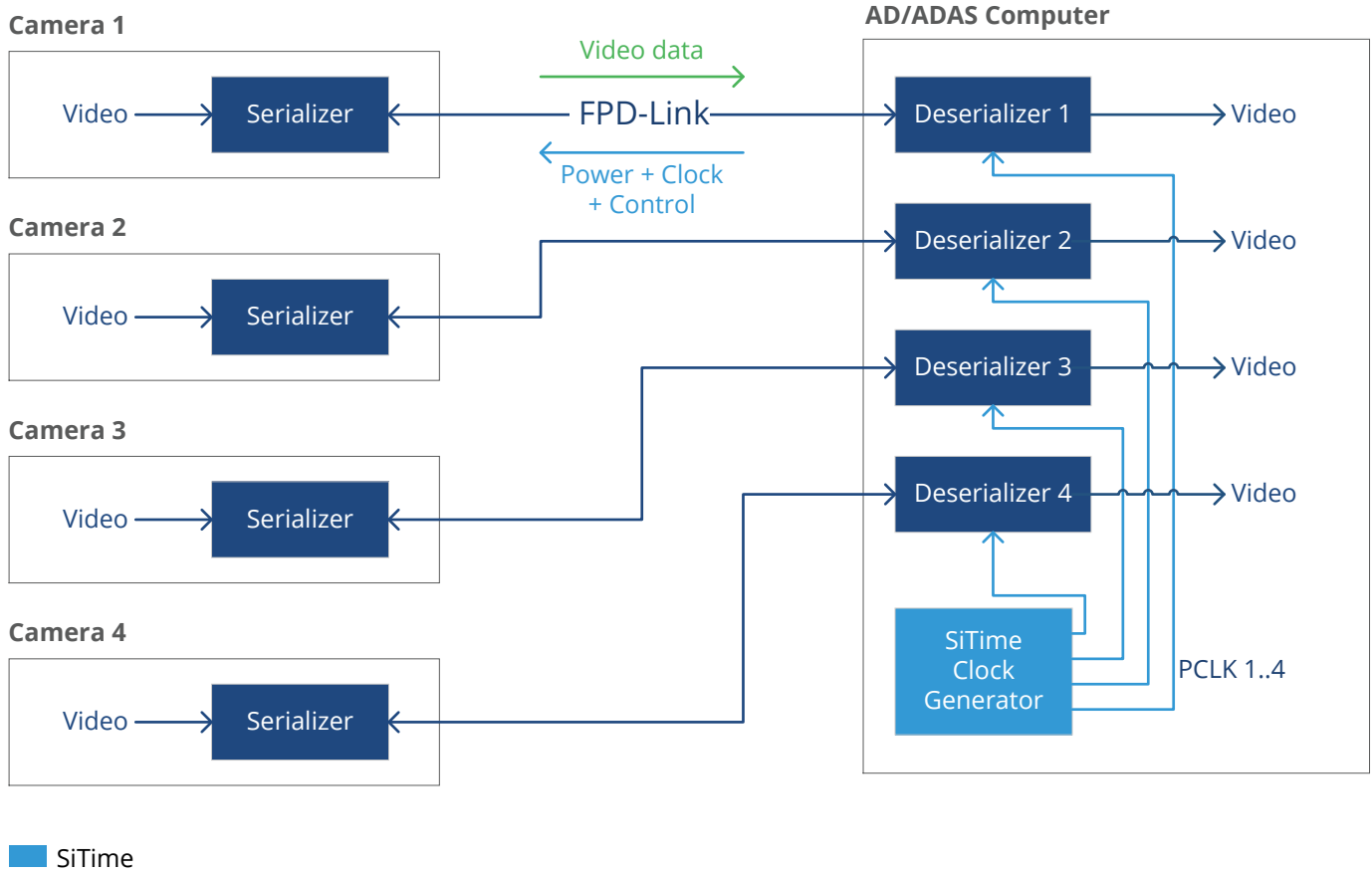


Figure 3. Multiple synchronous FPD-Links

SiTime Advantages

All SiTime devices offer the following advantages over quartz crystals, which are particularly important for automotive applications.

- Up to 50x better reliability. Apart from reducing the amount of field failures, better reliability translates to a lower FIT rate. This provides better hardware safety metrics in an FMEDA, the quantitative analysis required as part of a functional safety assessment.
- Up to 100x better resilience to shock, vibration and electromagnetic interference, due to the smaller size (0.4 x 0.4 mm) and lower mass of MEMS resonators compared to crystals.
- EMI reduction features including drive strength selection and spread spectrum clocking (select devices).

Featured products – please refer to the [Selector Guide](#) for more options

Type	Product	Frequency	Key Features	Key Values
Low Power Oscillator	SiT1625	<p>44 standard frequencies</p> <p>incl. 25 MHz (SiT1625A) for FPD-Link IV ADAS</p> <p>and 27 MHz (SiT1625C) for FPD-Link IV Infotainment</p>	<ul style="list-style-type: none"> -40°C to +125°C ±25, ±30, ±50 ppm stability 1612, 2016, 2520, 3225 packages 500 fs RMS jitter¹ 2.3 mA typ. current consumption 	<ul style="list-style-type: none"> High reliability Extended temperature range EMI reduction features Small footprint Low power Low jitter enables highest speed links
Clock Generator	SiT9128x family	1 to 1000 MHz	<ul style="list-style-type: none"> 4 configurable output pairs: 4 differential pairs or 8 single-ended outputs ±30, ±50 ppm stability LVPECL, LVDS, HCSL, Low-power HCSL, FlexSwing™ < 200 fs RMS jitter¹ Spread spectrum -40°C to +125°C 4x4 mm package 	<ul style="list-style-type: none"> High reliability Integration: generates all clocks for multiple FPD-Links as well as more clocks in the system: PCI-Express, Ethernet, SoC clocks, etc. No external resonator needed Advanced features for AD/ADAS applications Please contact SiTime for information on advanced features and product availability

¹ 12 kHz to 20 MHz integration range



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