Building Clock Trees in SiTime Cascade GUI Software

Application Note

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1 Introduction

The clock network generated and distributed within a digital system is usually called a *clock tree*. It may comprise such clocking device types as clock oscillators, clock buffers, clock generators, jitter cleaners and network synchronizers, as noted from clock source to destination. The number of clock tree components and outputs depends on the digital system's complexity. A clock tree can have several ICs with different clock performance depending on the application. A simple clock tree example is shown in Figure 1.

This document applies to the Cascade SiT9514x products which SiTime recommends using for building clock trees.

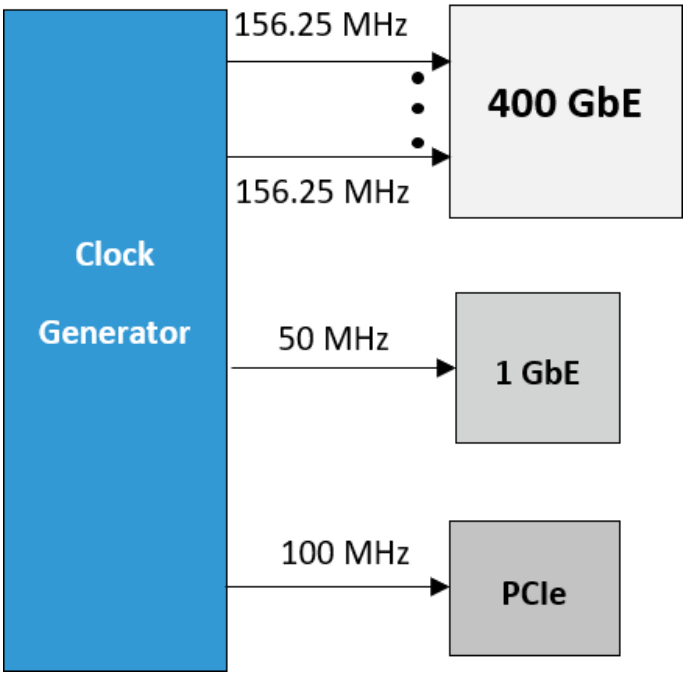

Figure 1: Clock tree example

2 SiTime clock tree components

SiTime offers the following components for clock tree design:

- Temperature compensated oscillators (TCXOs)
- Voltage-controlled temperature compensated oscillators (VCTCXOs)
- Oven-controlled oscillators (OCXOs)
- Ultra-low jitter differential oscillators
- Clock generators
- Clock jitter attenuators (jitter cleaner)
- Network synchronizers

3 SiTime Cascade MEMS clock generators, jitter cleaners, and network synchronizers – short descriptions of general functional features

SiTime MEMS Clock Generator – a single-chip IC that uses an integrated MEMS resonator as a reference frequency source for generating multiple output clocks at one or multiple frequencies.

SiTime MEMS Clock Jitter Attenuator (Jitter Cleaner) – a single-chip IC that uses an integrated MEMS resonator as a reference frequency source for generating multiple output clocks at one or multiple frequencies to improve jitter performance for incoming clock signals and consequently minimizing phase jitter in the end application. These ICs are also called jitter cleaners.

SiTime MEMS Network Synchronizer – a single-chip IC that uses an integrated MEMS resonator as a reference frequency source for generating multiple output clocks at one or multiple frequencies to improve jitter performances for incoming clock signals and consequently minimizing phase jitter, and featuring 4 independent clock domains for SyncE and IEEE1588 applications.

Table 1 summarizes the clock device features which helps in making the right component choice when building clock trees.

Table 1: Comparison of functional features

Function	Clock Generator	Clock Jitter Attenuator	Network Synchronizer
Free-run operation	Yes	Yes	Yes
Synchronous operation	Yes	Yes	Yes
Zero delay mode	Yes	Yes	Yes
Holdover operation	No	Yes	Yes
Jitter cleaning	No	Yes	Yes
Prog loop bandwidth	No	Yes	Yes
Hitless switching	No	Yes	Yes
Low wander mode	No	No	Yes

3.1 Free-run operation

Free-running mode is the mode of operation before the loop is locked to the selected input clock or the mode of operation for the case when none of the input clocks are available. Examples of applications are processors, memory controllers, and peripheral components.

3.2 Synchronous operation

Synchronous mode is the mode of operation where the output clock is locked to the input clock. This mode is used in applications which require continuous communication and network-level synchronization. In synchronized mode, the internal PLL is able to lock to a *gapped input* clock with some edges missing, producing a smooth output clock without any gaps, and with the requested frequency translation from input to output. Examples of such applications are synchronous Ethernet, IEEE 1588, optical transport networking (OTN), and mobile backhaul. These applications require transmitters and receivers operating at the same frequency.

3.3 Holdover operation

Holdover mode of functionality is entered when the input clock is lost. The PLL locks to the highest priority spare clock available and if all specified input clocks are lost, the PLL enters *holdover* mode by applying the correction based on the historical average of the input clock. This mode applies to clock jitter attenuators and network synchronizers.

3.4 Zero delay mode

Zero delay clock mode is the mode of operation when the outputs are edge-aligned with the clock input. This mode applies to clock generators, clock jitter attenuators, and network synchronizers.

3.5 Jitter optimization recommendations for clock tree design

It is important to evaluate clock tree devices' jitter performance. Clock jitter performance varies across a wide range of conditions, including device configuration, operating frequency, signal format, input clock slew rate, and power supply noise, etc. Some ways of achieving the optimal jitter performance using the Cascade GUI for device configuration are described below.

3.5.1 Cascade GUI guideline for optimal jitter performance

SiTime's Cascade Software GUI supports *frequency planning*. This is a process of internally configuring network synchronizers, clock generators, or clock jitter attenuators to create a configuration that implements the required number of inputs and outputs with predefined input and output frequencies.

3.5.1.1 Output placement and frequency planning

The output placement in the frequency plan should be implemented in a way that ensures outputs having frequency difference in the range from 12 kHz to 20 MHz are not placed next to each other and are spaced as far apart as possible to minimize output-to-output coupling, resulting in in-band spurs. An example of a poor frequency plan with sub-optimal output placement is shown in Figure 2 (where O3 and O2 placed next to each other). Figure 3 shows an example with proper output placement in a frequency plan (where the 156.25 MHz and 175 MHz outputs are placed far apart from each other).

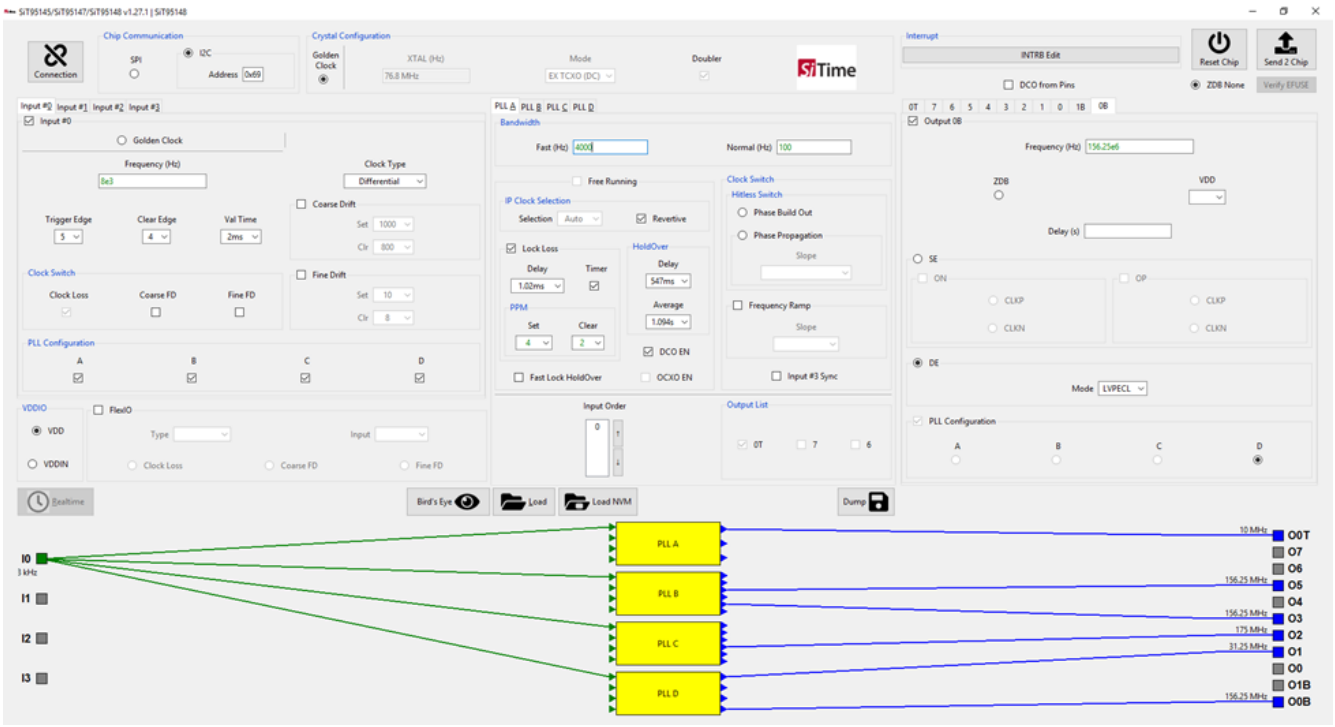

Figure 2: Cascade GUI example of sub-optimal output placement

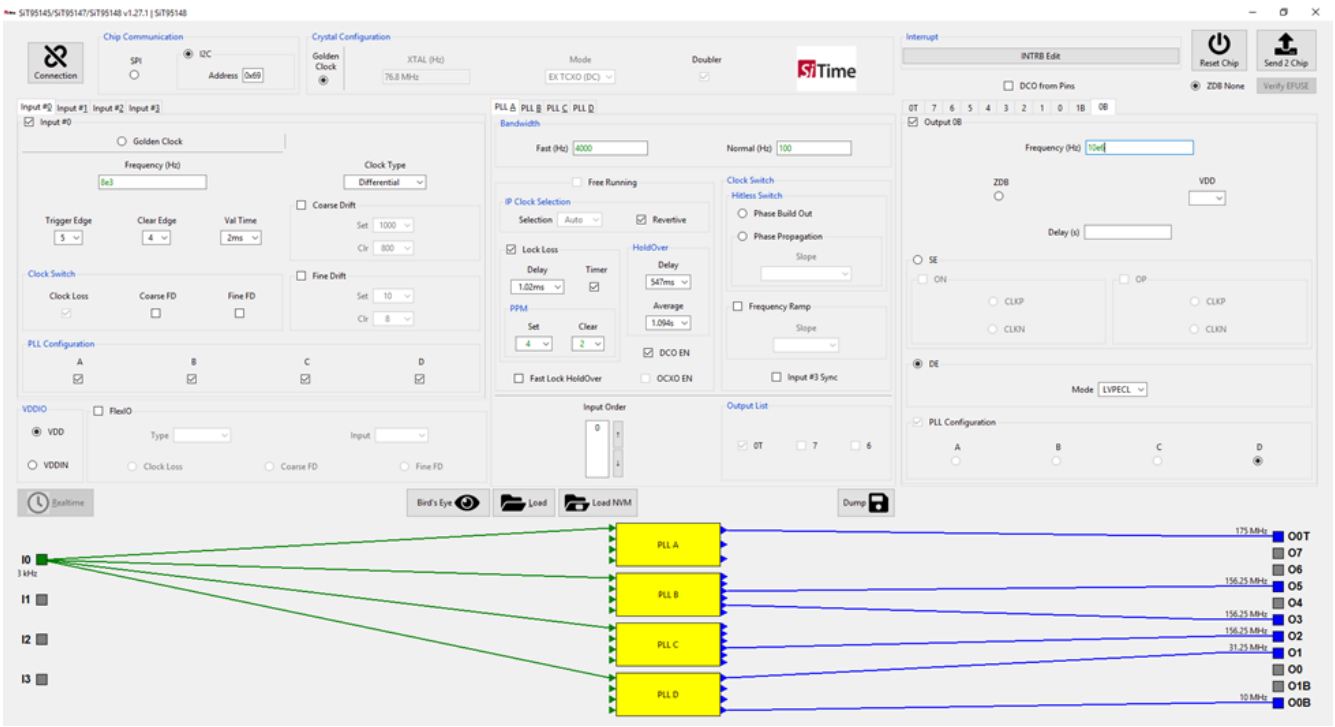

Figure 3: Cascade GUI example of optimal output placement

To minimize phase noise spurs caused by crosstalk from placement of LVCMOS outputs, a frequency plan should be done in a way that avoids up to 3rd-harmonic of the adjacent LVCMOS outputs, to land within the integration frequency band of the jitter sensitive output frequency, as shown in Figure 4.

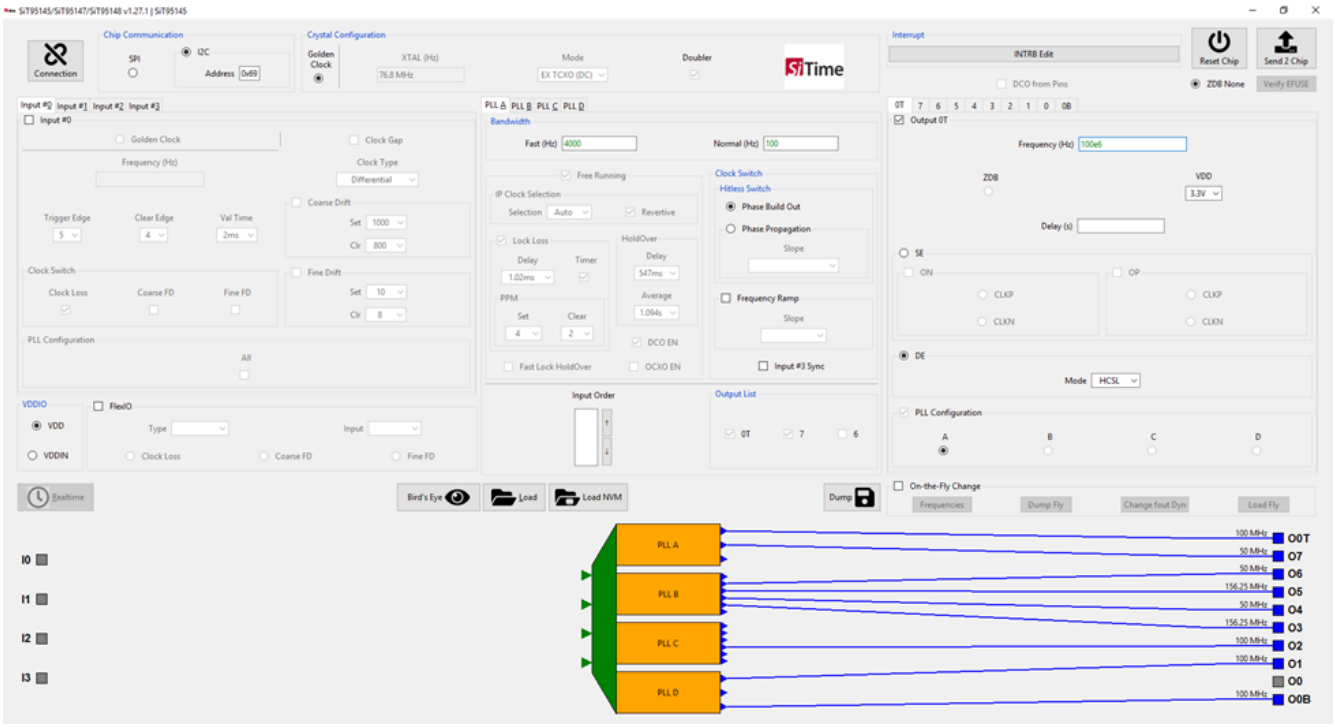

Figure 4: Cascade GUI example of crosstalk minimizing output placement

The frequency value of the LVCMOS output O6 is 50 MHz. The frequency value of the LVCMOS output O5 is 156.25 MHz. So the third harmonic of this frequency is 150 MHz. The difference is 6.25 MHz that is within the integration band (12 kHz to 20MHz) for the phase jitter calculation. The same principle applies to LVCMOS outputs O4 and O3.

3.5.1.2 Single-ended CMOS output type selection

To minimize coupling of single-ended CMOS outputs to differential outputs, it is recommended to select complimentary outputs of the single-ended CMOS outputs in the Cascade GUI, as shown in Figure 5. Output type selection should be OP and ON, with OP=CLKP and ON=CLKN.

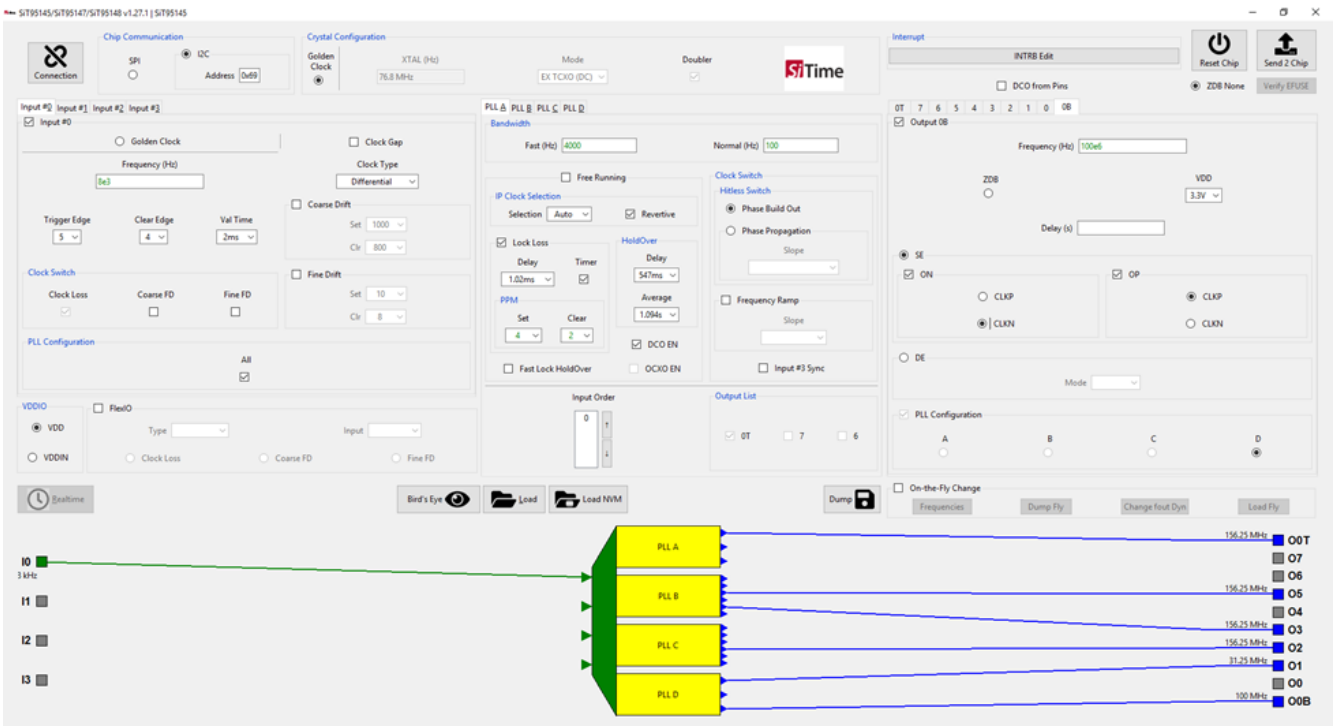

Figure 5: Cascade GUI example of single-ended CMOS output type selection

4 SiTime's Cascade CSoC product line

SiTime Cascade clock-system-on-a-chip includes 5 products with different features for different applications and shown in the following table.

Table 2: SiTime Cascade products

Category	Part Number	Inputs	Ouputs	Timing Domains
Clock Generator	SiT95141	4	10	1
Jitter Attenuator	SiT95145	4	10	1
Network Synchronizer	SiT95147	4	8	4
	SiT95148	4	11	4

5 SiTime Cascade GUI clock tree examples and implementation

Clock tree architecture examples for the SiT96141 clock generator, SiT96145 jitter cleaner, and SiT96147 network synchronizer are shown in the following sections.

5.1 4K-to-8K encoder with secure reliable transport (SRT) protocol clock tree

The following figure shows an application example of the 4K-to-8K encoder with a clock generator clock tree.

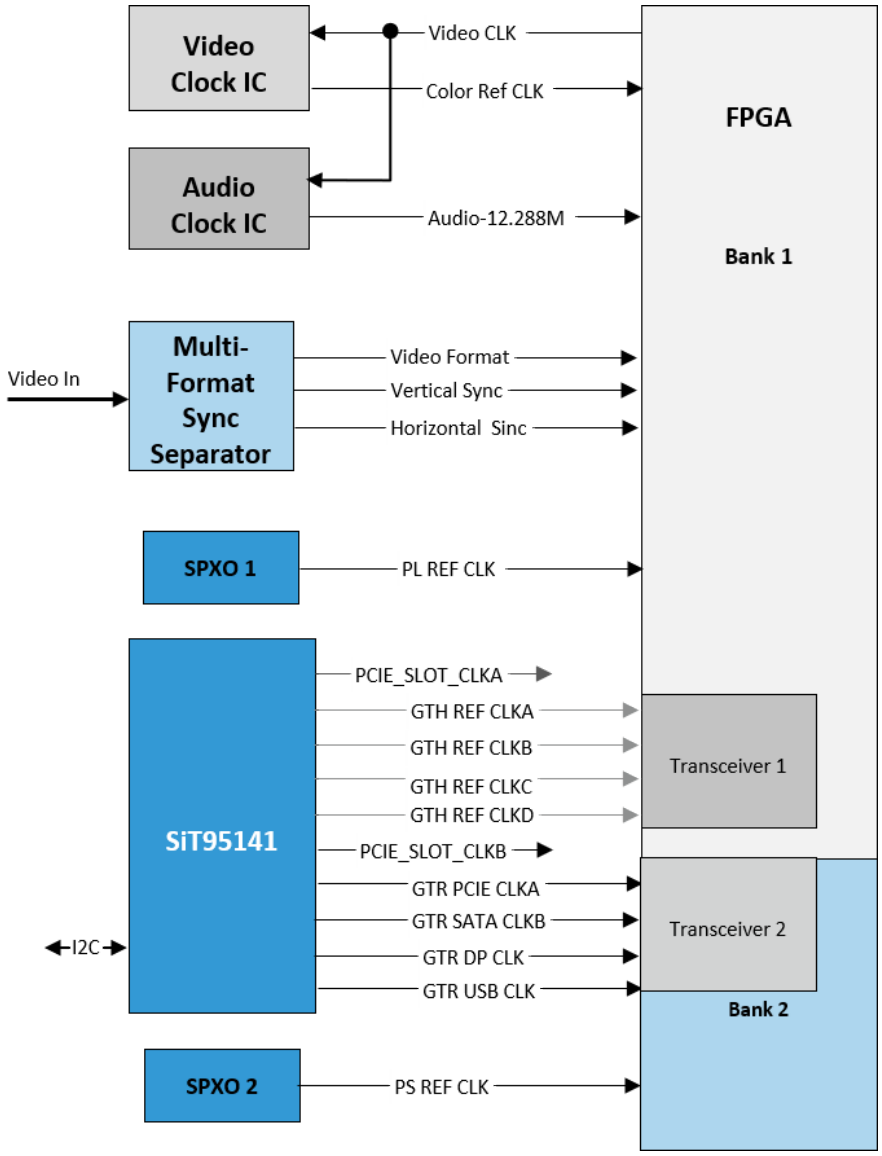

Figure 6: 4K-to-8K encoder clock tree

The following table lists all frequency values for the 4K-to-8K encoder.

Table 3: 4K to 8K encoder frequencies list

Clock Name	Clock Frequency Value, MHz	Comments
Video CLK	27/74.25/74.176	
Color Ref CLK	27	
Audio-12.288M	12.288	
PL REF CLK	27	
PCIE SLOT CLKA	100	PCIE
GTH REF CLKA	148.35/148.5/297	12G SDI
GTH REF CLKB	148.35/148.5/297	HDMI
GTH REF CLKC	100	PCIE
GTH REF CLKD	148.35/148.5/297	
PCIE SLOT CLKB	100	PCIE
GTR PCIE CLKA	100	PCIE
GTR SATA CLKB	125	SATA 6Gb
GTR DP CLK	27	
GTR USB CLK	26	USB 3.0
PS REF CLK	33.33	

In this application, the SiTime SiT95141 is used as a multi-frequency clock generator.

The frequency plan is implemented in the Cascade GUI as shown in the following figure.

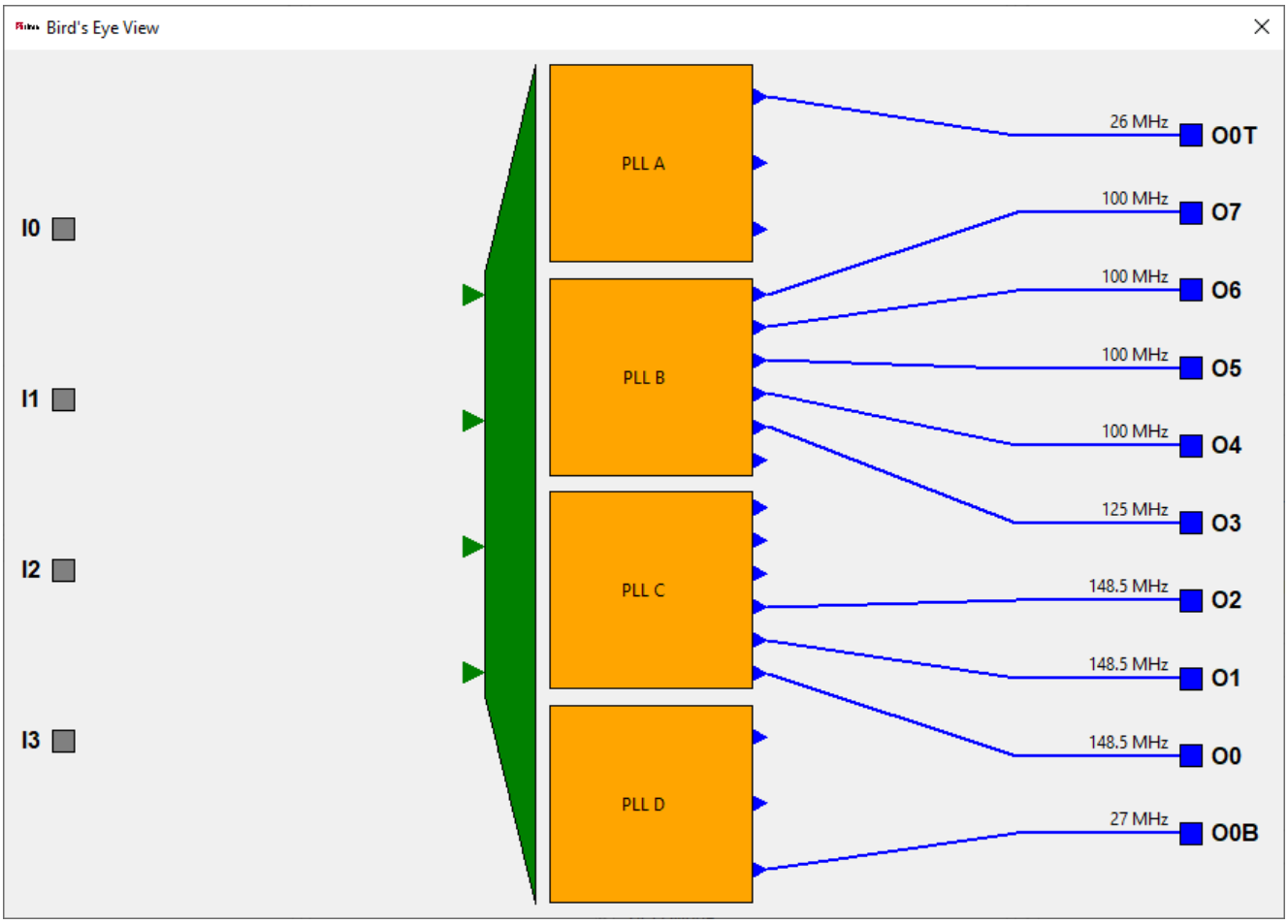

Figure 7: 4K-to-8K encoder frequency plan

5.2 Fiber link clock tree

The application in the figure below shows an example using a fiber link with a jitter cleaner clock tree.

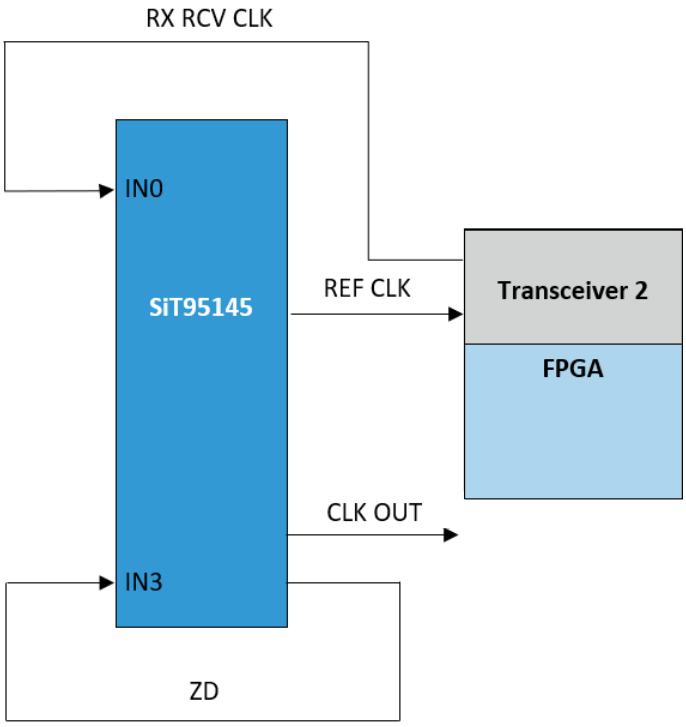

Figure 8: Fiber link clock tree

This table lists all frequency values for the fiber link.

Table 4: Fiber link frequencies list

Clock Name	Clock Frequency Value, MHz	Comments
RX RCV CLK	80	Recovered clock
REF CLK	160	Reference clock
CLK OUT	40	Output clock
ZD	80	Zero-delay mode clock

In this application, a SiTime SiT95145 is used as a jitter cleaner of a recovered clock from an FPGA transceiver.

The frequency plan is implemented in the Cascade GUI, as shown in the figure below.

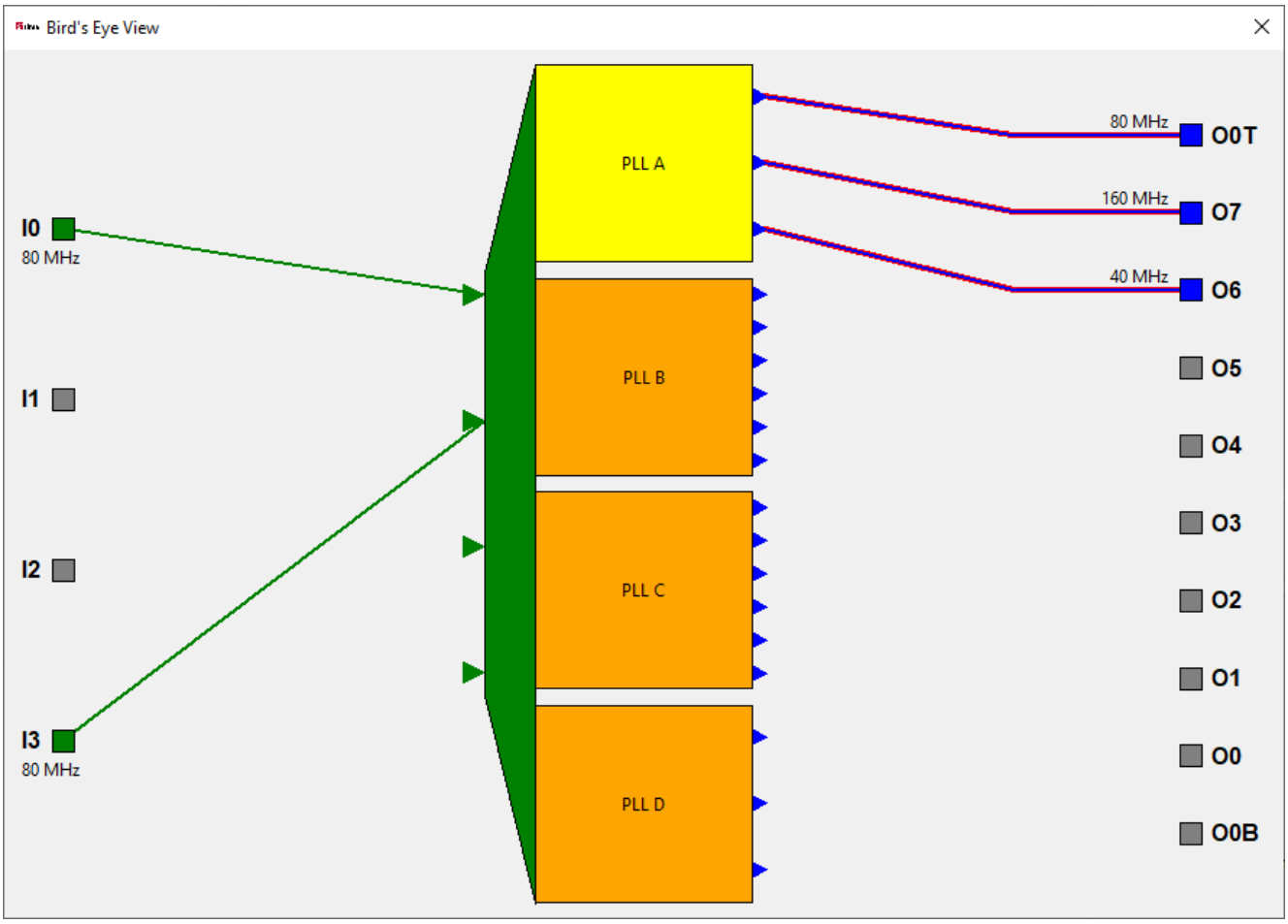

Figure 9: Fiber link frequency plan

5.3 Base Station RRU with eCPRI Clock Tree

This example uses a base station RRU with an eCPRI clock tree, as shown below.

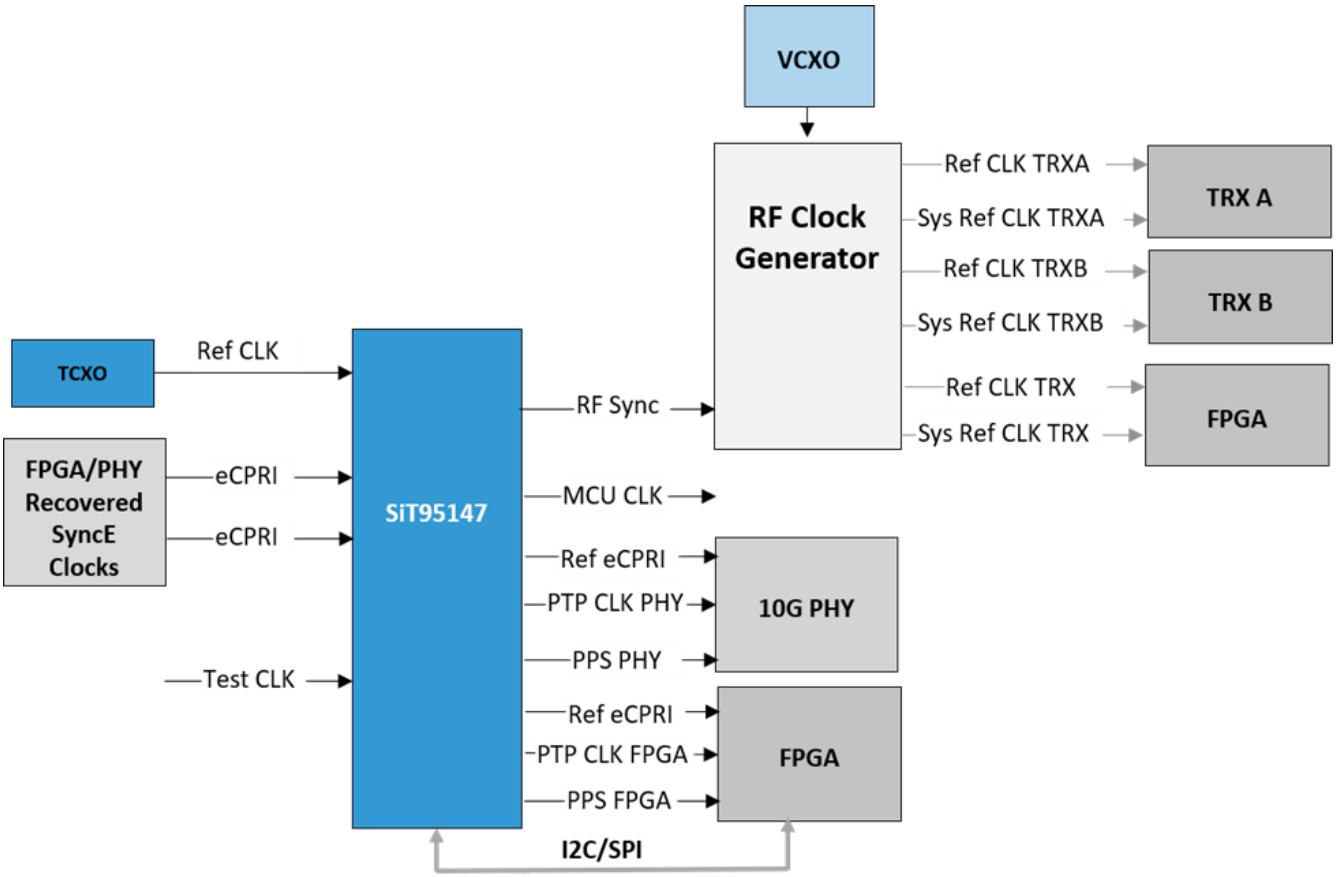

Figure 10: Base station RRU with eCPRI clock tree

The following table lists all frequency values for the base station RRU with eCPRI example.

Table 5: Base station RRU with eCPRI frequencies list

Clock Name	Clock Frequency Value, MHz	Comments
Ref CLK	10	TCXO Reference Clock
eCPRI	156.25	
Test CLK	10	Test Clock
RF Sync	30.72	RF Sync Clock
MCU CLK	100	MCU Reference Clock
Ref eCPRI	156.25	
PTP CLK PHY	125	
PPS PHY	1E-6	
PTP CLK FPGA	125	
PPS FPGA	1E-6	
Ref CLK TRXA	122.88	
Sys Ref CLK TRXA	7.68	
Ref CLK TRXB	122.88	
Sys Ref CLK TRXB	7.68	
Ref CLK TRX	122.88	
Sys Ref CLK TRX	7.68	

In this application, the SiTime SiT95147 network synthesizer is used.

The frequency plan is implemented in the Cascade GUI, as shown in the figure below.

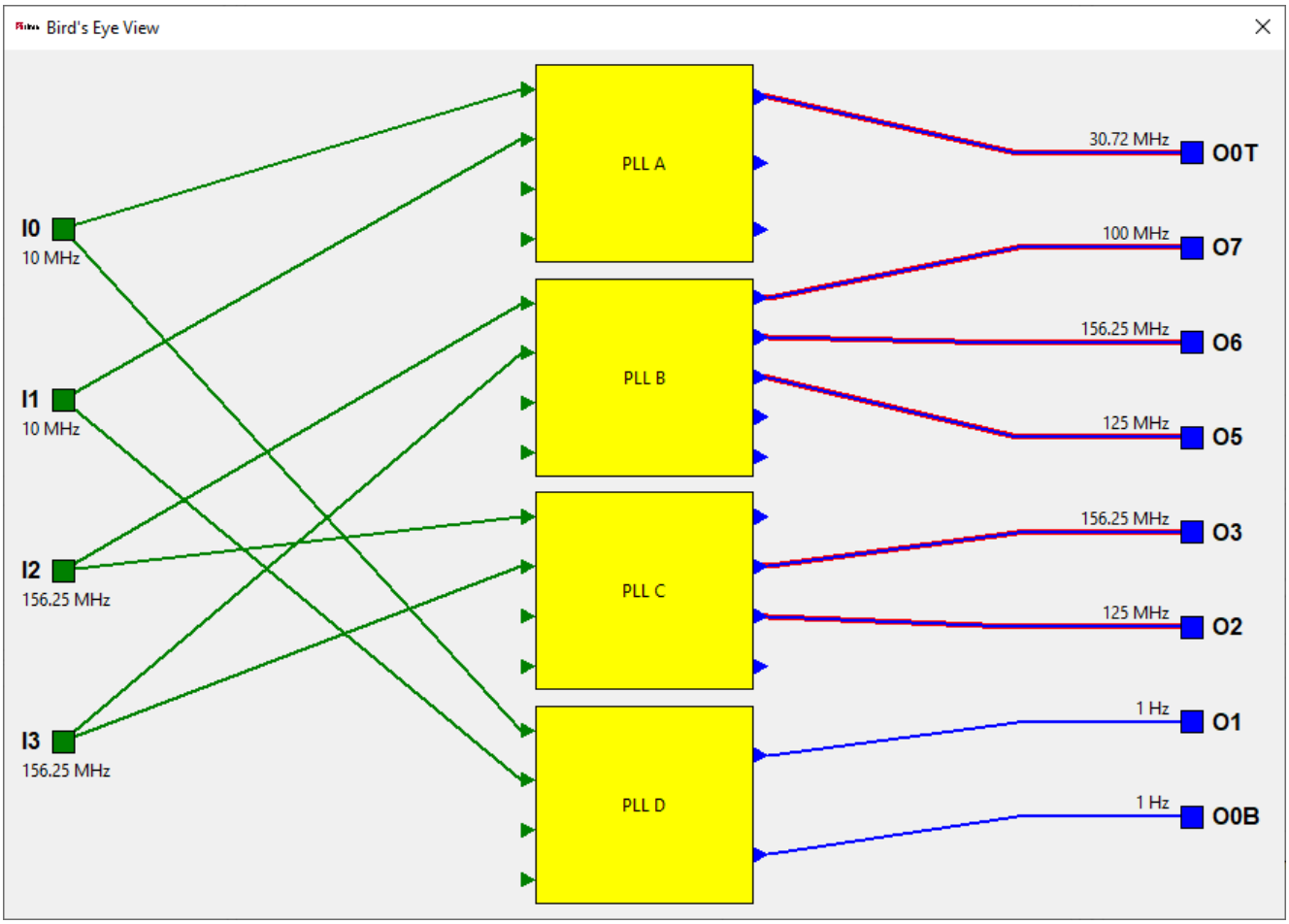

Figure 11: Base station RRU with eCPRI frequency plan

6 Summary

- Clock trees can be highly complex or relatively simple, but in all cases, they provide a fundamentally important part of the system and must be optimized for performance and cost.

- SiTime provides different types of clock tree components and the SiTime Cascade GUI software to simplify how you configure not only the most demanding applications, but also the most cost-conscious ones.

7 Revision history

Table 6: Document revision history

Revision	Date	Description
1.1	26 May 2022	Initial release.

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