XCalibur Active MEMS Resonator
MCU Requirements

Application Note

Contents

1 Introduction

Embedded microcontroller (µM/MCU) and micro-processor systems typically rely on an external quartz-based resonator for their operation. XCalibur active MEMS resonators are a drop-in replacement for 4-pin SMD resonators and offer a reliable, higher frequency stability alternative to quartz-based MHz resonators Figure 1.

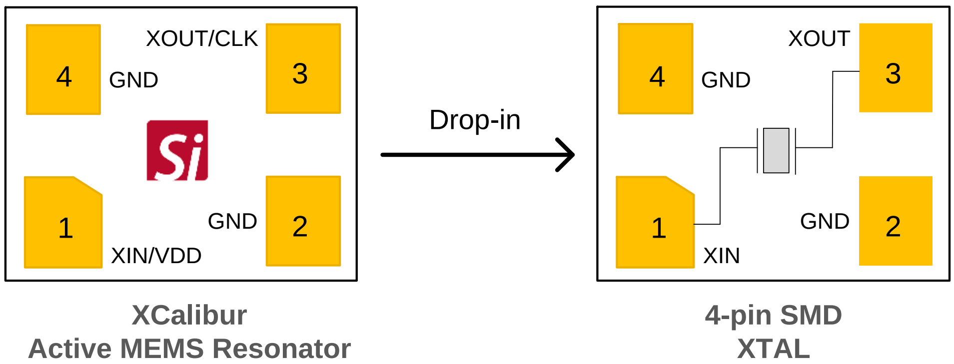

Figure 1: XCalibur Active MEMS Resonator Drop-In Compatible with 4-Pin SMD XTAL (TOP View)

The MCU system must meet the following conditions before XCalibur active MEMS resonators can be used as a drop-in replacement:

1. MCU can disable analog-mode for external crystal-resonator and bypass the MCU's internal Pierce oscillator circuit.
2. MCU can enable digital mode and drive GPIO to VDD to power up XCalibur XIN pin with ≥ 6 mA of current.
3. External pair of loading caps should be removed and a 4.7 nF decoupling cap to be placed on XIN for the GPIO power.

This application note provides details on the three requirements above to ensure a seamless drop-in transition to XCalibur resonators.

Example firmware is provided in Chapter 4: MCU Programming Requirements for a select number of MCUs where XCalibur resonators have been tested successfully. Sample firmware highlights required steps to switch from Analog Mode to Digital Mode to power up XCalibur.

Appendix A lists compatible MCUs that support XCalibur resonator requirements listed above.

A list of MCU that are **not** compliant with XCalibur resonator requirements are provided in Appendix B.

2 MCU Analog and Digital Operation Modes

Quartz-based resonators rely on a Pierce oscillator inside an MCU to bias and drive the external resonator. XCalibur active resonators do not rely on a Pierce oscillator and only require power from the MCU's GPIO (X1 in Figure 2).

To meet this requirement, the MCU must disable the *Analog Mode* to bypass the Pierce oscillator (X1 and X2 pins), and then enable *Digital Mode* to provide GPIO power from X1 to XIN pin of the XCalibur resonator.

This analog to digital operating mode change is shown conceptually in Figure 2.

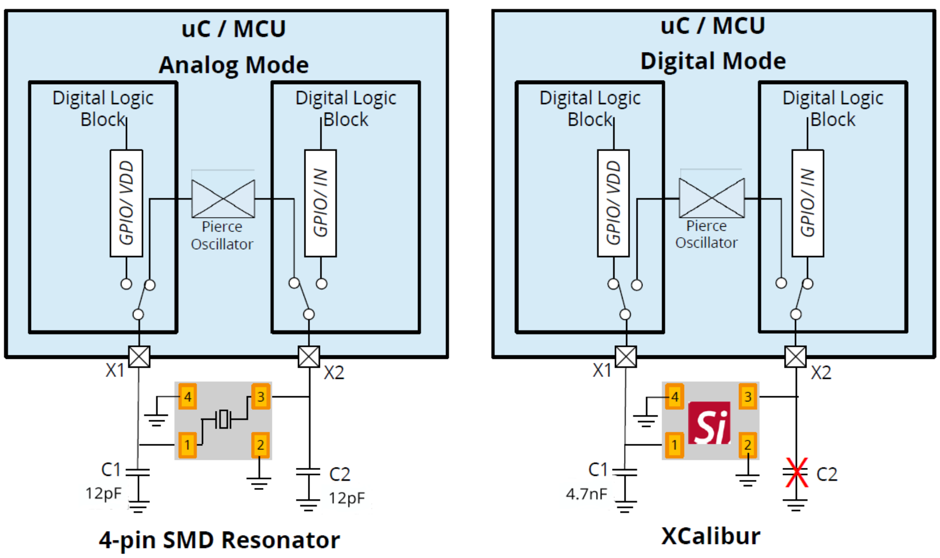

Figure 2: MCU in Analog Mode with Pierce Oscillator (left), and Digital Mode with GPIO Enabled (right)

3 MCU GPIO

The XCalibur SiT14xx family of resonators require a power source from the MCU. This section outlines power requirements from the MCU and considerations to mitigate potential transient-currents that may be present during power-up and power-down events.

List of power requirements:

1. The MCU must provide power over GPIO in the range of 1.8 V to 3.3 V.
2. The GPIO must deliver 6 mA or greater current.
3. External crystal-resonator loading caps are removed, and a single decoupling cap of 4.7 nF is added on the VDD pin of the XCalibur resonator.
    a. An MCU with on-chip loading caps should accommodate an external decoupling cap on the existing PCB.

3.1 Power Requirements (VDDIO)

Most MCUs can provide a GPIO voltage (VDDIO) equal to the core-voltage VDD. Any voltage drop on the GPIO must be accounted and maintained within the operating specification range of XCalibur resonators.

3.2 Current Requirements

A minimum of 6 mA or greater current is required for normal operation across supported voltage supplies between 1.8 V to 3.3 V. Using a 4.7 nF decoupling cap is a requirement that will ensure stable power supply that will meet XCalibur requirements.

3.3 Decoupling Cap Power Filter

A 4.7 nF decoupling cap is required when using XCalibur resonators as a drop-in replacement. This capacitor replaces the existing 12 pF loading capacitor C1 on X1 (XCalibur XIN) Pin. The second 12 pF loading cap C2 on X2 must be removed.

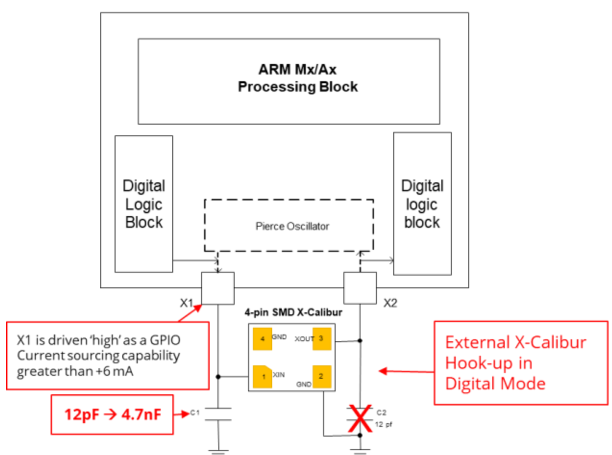

Figure 3. MCU De-Coupling Cap on GPIO

The decoupling cap minimizes power supply fluctuations and filters out power supply noise due to external influences. Adding a decoupling capacitor to a circuit introduces charge and discharge currents during power-up (rising edge) and power-down (falling edge) of the GPIO output (Figure 4).

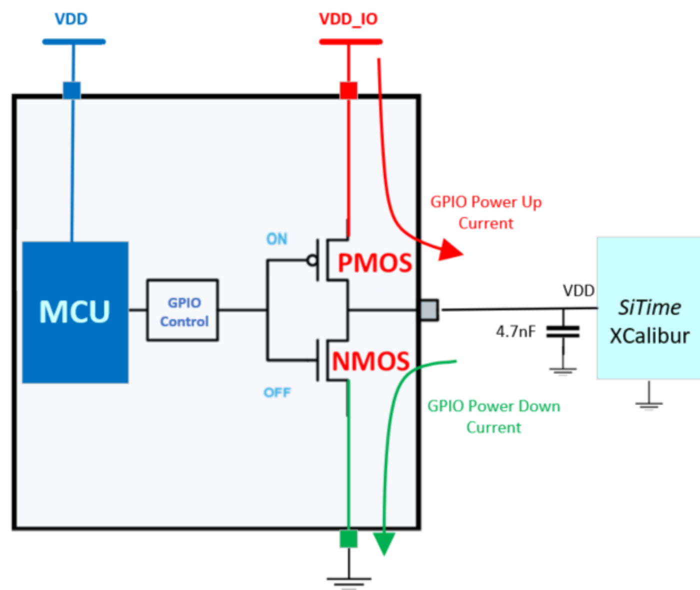

Figure 4. MCU Push-Pull Output Voltage and Current Path

4 MCU Programming Requirements

After reset, an MCU is brought up using an internal low-rate RC oscillator to manage basic H/W configuration and initialization of its I/O pins. This section gives example code for a select number of MCUs to configure their GPIO for proper operation using XCalibur active MEMS resonators. Sample code is provided for the following MCUs:

- Microchip/Atmel ATSAME54P20
- TI MSP432P4111P
- NXP S32K146
- Renesas R7FS5D97
- ST Micro STM32F303

Please contact SiTime for any support in programming different MCU.

4.1 Microchip/Atmel ATSAME54P20

The external oscillator operations are configured via OSCCTRL control registers. Through this interface, these oscillators are enabled, disabled, or have their calibration values updated.

The external Multipurpose Crystal Oscillator (XOSCn) can operate in two different modes:

- External clock, with an external clock signal connected to the XIN pin
- Crystal oscillator, with an external 8-48 MHz crystal connected to the XIN and XOUT pins

After a reset, the XOSCn is disabled and the XINn/XOUTn pins can be used as General Purpose I/O (GPIO) pins by other peripherals in the system.

When XOSCn is enabled, the operating mode determines the GPIO usage. The XINn and XOUTn pins are controlled by the OSCCTRL when in crystal oscillator mode, and GPIO functions are overridden on both pins.

Only the XINn pins will be overridden and controlled by the OSCCTRL when in external clock mode, while the XOUTn pins can still be used as GPIO pins.

The latter is the mode used by XCalibur resonators.

Table 1: Atmel ATSAM54P20 sample code for configuring XOUT as GPIO

```
OSCCTRL->XOSCCTRL[1].reg &= ~(1 << 2);    //  select external clock instead of crystal by //writing 0 to XTALEN bit
PORT->Group[1].DIRSET.reg |= (1 << 23);    // configure XOUT (PB23) as pin out
PORT->Group[1].OUTSET.reg |= (1 << 23);   // set PB23 to high state
OSCCTRL->XOSCCTRL[1].reg |= (1 << 1);      // enable OSC block by writing 1 to ENABLE bit
/* wait 5ms to ensure XCalibur starts */
/* select XOSC1 as a clock source for the system (e.g., for DPLL or GCG) */
```

4.2 Texas Instruments MSP432P4111P

TI MSP432P4111P device can support a high-frequency crystal on the HFXT pins.

It is possible to apply an Oscillator digital clock such as XCalibur to the LFXIN and HFXIN input pins when the appropriate LFXTBYPASS or HFXTBYPASS mode is selected.

In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes. If they are left unused, they must be terminated.

XCalibur uses this HFXTBYPASS mode to use the HFXT pins in GPIO mode.

Table 2: TI MSP432 sample code to enable GPIO Mode

```
CS->KEY = 0x695A;                          // unlock clock system registers

CS->CTL2 &= ~(1 << 25) | ~(1 << 24)        // Set HFXT for bypass mode

PJ->SEL0 = (PJ->SEL0 & 0xF3) | 0x08;       // Set HFXIN to bypass mode
PJ->SEL1 = (PJ->SEL1 & 0xF3) | 0x00;       // Set HFXOUT to GPIO mode

PJ->DIR |= (1 << 2);                       // set HFXOUT (PJ.3) to Out direction
PJ->OUT |= (1 << 2);                       // set PJ.3 to high state

/* wait 5ms to ensure XCalibur starts */
/* select HFX as a clock source for the system */

CS->KEY = 0;                 // lock clock system registers
```

4.3 NXP S32K146

NXP S32K1XX is a low-power ARM Cortex-M4F/M0+ core micro-controller.

Clocking options for the NXP processor are:

- 4 to 40 MHz fast external oscillator (SOSC) or 50 MHz DC external square input clock in external clock mode
- 48 MHz Fast Internal RC oscillator (FIRC)
- MHz Slow Internal RC oscillator (SIRC)
- 128 kHz Low Power Oscillator (LPO)
- Up to 112 MHz (HSRUN) System Phased Lock Loop (SPLL)
- Up to 20 MHz TCLK and 25 MHz SWD_CLK
- 32 kHz Real Time Counter external clock (RTC_CLKIN)

XCalibur uses “SOSC” external oscillator mode using the following configuration.

Table 3: NXP S32K146 SOSC external clock mode configuration firmware

```
SCG->SOSCCFG &= ~(1 << 2);          // configure SOSCCFG External reference clock

PCC-> PCCn[0x128] |= (1<<30);       // Enable clock on PORT B
PORTB->PCR[6] |= (PORTB->PCR[6] & 0xFFFFF8BF)|(1<<8)|(1<<6);
// Configure XTAL (PB6) pins to GPIO with high drive strength

PTB->PDDR |= 1 << 6;                // set XTAL pin(PB6) to out direction
PTB-> PSOR |= 1 << 6;               // set PB6 to high state

/* wait 5ms to ensure XCalibur starts */
/* select OSC as a clock source for the system */
```

4.4 Renesas R7FS5D97

The Renesas MCU supports an external oscillator by configuring XTAL as a CMOS GPIO Output and EXTAL as the clock input.

XCalibur clock output is connected to EXTAL input of the MCU.

Table 4: Renesas R7FS5D97 MCU EXTAL/XTAL clock mode configuration firmware

```
R_SYSTEM->PRCR = 0xA501;            // Enables writing to the registers related to
                                    the Clock Generation Circuit

R_PFS->P213PFS = 0xC00;             // set XTAL pin function as CMOS with hi-drive
                                    capability

R_IOPORT2->PCNTR1 | = (1 << 29) | (1 << 13)      // Configure XTAL pin (P213) to out
                                                 direction with high state

R_SYSTEM->MOSCCR_b.MOSTP = 0x01;    // stop main oscillator
R_SYSTEM->MOMCR_b.MOSEL = 0x01;  // Configure Main Clock to external clock input
R_SYSTEM->MOSCCR_b.MOSTP = 0;    // enable main oscillator

R_SYSTEM->PRCR = 0x0;               // Disable writing to the registers related to
                                    the Clock Generation Circuit

/* wait 5ms to ensure XCalibur starts */
/* select Main clock oscillator as a clock source for the system */
```

4.5 ST Micro STM32F303

```
RCC->CR |= (1 << 18) | (1 << 16);             // Configure external clock

RCC->AHBENR |= (1 << 22);                     // enable clock on PORT F
GPIOF->MODER |= (GPIOF->MODER & 0xFFFFFFF3) | 0x04; // set    PF1    (XOSC_OUT)    pin
                                                    function as GPIO
GPIOF->OTYPER &= ~ (1 << 1);                  // select output type as push-pull
GPIOF ->OSPEEDR |= (1 << 3) | (1 << 2);// select hi-drive capability
GPIOF->BSRR |= (1 << 1);                      // set PF1 to high state

/* wait 5ms to ensure XCalibur starts */
/* select Main clock oscillator as a clock source for the system */
```

5 Appendix A: MCU Compatibility List

The following compatibility list has been compiled based on information obtained from each MCU datasheet. Please contact the SiTime support team for the latest update to this list.

Table 5: XCalibur MCU Compatibility (Based on Datasheet)

Manufacturer	MCU Type	MCU Series	MCU PN	XCalibur Compliant Based on Datasheet (with Sample Code *)
ST-Micro	ARM	STM32F	STM32F303RET6	**Yes***
ST-Micro	ARM	STM32G STM32G0	STM32G081xB STM32G474xB	**Yes**
ST-Micro	ARM	STM32H	STM32H742xI/G	**Yes**
ST-Micro	ARM	STM32L0 STM32L1 STM32L4 STM32L4+ STM32L5	STM32L010RB STM32L151xE STM32L471xx STM32L4R5xx STM32L562xx	**Yes**
ST-Micro	ARM	STM32U	STM32U585xx	**Yes**
Microchip (Atmel)	ARM	ATSAME54	ATSAME54P20	**Yes***
TI	ARM	MSP432	MSP432P4111P	**Yes***
Renesas	ARM	S5D9	R7FS5D97E3A01CFC	**Yes***
NXP	ARM	S32K1xx	S32K146	**Yes***
Infineon (Cypress)	ARM	PSoC4-BLE	CY8C4248LQI-BL583	**Yes**
Microchip	CISC	PIC18	PIC18LF46K22T-I/ML	**Yes**

6 Appendix B: Incompatible MCU List

The following MCUs are not compatible as a drop-in replacement for XCalibur resonators. Please contact the SiTime support team for the latest update to this list.

Table 6: Incompatible MCU List (Based on Datasheet)

Manufacturer	Grade	MCU Series	MCU PN	XCalibur Compliant
ST-Micro	Commercial	STM32WB STM32WL		**No**
ST-Micro	Auto	SPC5	SPC58EC80E5	**No**
Infineon	Auto	TC3xx(Aurix)	SAK-TC375TP-96F300W	**No**
Infineon	Industrial	XMC4000		**No**
TI	Auto	CC2642R-Q1	CC2652R1FRGZ	**No**
Renesas	Commercial	RL78/G13	R5F100LEAFB	**No**
NXP	Commercial	LPC11U68	LPC11U68JBD100	**No**
NXP	Auto	S32G	S32G2	**No**
Cypress	Auto	PSoC4-BLE	CY8C4248LQI-BL583	**No**
SiLabs	Commercial	EFM32G	EFM32G890F128	**No**
Renesas	Automotive	RH-850/D1L2	R7F701422	**No**

Table 7: Revision History

Version	Release Date	Change Summary
0.1	1-Nov-2021	Initial Release
0.2	2-Nov-2021	Updates to Diagrams, General Text
0.4	8-Nov-2021	Added ST-Micro Sample Code; Updates to Compatibility and Non-Compliant Lists; Formatting and logo update
0.5	10-Nov-2021	Updates to Diagrams. General edits.
0.6	28-Dec-2021	Incorporate general feedback. Editorial review

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439