SiT6760EB Evaluation User Manual

Contents

1 Introduction

The SiT6760EB evaluation board (EVB) is a simple and easy to use tool that enables component-level performance evaluation of SiTime SiT9501 and SiT937x differential oscillators. The EVB is shipped to customers with the differential oscillator in 3.2 mm x 2.5 mm 6-pin QFN package mounted on the board. The oscillator is factory pre-configured according to the ordering part number.

The SiT6760EB supports all output signal options of SiTime SiT9501 and SiT937x differential oscillators, such as LVPECL, LVDS, HCSL, low-power HCSL and FlexSwing™. For more information about specific signaling options please refer to the product datasheet.

2 Board Overview

The SiT6760EB EVB is a 2 x 2 inch PCB (Figure 1). The only active device on the EVB is the SiTime differential oscillator. The board contains input and output connectors described in Table 1, a power supply bypass network (on the back side of the board) and a configurable universal differential output termination network.

To improve signal integrity the configurable universal differential termination network is designed to have minimum stubs and trace impedance mismatches. Since it contains a large variety of termination configurations, some resistor placeholders are dual-purpose and can accommodate capacitors. For example, R12 can be a 0-ohm resistor in one configuration and a 0.1-uF capacitor in another. Section 3 describes configuration of the EVB at shipment.

The full detailed schematic is shown in Appendix A.

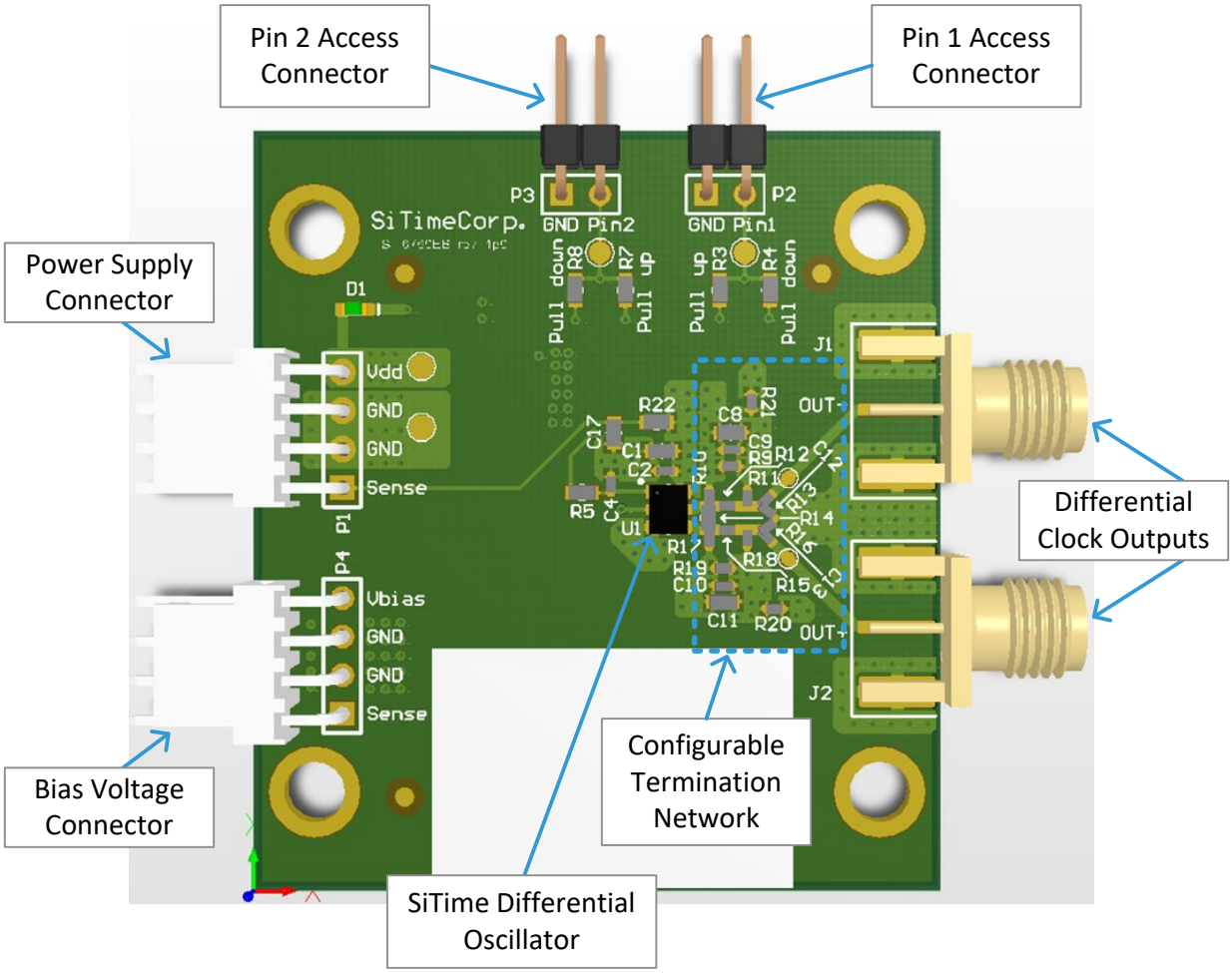

Figure 1: SiT6760EB

Table 1: I/O Connectors Description

Connector Name	Designator	Functional Description
Vdd	P1	Oscillator power supply input. 4-pin connector. Vdd pin – Input pin for external power supply. GND pins – PCB ground (including oscillator ground). Sense pin – Vdd sense signal of the oscillator power supply. Routed directly from the Vdd pad of the oscillator through low-pass RC filter (C17 + R22). Pin locations are identified in the silkscreen.
Vbias	P4	Output termination bias voltage input. Used with certain differential termination options to supply external bias voltage. 4-pin connector. Vbias pin – Input pin for external bias voltage. GND pins – PCB ground (including oscillator ground). Sense pin – Bias voltage sense signal. Routed directly from the trace connecting to termination network through low-pass RC filter (C15 + R23).
Pin 1	P2	A 2-pin header provides access to pin 1 of the oscillator. Has on-board placeholders for pull-up and/or pull-down resistors.
Pin 2	P3	A 2-pin header provides access to pin 2 of the oscillator. Has on-board placeholders for pull-up and/or pull-down resistors.
OUT+ and OUT-	J1, J2	Differential outputs of the device

Note: Pin 1 location of the oscillator is indicated on the silkscreen with a dot.

3 Standard Shipping Configurations

To simplify the evaluation of SiTime differential oscillators the SiT6760EB is shipped with the assembly option that enables direct connection of the EVB to measurement equipment with 50-ohm inputs, such as a high-speed oscilloscope. SMA cables of the same length must be used to connect both true and complimentary outputs of the EVB, otherwise undesired signal skew between the differential outputs will be introduced due to unequal signal delays in the cables.

The default shipping configuration depends on the requirements of the specific output signaling type. This section describes the default shipping configuration for each signaling type.

3.1 LVPECL, FlexSwing and LVDS Shipping Configuration

LVPECL, FlexSwing and LVDS output drivers share the same shipping configuration that enables direct connection to the instrument with a 50-ohm input. The termination on the EVB is very simple and consists of a pair of 0.1-uF capacitors connected in series with the differential output (Figure 2). This configuration assumes that the measurement instrument has a built-in 50-ohm termination which completes an AC-coupled termination for the differential driver.

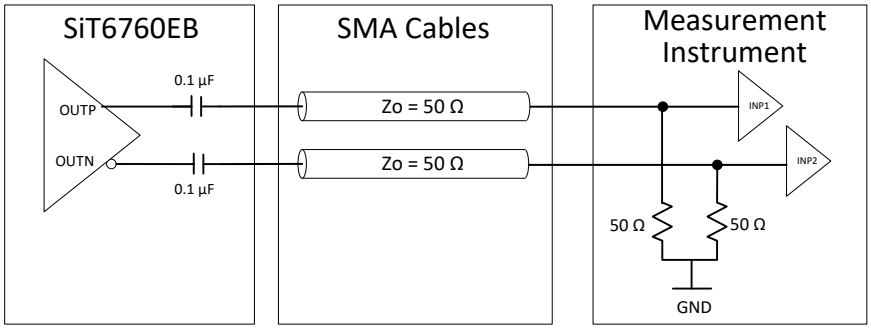

Figure 2: LVPECL, FlexSwing and LVDS AC-coupled termination for direct connection to the instrument with 50-ohm inputs

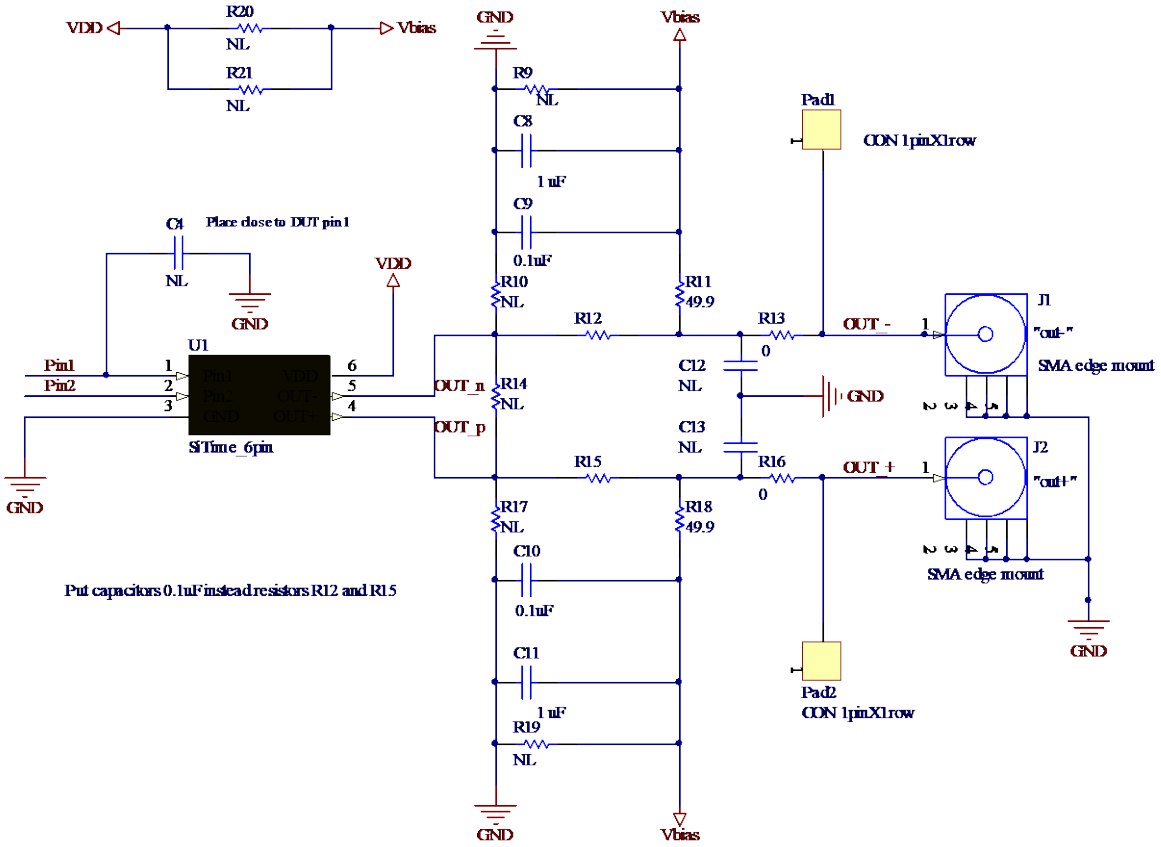

Figure 3: Schematic of LVPECL, FlexSwing and LVDS standard shipping configuration. NL designates components that should not be loaded. Note that resistor footprints R12 and R15 should be loaded with 0.1-uF capacitors

3.2 HCSL Shipping Configuration

The HCSL output driver configuration enables direct connection to the instrument with a 50-ohm input consisting of a pair of 33-ohm resistors connected in series with the differential output (Figure 4). This configuration assumes that the measurement instrument has a built-in 50-ohm termination which completes a DC-coupled termination for the HCSL driver.

In contrast to the standard HCSL driver, the low power HCSL driver should not be directly connected to 50-ohm instrument inputs as it will experience signal attenuation and will not meet the datasheet specs.

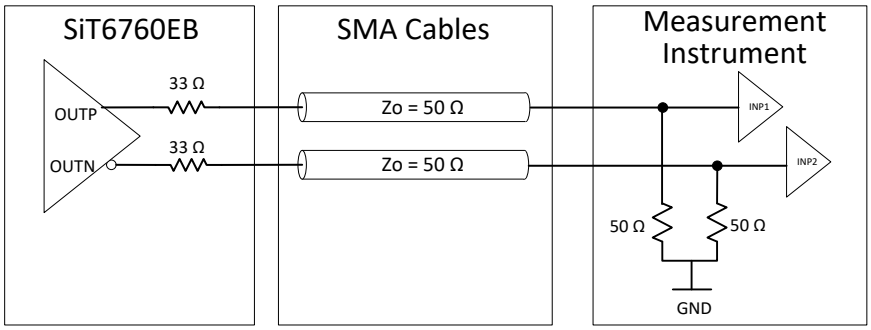

Figure 4: HCSL DC-coupled termination for direct connection to the instrument with 50-ohm inputs

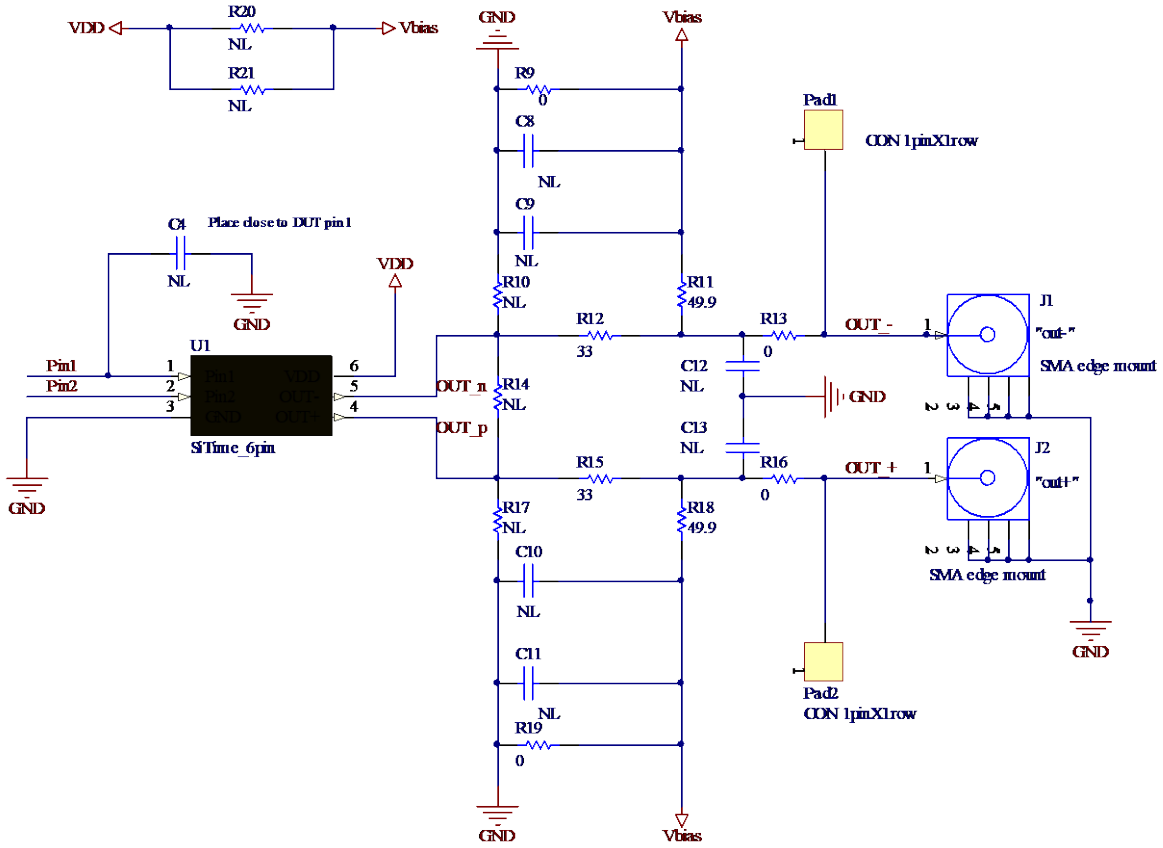

Figure 5: Schematic of HCSL standard shipping configuration. NL designates components that should not be loaded

4 Phase Noise and Phase Jitter Measurement

When measuring phase noise using an instrument with only a single-ended input, such as a spectrum analyzer or phase noise analyzer (e.g. Keysight Technologies E5052B Signal Source Analyzer), it can be convenient to connect one of the differential outputs to the equipment and apply a dummy termination to the other output to balance the load. This approach often yields acceptable results, but in a low noise device the phase noise measurement may suffer a few dB of noise floor degradation at offsets above 10 MHz.

To resolve this issue, it is recommended to use a balanced-unbalanced (balun) transformer to convert the differential signal into a single-ended signal without performance degradation. This balun takes the differential input and produces a single-ended output that is the difference between OUTP and OUTN. The common-mode noise present on individual conductors of a differential-pair are attenuated inside the balun.

The SiTime SiT6801EB balun board can be used together with the SiT6760EB as shown in Figure 6. For more information regarding measuring phase noise, refer to application note AN10067.

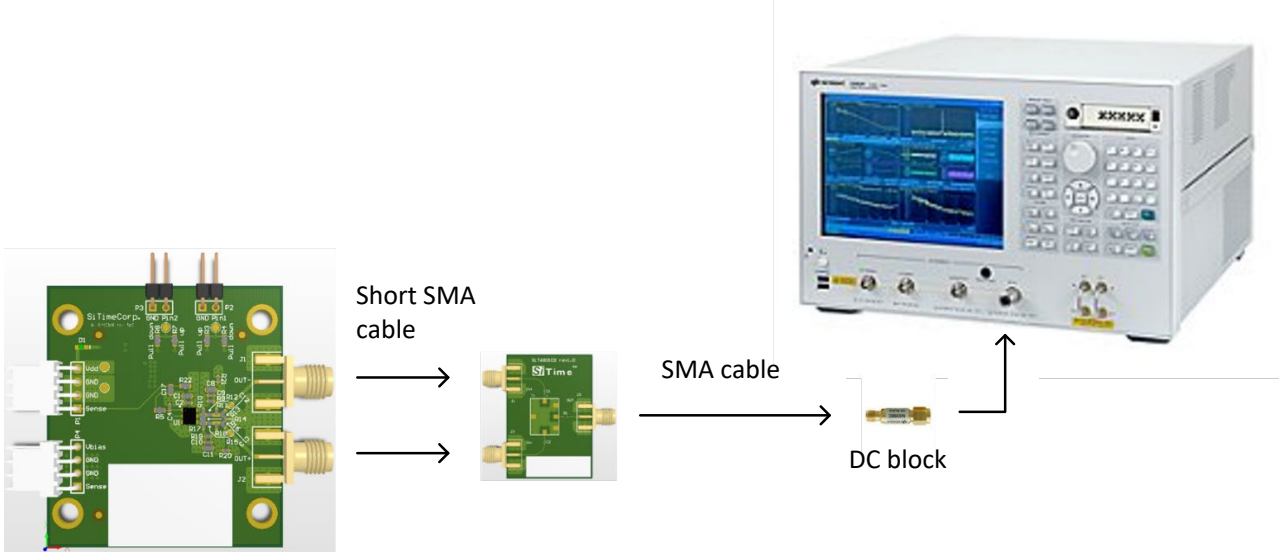

Figure 6: SiT6760EB (left) and SiT6801EB connection for phase noise and phase jitter measurements

Appendix A – Generic EVB Schematic*

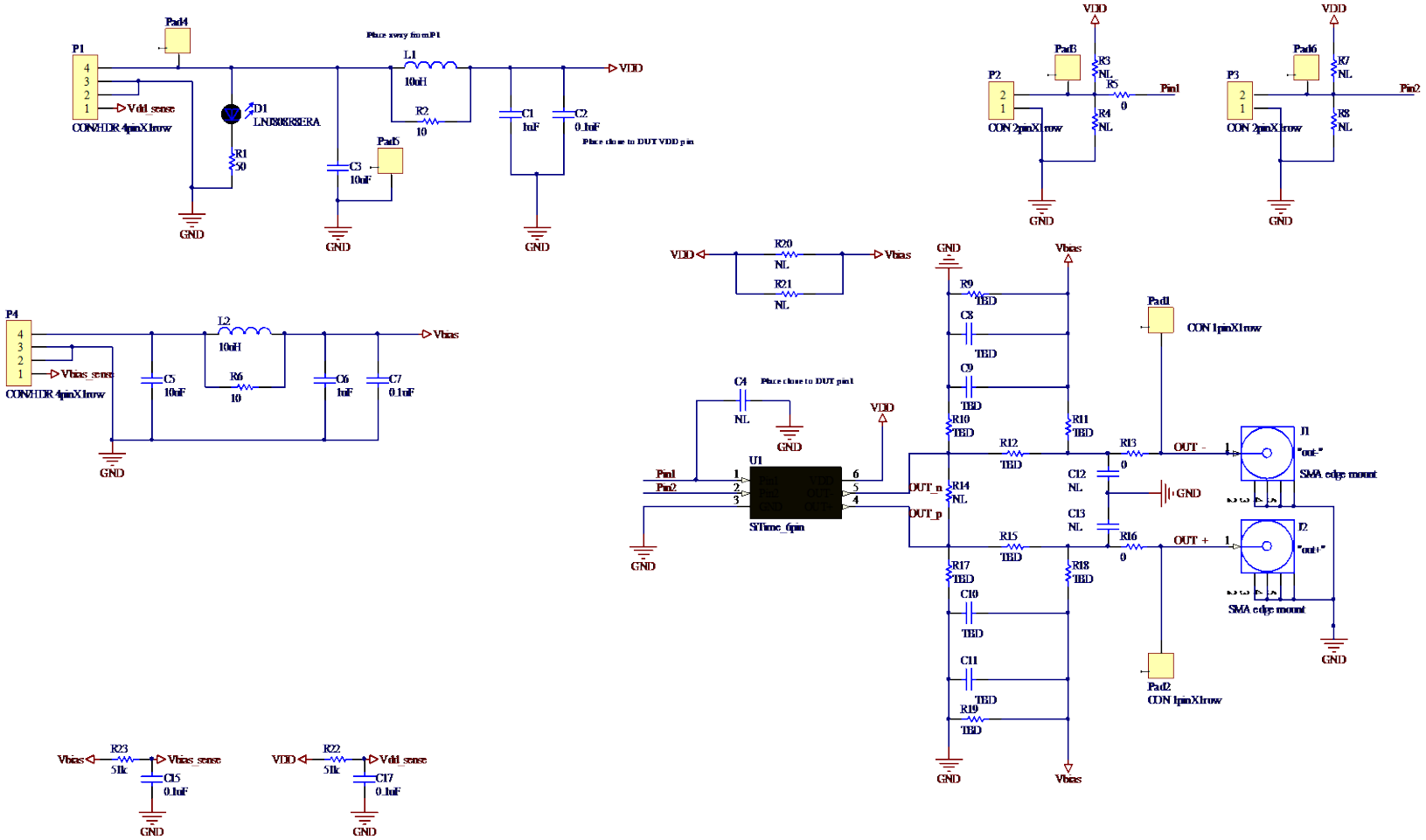

Figure 7: SiT6760EB rev 1.0 schematic

*Refer to Section 3 for the exact termination circuit assembly option for your shipping configuration.

Appendix B – Connector Ordering Codes

Table 2: Connector Ordering Codes

Connectors	Digi-Key p/n	Digi-Key p/n for mating connector	Digi-Key p/n for associated products
POWER	WM4302-ND	WM2002-ND	WM1114-ND
VBIAS	WM4302-ND	WM2002-ND	WM1114-ND
PIN 1	732-5335-ND	609-2341-ND	609-3614-1-ND
PIN 2	732-5335-ND	609-2341-ND	609-3614-1-ND
OUTPUT	343-CONSMA020.062-G-ND		

Appendix C – Board View

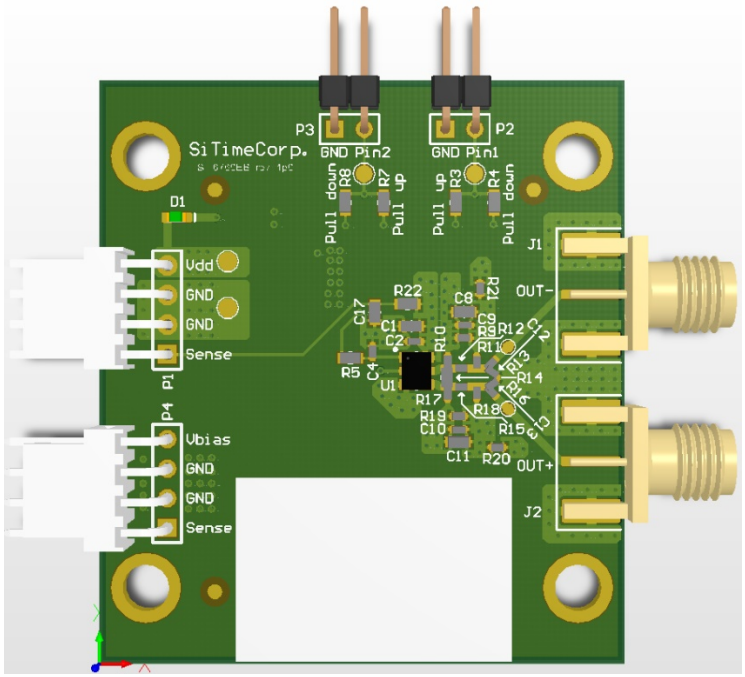

Figure 8: SiT6760EB rev 1.0 – Top view

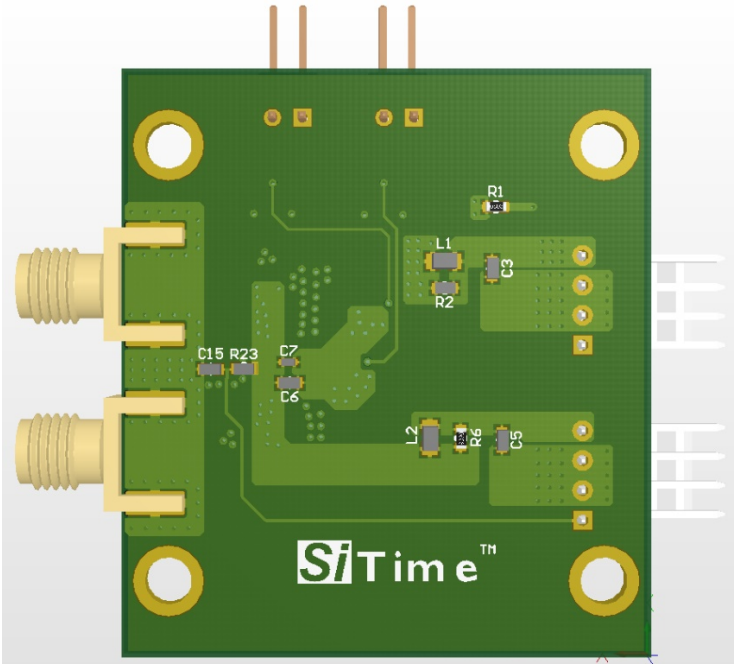

Figure 9: SiT6760EB rev 1.0 – Bottom view

Table 3. Revision History

Version	Release Date	Change Summary
1.0	Nov 10, 2020	Preliminary version

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