SiT6722EB Evaluation Board User Manual

Contents

1 Introduction

The SiT6722EB evaluation board (EVB) is designed for use with SiTime's Elite Super-TCXOs in the 10-pin, 5.0x3.2 mm ceramic packages. It enables the evaluation of key functionalities of these precision Super-TCXOs in all three configuration modes including TCXO, VCTCXO and DCTCXO with I^2C.

EVB Features

- Support for all three Super-TCXO configuration modes: TCXO, VCTCXO, DCTCXO
- Probing points for frequency measurements
- Connector access for controlling the output frequency via I^2C
- Connector for current measurement

SiTime typically ships the EVB with the Super-TCXO mounted using SiTime recommended reflow profile. The Super-TCXO device should only be evaluated in its original soldered down state for best signal integrity and frequency stability. The device performance is not guaranteed if it is de-soldered and then re-soldered either manually or via reflow process.

2 I/O Descriptions

Table 1: SiT6722EB I/O

I/O	Description
Power	SMA connector (J1), a two-pin connector (P5) for DC power supply. Pins polarities are identified on the silkscreen pattern near the connector (see Figures A1 and A2). Two-pin headers (P3, P4).
Pin 1 access	A two-pin header (P7) provides access to the pin 1 of the Super-TCXO in either OE mode or VCTCXO mode. In OE mode, pin 1 can be left floating as there is an internal pull-up resistor.
Frequency control via I^2C	A five-pin header (P9) provides access to I^2C (SDA, SCL).
Output	Oscillator output can be accessed either using active probe or SMA connector. The test points for active probe are placed closely to the oscillator output for better signal integrity (see Figure A2). The output pin of the oscillator can also be connected to the SMA connector (J2) through the R9 source termination resistor. Section 3.2 describes in details the recommended measurement configurations.
Current Measurement	A two-pin connector (P6) enables measuring the current consumption of the device.
Service connectors	P1, P2, P3, P4 are reserved for SiTime internal use only.

3 EVB Usage Descriptions

3.1 EVB Configurations

SiT6722EB can be configured to support all three Super-TCXO configuration modes including TCXO with output enable (OE), VCTCXO with analog voltage control and DCTCXO with I^2C.

Figure A1 in Appendix A shows the complete electrical schematic of SiT6722EB. Components labeled "DNP" are not assembled.

Oscillator output waveform can be measured with an active probe in all configurations. The value of the load capacitor C5 can be adjusted to match the load conditions in the target application. This enables the user to measure waveform characteristics under similar conditions as close to those on the target board as possible.

Shipment Configuration
SiT6722 is shipped without components labeled "DNP" on the schematic (see Figure A1 in Appendix A).

3.1.1 I^2C Support

The two pull up resistors (R10 and R11 with 4.7 kOhm value) need to be assembled to support the I^2C configuration. If requested, the EVB will ship with these resistors.

3.2 Waveform Capturing Using Active Probe

SiTime Elite Super-TCXO is a high-speed logic output device. It is critical that the proper logic and high frequency measurement techniques are used along with the high-quality active probe in order to ensure best measurement results.

SiTime recommends the following minimum equipment for proper clock waveform measurement:

1) GHz or higher active probe with capacitance <1 pF, such as an Agilent1134A.
2) Oscilloscope with 4GHz bandwidth or higher such as a DSA90604A.

A passive voltage probe should not be used as it adds a high capacitive load to the part and the long ground lead clip is not suitable for high frequency measurement applications. The inductance of the long ground lead coupled with the input capacitance of the probe results in a resonant circuit. The consequence of this resonance results in the distortion of the clock signal. Typical manifestations of this distortion include ringing, overshoot, and undershoot of the clock signal.
Eliminating such distortion requires a probe with the lowest input capacitance and a low inductance ground lead. In addition, SiTime Super-TCXOs are typically configured for fast rise and fall times (1 ns or less) with 15 pF load. It is therefore critical that the probe tip ground be as short as possible, lowest inductance, and the return path for the ground be located as close as possible to the trace carrying the RF logic signal. Please refer to Figure A2 for test point locations on the SiT6722EB and an example of proper probing.

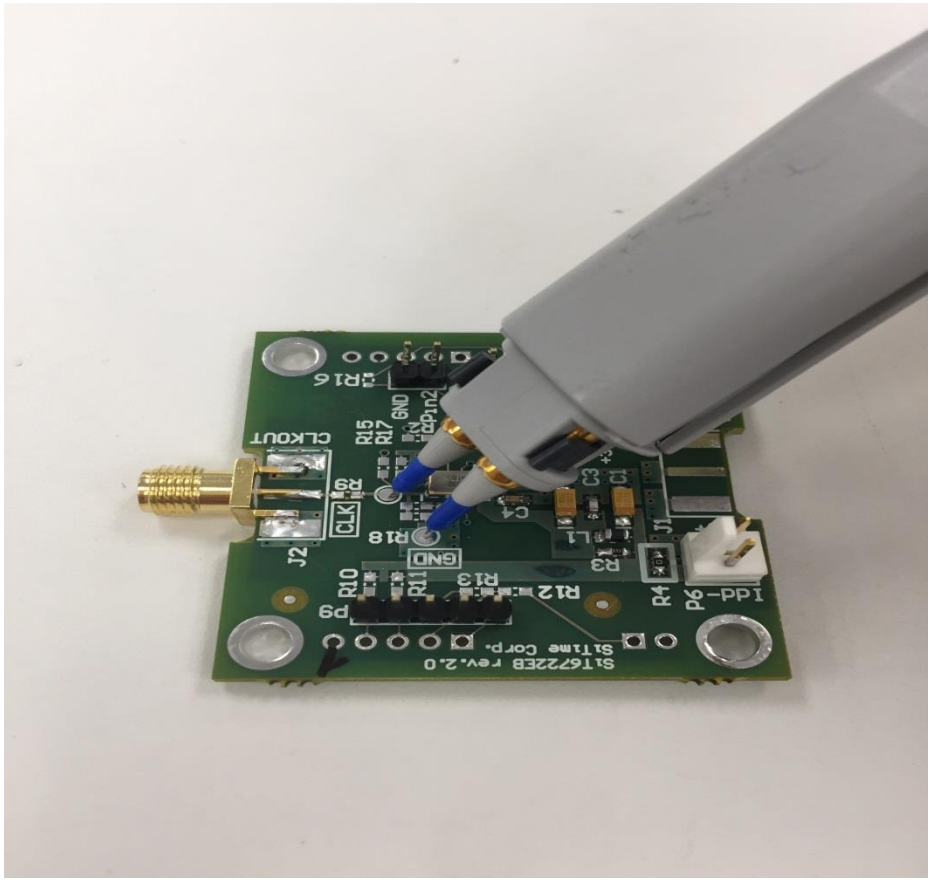

Figure 1: Proper Waveform capturing on SiT6722EB

3.3 Measuring Jitter and Phase Noise

For jitter measurements, make sure that SMA connector and source termination resistor R9 are properly soldered on the EVB. R9 value should be 25Ω for best source matching (refer to SiTime AN10002 for more information). The R9 can be populated using one of the following options:

1) 0Ω resistor. This allows DC coupling the output to 50Ω instruments directly. Note that due to 50Ω loading, the signal swing levels and rise/fall times will be different from those specified in the datasheet.
2) 0.1uF capacitor for AC-coupling to 50Ω instruments.

SMA connector is used to connect directly to the jitter measurement instrument, such as Time Interval Analyzer (TIA) or high-bandwidth real-time oscilloscope. Jitter measurement technique is described in SiTime AN10007.

The SMA can also be connected through 50Ω coaxial cable to signal source analysers or spectrum analysers to measure phase noise. In such case the use of AC-coupling configuration is recommended because not all measurement instruments can accept DC voltage at their inputs.

3.4 Current Measurement

To measure the current, remove zero-ohm resistor R4, and connect the DMM or other current measuring device across this connector. It is recommended to measure the voltage on DUT VDD and adjust for any drop on the DMM to ensure known VDD voltage on the device.

Appendix A: EVB Schematic, BOM and Layout

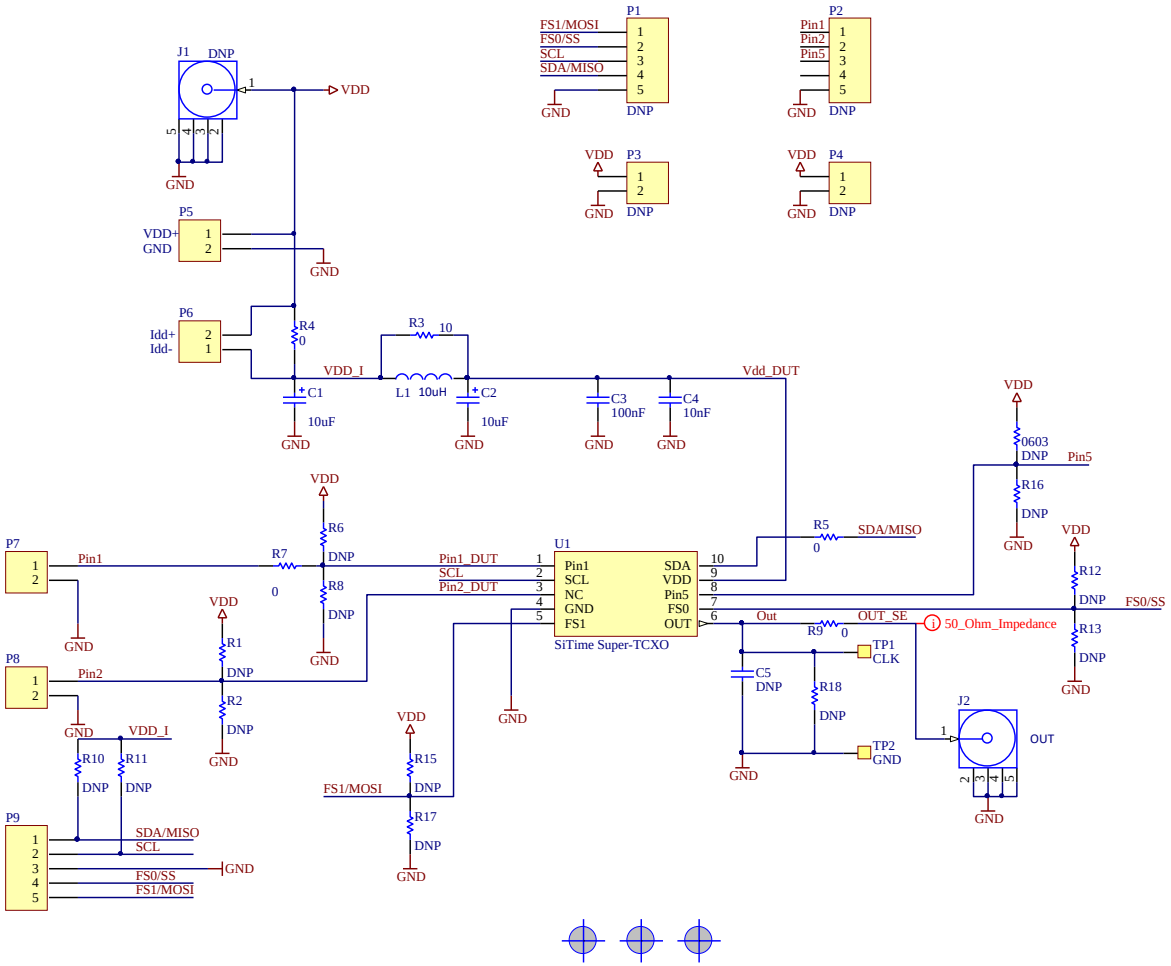

Figure A1: SiT6722EB EVB Electrical schematics

Table A1: Bill of Materials (BOM)

#	Reference Designators	Description	Qty	SMD component size	Value
1	C1, C2	Capacitors	2	Case A	10uF
2	C3	Capacitor	1	0603	0.1uF
3	C4	Capacitor	1	0603	0.01uF
4	C5	Capacitor	1	0603	15pF
5	R3	Resistors	1	0603	10 Ω
6	R4, R7, R5	Resistor	2	0603	0 Ω
8	R6, R8, R10, R11, R15, R17	Resistors	6	0603	4.7K
10	R18	Resistors	1	0603	51
11	R9	Resistor	1	0603	0 Ω or 24 Ω
12	L1	Inductor	1	0805	10mH
14	J1, J2	SMA connector	1	-	-
15	P1, P2, P9	5-pin header	3	-	-
16	P3, P4, P7	2-pin header	3	-	-
17	P5, P6	2-pin connector	2	-	-

Table A2: Connectors Digi-Key Part Number

Connectors	Digi-Key part number	Digi-Key part number for mating connector	Digi-Key part number for associated products
Power	WM2744-ND ARFX1231-ND 732-5334-ND	WM2011-ND	WM1114-ND
Pin 1 access	732-5334-ND	-	-
Frequency control via I^2C	732-5334-ND	-	-
OUT	ARFX1231-ND	-	-
Current Measurement	WM2744-ND	WM2011-ND	WM1114-ND

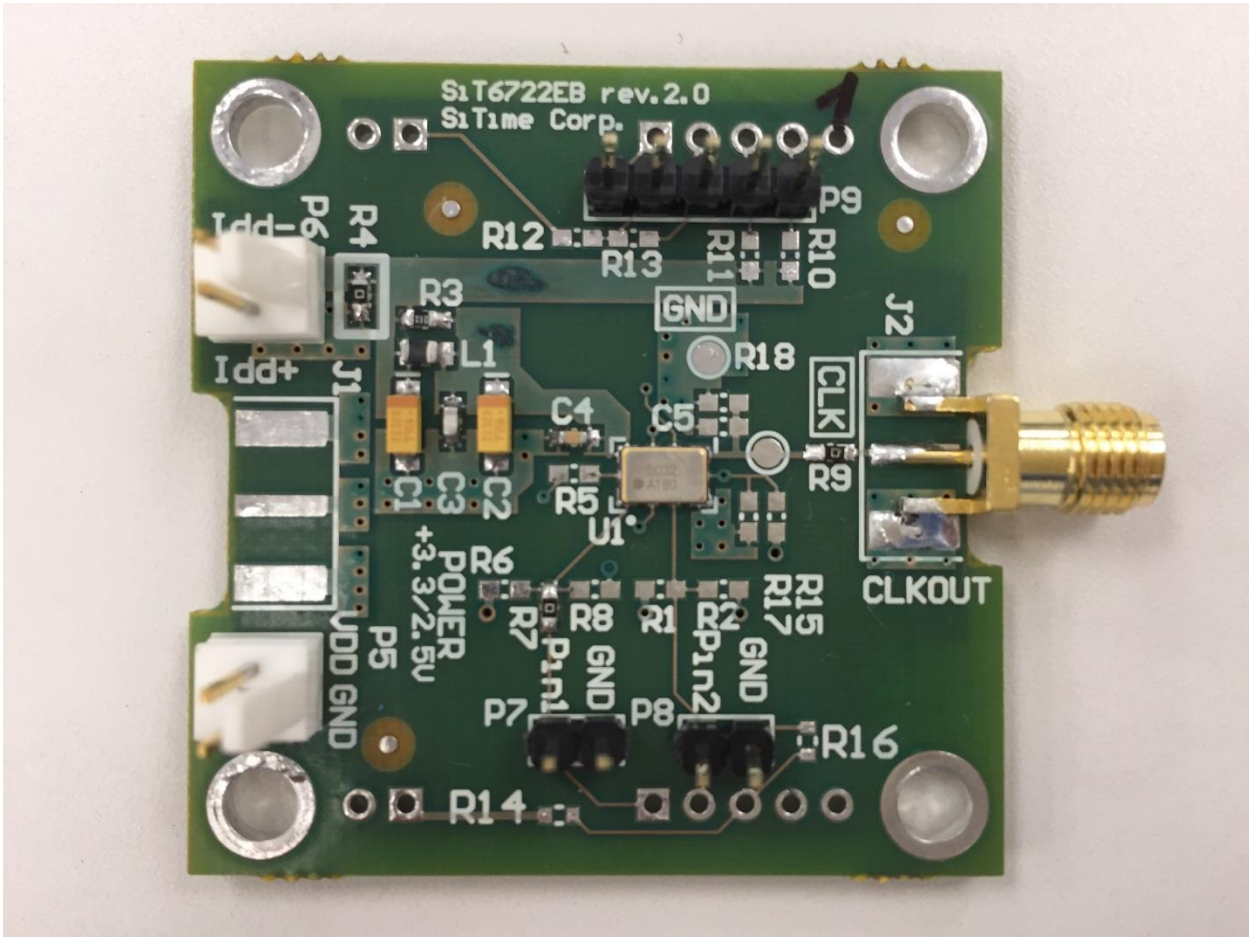

Figure A2: SiT6722EB EVB

Table 1: Revision History

Version	Release Date	Change Summary
1.01	30-Mar-2018	Initial Release
2.01	30-Jun-2019	Changed according to rev.2.0 board design
2.02	30-Jan-2023	Template update

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439