SiT6722EBBC Evaluation Board User Manual

Contents

1 Introduction

The SiT6722EBBC evaluation board (EVB) is designed for use with SiTime's Elite Super-TCXOs in the 10-pin, 5.0 x 3.2 mm x mm ceramic packages and Clipped Sinewave output type. It enables the evaluation of key functionalities of these precision Super-TCXOs in three configuration modes: TCXO, VCTCXO and DCTCXO with I²C.

The SiT6722EBBC supports 5.0 x 3.2 mm x mm package size including the following products:

Base Part Number	Type	Output frequency	Package
SiT5155	Super-TCXO	10 MHz – 40 MHz	5.0 x 3.2 CQFN
SiT5156	Super-TCXO	1 MHz – 60 MHz	5.0 x 3.2 CQFN
SiT5356	Super-TCXO	1 MHz – 60 MHz	5.0 x 3.2 CQFN
SiT5358	Super-TCXO	1 MHz – 60 MHz	5.0 x 3.2 CQFN
SiT5186	Automotive Super-TCXO	1 MHz – 60 MHz	5.0 x 3.2 CQFN
SiT5386	Automotive Super-TCXO	1 MHz – 60 MHz	5.0 x 3.2 CQFN
SiT5146	Ruggedized Super-TCXO	1 MHz – 60 MHz	5.0 x 3.2 CQFN
SiT5346	Ruggedized Super-TCXO	1 MHz – 60 MHz	5.0 x 3.2 CQFN
SiT5348	Ruggedized Super-TCXO	1 MHz – 60 MHz	5.0 x 3.2 CQFN

EVB Features

- Support for three Super-TCXO configuration modes: TCXO, VCTCXO, DCTCXO
- SMA output for direct or buffered connection to measurement equipment
- Probing points for accurate waveform measurement
- Connector access for controlling the output frequency via I^2C

SiTime typically ships the EVB with the Super-TCXO mounted using SiTime recommended reflow profile. The Super-TCXO device should only be evaluated in its original soldered down state for best signal integrity and frequency stability. The device performance is not guaranteed if it is de-soldered and then re-soldered either manually or via reflow process.

2 I/O Descriptions

Table 1: SiT6722EBBC I/O

Connector designator	I/O	Description
P1	**Power Supply and Sense**	Four-pin connector for DC power supply and power sensing. **VDD is connected to Pin 1, GND – to Pin2 of P1.** **VDD sense is connected to Pin 4, GND – to Pin3 of P1.**
P2	**Buffer power**	Two-pin connector for DC buffer power supply. **It is recommended to provide separate power to the buffer for best performance. 1.8 V supply required for buffer stable operation.**
P3	**Buffer power supply jumper**	A two-pin header (P3) provides access to using a jumper for buffer power supply configuration: • Without jumper (default shipment configuration) buffer is powered by the P2 connector. • With jumper buffer is powered by the DUT power supply P1 connector (not recommended for best phase noise measurement).
P4	**Frequency control via I^2C**	A four-pin header (P4) provides access to I^2C (SDA, SCL, A0).
P5	**Pin 1 access**	A two-pin header (P5) provides access to the pin 1 of the Super- TCXO in OE mode. In OE mode, pin 1 can be left floating as there is an internal pull-up resistor.
J1	**Output**	Oscillator output can be accessed either using active probe or SMA connector. The test points for active probe are placed closely to the oscillator output for better signal integrity (see Figure A2). Section 3.2 describes in details the recommended measurement configurations.

3 EVB Usage Descriptions

3.1 EVB Configurations

SiT6722EBBC can be configured to support three Super-TCXO configuration modes including TCXO with output enable (OE), VCTCXO with analog voltage control and DCTCXO with I^2C.

Oscillator output waveform can be measured with an active probe in all configurations. The value of the load capacitor C11 can be adjusted to match the load conditions in the target application. This enables the user to measure waveform characteristics under similar conditions as close to those on the target board as possible.

Oscillator output can be accessed in several ways listed in Table 1.

Table 2 describes components configuration to support all output configurations.

Table 2: Components configuration to support all output configurations

Output configuration	C11	R21	R17	C14	R10	R11	R14	C12	R15	C13	R16	R13
Direct	DNP	DNP	0.1 uF/ 0 Ω	DNP	DNP	DNP	0 Ω	DNP	0 Ω	DNP	0 Ω	DNP
Buffered output	DNP	DNP	0 Ω	0.1 uF	20 kΩ	20 kΩ	DNP	DNP	DNP	DNP	DNP	0 Ω
Probe	10 pF*	10 kΩ*	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP

* The value of the load capacitor C11 and load resistor R21 can be adjusted to match the load conditions in the target application. This enables the user to measure waveform characteristics under similar conditions as close to those on the target board as possible.

The test points for active probe are placed closely to the oscillator output for better signal integrity (see Figure A2).

Figure A1 in Appendix A shows the complete electrical schematic of SiT6722EBBC. Components labeled "DNP" are not assembled.

Shipment Configuration

SiT6722EBBC is shipped configured for buffered output allowing connecting it to the instrument input using 50 Ω coax cable. Details on the board assembly for shipment configuration can be found on the schematic (see Figure A1 in Appendix A).

3.1.1 I²C Support

The two pull up resistors (R1 and R2 with 4.7 kΩ value) can be assembled to support the I²C configuration (in case I²C master does not have it). If requested, the EVB will ship with these resistors.

3.2 Waveform Capturing Using Active Probe

SiTime Elite Super-TCXO is a high-speed logic output device. It is critical that the proper logic and high frequency measurement techniques are used along with the high-quality active probe to ensure best measurement results.

SiTime recommends the following minimum equipment for proper clock waveform measurement

1) 4 GHz or higher active probe with capacitance <1 pF, such as a Keysight 1134B;
2) Oscilloscope with 4 GHz bandwidth or higher such as a Keysight DSA90604A.

A passive voltage probe should not be used as it adds a high capacitive load to the part and the long ground lead clip is not suitable for high frequency measurement applications. The inductance of the long ground lead coupled with the input capacitance of the probe results in a resonant circuit. The consequence of this resonance results in the distortion of the clock signal. Typical manifestations of this distortion include ringing, overshoot, and undershoot of the clock signal.

Eliminating such distortion requires a probe with the lowest input capacitance and a low inductance ground lead. In addition, SiTime TCXOs are typically configured for fast rise and fall times with 15 pF load. It is therefore critical that the probe tip ground be as short as possible, lowest inductance, and the return path for the ground be located as close as possible to the trace carrying the RF logic signal.

For waveform measurement, it's recommended to remove resistor R17. Please refer to Figure A2 for test point locations on the SiT6722EBBC. If the soldering probe is used, it is recommended to use R21 resistor pads or solder it over it if necessary (Figure 1).

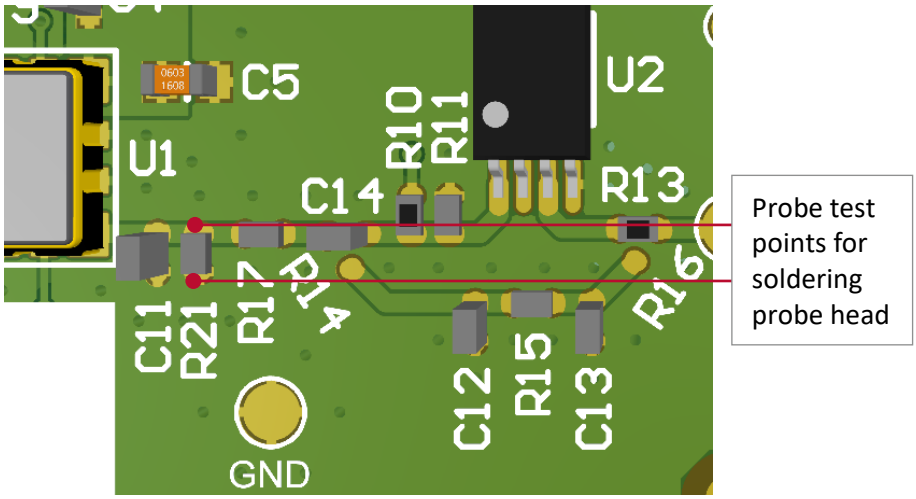

Figure 1: Recommended points for soldering probe head

More details on the SiTime recommendations on the oscillator's output probing can be found in AN10028.

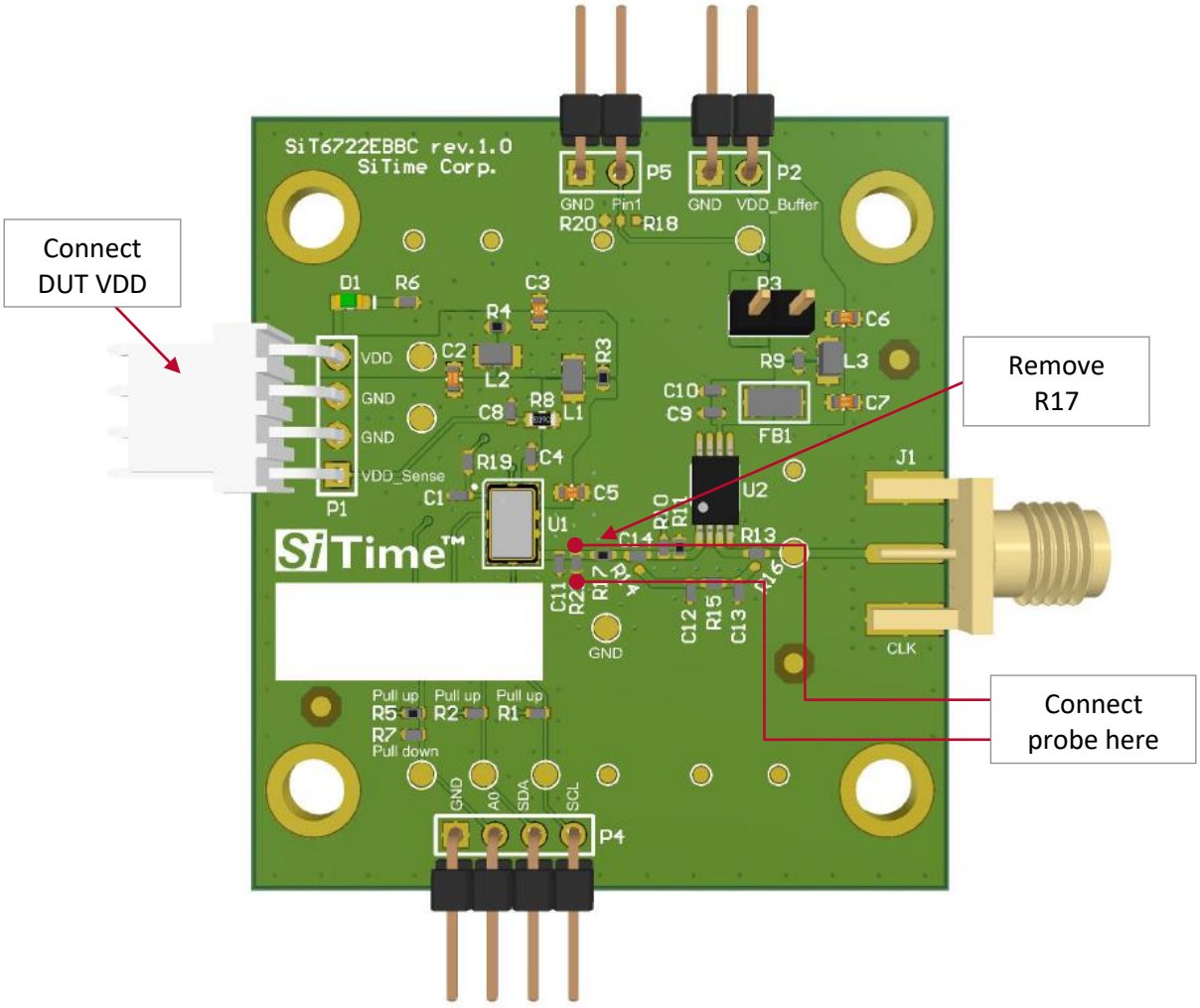

Figure 2: Signal measurement using probe

3.3 Measuring Jitter and Phase Noise

For jitter and phase noise measurements, buffered output configuration is recommended. SiTime TCXO was not designed to drive 50 Ω load directly so buffer avoids excessive current draw from the device output. For minimal impact on the measurement LMK1C1102 low-additive jitter buffer is used on the board.

SMA connector is used to connect directly to the jitter measurement instrument, such as Time Interval Analyzer (TIA) or high-bandwidth real-time oscilloscope. Jitter measurement technique is described in SiTime AN10007.

The SMA can also be connected through 50 Ω coaxial cable to signal source analyzers or spectrum analyzers to measure phase noise. In such case the use of AC-coupling configuration is recommended because not all measurement instruments can accept DC voltage at their inputs.

Note: It is highly recommended to use separate supply for the LMK1C1102 buffer for best phase noise and jitter measurement to avoid negative impact on TCXO supply from high-speed, high magnitude current draw of buffer into the 50 Ω load.

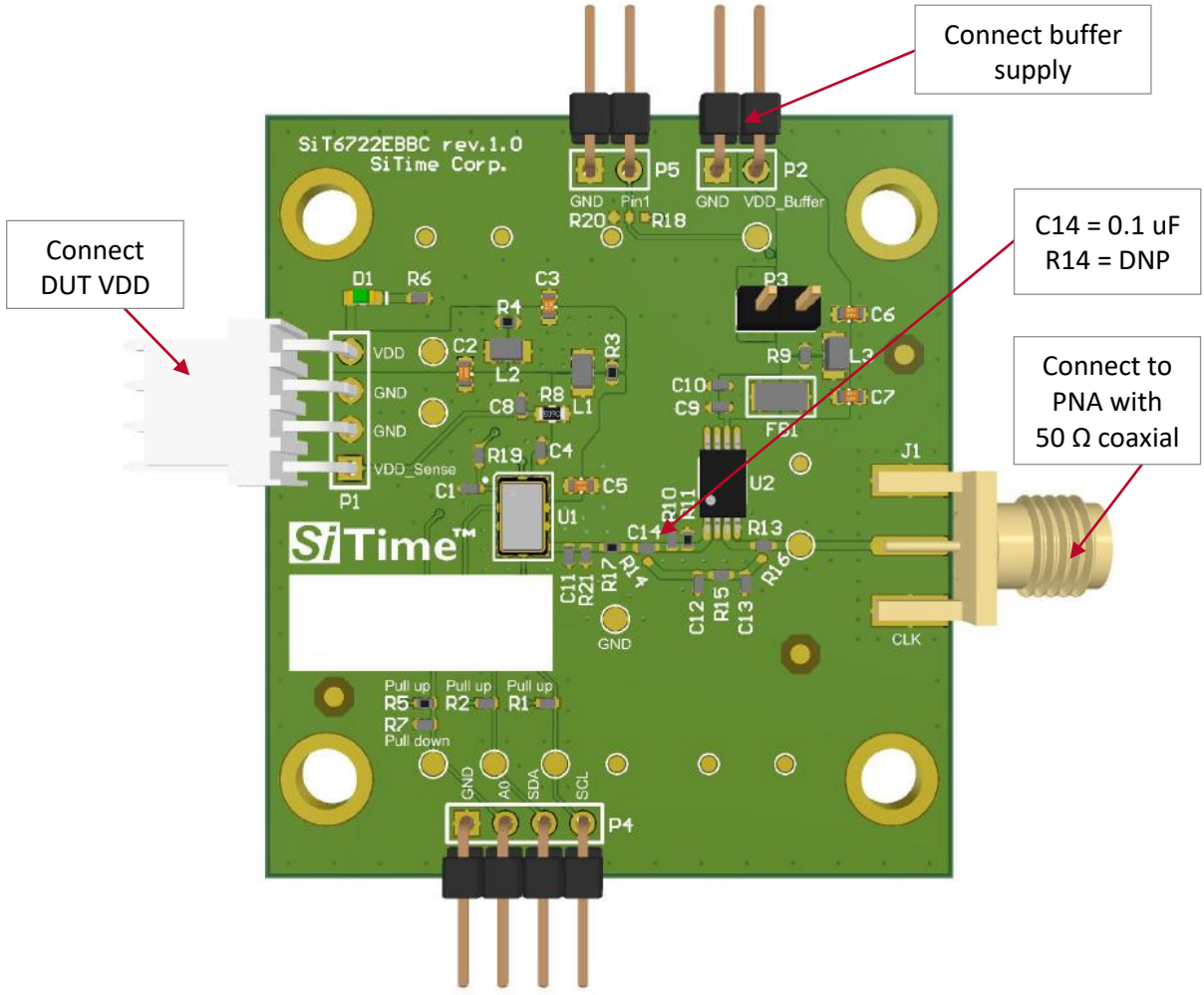

Figure 3: Phase noise measurement using buffer

3.4 Current Measurement

To measure the current consumption, user need to use ammeter/multi-meter in the power supply circuit. We recommend removing diode D1 to avoid measuring the additional current of the diode circuit. It is recommended to measure the voltage on DUT VDD and adjust for any drop on the DMM to ensure known VDD voltage on the device. VDD adjustment must be completed before every current measurement.

Appendix A

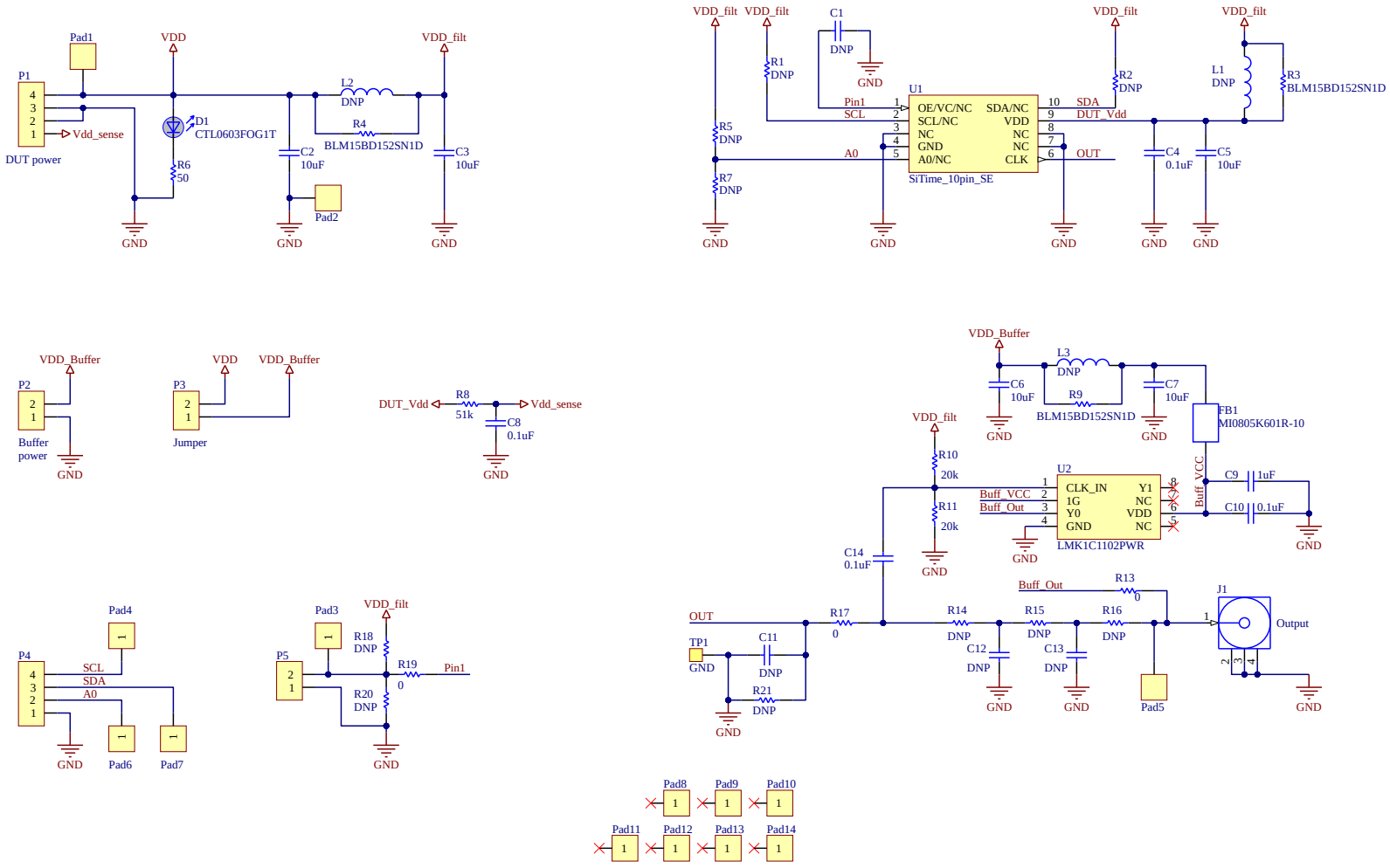

Figure A1: SiT6722EBBC electrical schematics

Table A1: Bill of Materials (BOM)

#	Reference Designators	Description	Qty	SMD component size	Value
1	C1, C11, C12, C13	Capacitors	4	0402	DNP
2	C2, C3, C5, C6, C7	Capacitors	5	0603	10 uF
3	C4, C8, C10, C14	Capacitors	4	0402	0.1 uF
4	C9	Capacitor	1	0402	1 uF
5	D1	LED	1	0603	Green
6	FB1	Ferrite bead	1	0805	600 Ω @ 100 MHz
7	L1, L2, L3	Inductance	3	0805	DNP
8	R13, R17, R19	Resistors	3	0402	0 Ω
9	R1, R2, R5, R7, R14, R15, R16, R18, R20, R21	Resistors	10	0402	DNP
10	R3, R4, R9	Ferrite Beads	3	0402	1.5 kΩ @ 100 MHz
11	R6	Resistor	1	0402	50 Ω
12	R8	Resistor	1	0603	51 kΩ
13	R10, R11	Resistors	2	0402	20 kΩ
14	U2	Buffer	1	TSSOP8-TI	LMK1C1102
15	P1	4-pin header	1	-	-
16	P2, P3, P5	2-pin headers	3	-	-
17	P4	4-pin header	1	-	-
18	J1	SMA connector	1	-	-

Table A2: Connectors Digi-Key Part Number

Connectors	Digi-Key part number	Digi-Key part number for mating connector	Digi-Key part number for associated products
Power/Power adjust	WM10299-ND	WM2002-ND	WM1114TR-ND
Buffer power	WM10297-ND	WM2011-ND	-
Buffer power supply jumper	Z5275-ND	-	S9342-ND
Frequency control via I^2C	2057-PH1RB-04-UA-ND	-	-

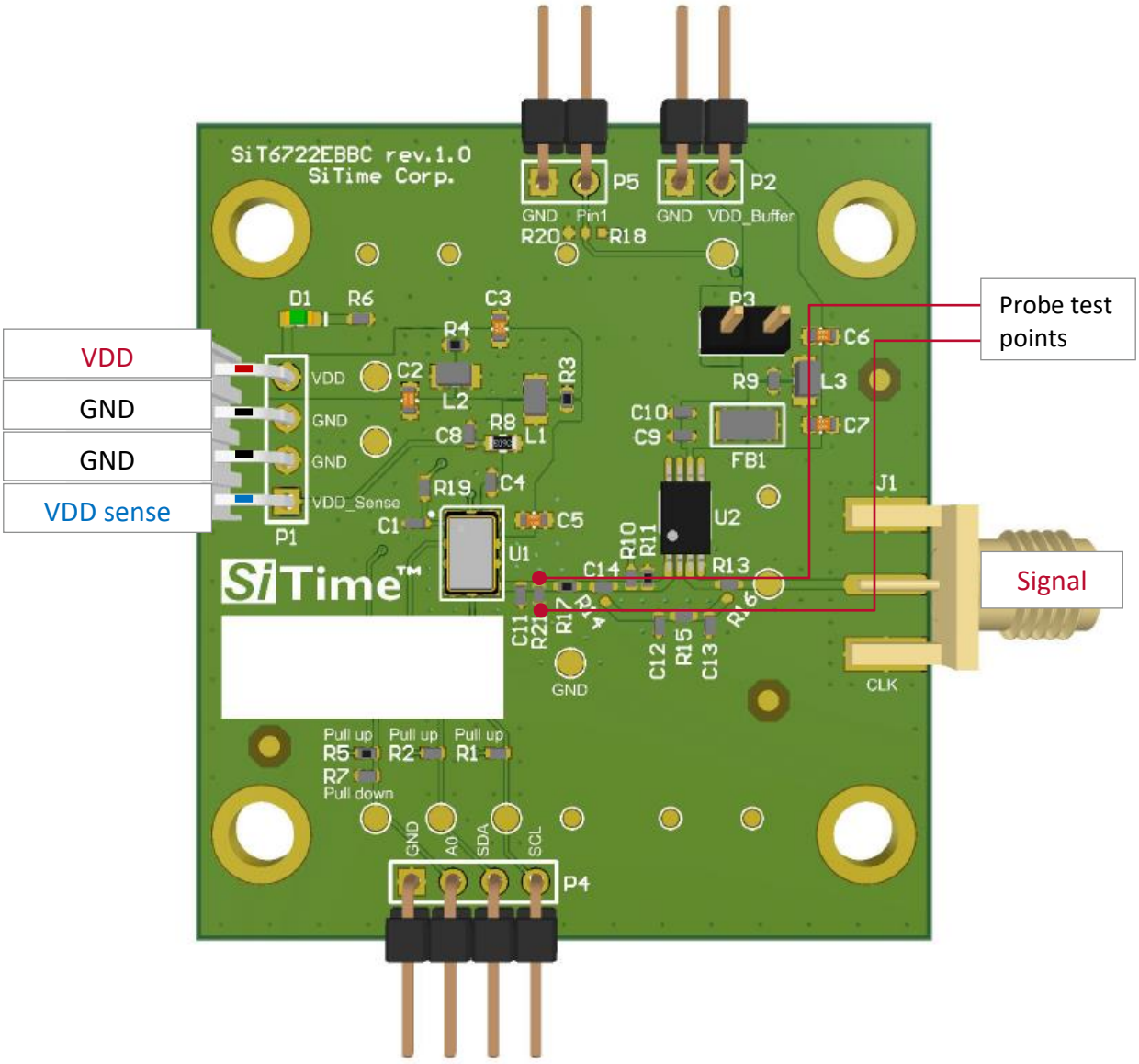

Figure A2: SiT6722EBBC layout

Table 3: Revision History

Version	Release Date	Change Summary
1.0	29-Sep-2023	Original doc
1.1	30-Apr-2024	Modified table with supported products
1.2	29-Nov-2024	Updated power filters on schematic and BOM Updated document format

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