SiT6701DM Demo Board User Manual

Contents

1 Introduction

The SiT6701DM is a PC-controlled demonstration board designed for evaluating SiTime Elite Platform™ I^2C/SPI programmable oscillators (SiT3521/2) that support differential signaling outputs in the 5.0 x 3.2 mm 10-pin QFN package. It enables the user to evaluate all aspects of the I^2C/SPI programmable devices including signal integrity, phase noise, phase jitter, output frequency re-programming and pulling via I^2C/SPI interfaces. The SiT6701DM board has a USB interface for connecting to the PC. The board is powered through the USB by default, but it can be configured to accept an external +5-V supply. TimeMaster™ clock configurator software is provided for controlling the board.

2 SiT6701DM Package

Table 1: The SiT6701DM rev.1.01 shipment package includes:

Item	Photo
SiT6701DM rev.1.01	

3 SiT6701DM Configurations

SiT6701DM ships with the pre-configured to default configuration SiT3521/2 device on it. Configurations available for SiT6701DM order are listed in Table 2.

Table 2: SiT6701DM Configurations

Ordering Code	Description
SiT6701DM-SiT3521AI-1C1-33-AB-156.250000	SiT6701DM with pre-configured SiT3521AI-1C1-33-AB-156.250000 LVPECL device
SiT6701DM-SiT3521AI-2C1-33-AB-156.250000	SiT6701DM with pre-configured SiT3521AI-2C1-33-AB-156.250000 LVDS device
SiT6701DM-SiT3521AI-4C1-33-AB-156.250000	SiT6701DM with pre-configured SiT3521AI-4C1-33-AB-156.250000 HCSL device
SiT6701DM-SiT3522AI-1C1-33-AB-491.520000	SiT6701DM with pre-configured SiT3522AI-1C1-33-AB-491.520000 LVPECL device
SiT6701DM-SiT3522AI-2C1-33-AB-491.520000	SiT6701DM with pre-configured SiT3522AI-2C1-33-AB-491.520000 LVDS device
SiT6701DM-SiT3522AI-4C1-33-AB-491.520000	SiT6701DM with pre-configured SiT3522AI-4C1-33-AB-491.520000 HCSL device

4 Board Features and Connections

The SiT6701DM board supports the following features:

- Support for SiT3521 (1 MHz to 340 MHz) and SiT3522 (340 MHz to 725 MHz) I^2C/SPI programmable oscillators
- Probing points for output frequency measurements
    - Support for LVPECL, LVDS, and HCSL output signal types

  - Support for waveform measurements
  - Support for phase noise and phase jitter measurements
- PC control through USB interface (USB Micro B connector) and TimeMaster software
- USB power or external +5V power (resistor configurable)
- Device power configuration: +2.5V/+3.3V
- I^2C communication with SiTime devices

External connections for the SiT6701DM are listed in Table 3. Refer to Figure 1 for board top view and Figure A1 in Appendix A for the SiT6701DM schematics.

Table 3: SiT6701DM I/O

I/O	Description
USB	USB Micro B connector for connection to the PC. By default board is powered through this connector.
External Power	A two-pin connector (P3) for DC power supply to the SiT6701DM board. Pin's polarity is identified on the silkscreen pattern near the connector (see Figure 1). Nominal voltage required is +5V.
VBIAS	A three-pin connector (P4) is available for supplying bias voltage. See Section 5.1 for detailed information on different termination schemes. A third pin is intended for Vbias sensing.
OUT+ and OUT-	OUT+ and OUT- are connected to the frequency output of the I^2C/SPI programmable device. The output should be measured using either the high-impedance, high-bandwidth active probe or via the SMA connectors (J3 and J4). Section 5.1 describes in detail the recommended measurement configurations.

Note: Pin 1 location of the device o is indicated by a chamfer in the silkscreen pattern around the device footprint.

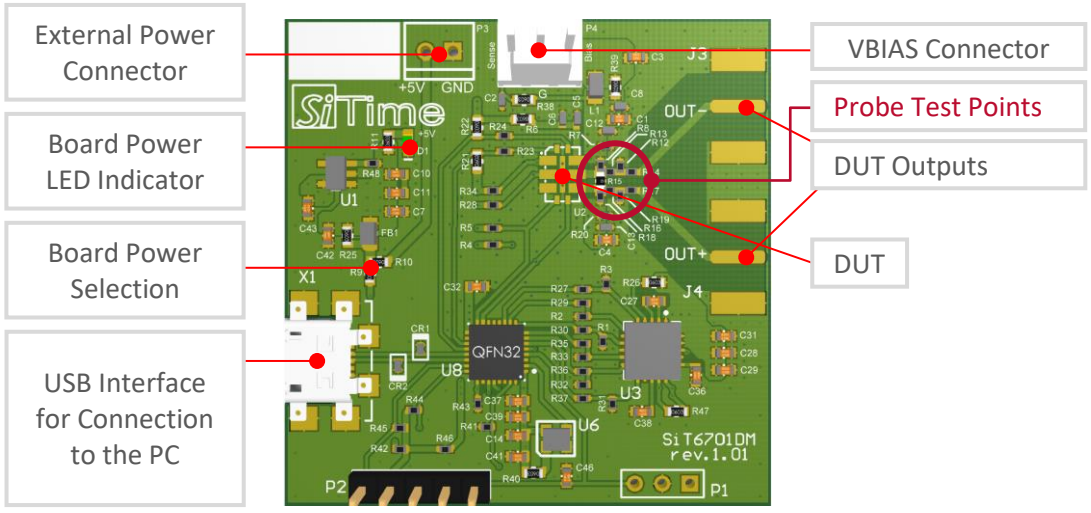


Figure 1: SiT6701DM top view and connections

Table 4: Power options

Power Option	R9	R10	Comment
USB (default)	0 Ω	Do not stuff	Board is powered from USB
External	Do not stuff	0 Ω	Board is powered from external supply connected to P3

Note that not all components shown in the schematics are populated for all configurations of the board. Specifically:

- Any components with assigned nominal values are used in all configurations of the board
- Any components without assigned nominal values are populated only for a specific configuration of board where these parts are needed

Any components labeled “DNP” are not populated on the EVB and are reserved for SiTime internal use only.

5 SiT6701DM Usage Description

5.1 Output Termination Configurations

The SiT6701EB supports multiple configurations for different signaling types of SiTime differential oscillators by using different component loading options.

5.1.1 LVPECL, Standard Termination, Active Probe

In this configuration, the LVPECL outputs are terminated to Vbias = VDD – 2V with 50-Ω resistors (R8 and R18). A high speed active probe, as shown on Figure 2, is placed on the termination resistor pads which are on the OUT+ and OUT- traces. Figure 2 shows the termination scheme for this configuration.

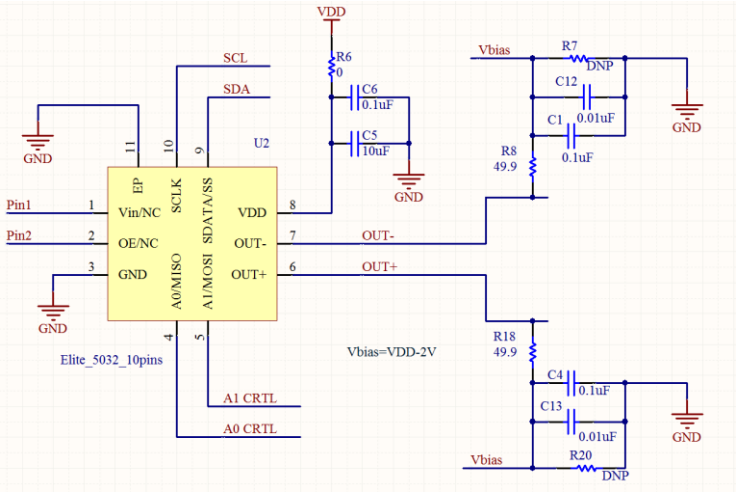


Figure 2: LVPECL output termination with 50Ω to Vbias and measurement using high impedance and high bandwidth active probe

5.1.2 LVPECL, AC-coupling Configuration, Direct to Instrument

This is default shipment configuration for evaluation boards with LVPECL devices.

This configuration allows LVPECL output connection to the measurement instrument using 50-Ω coaxial cables. Outputs are terminated with 150Ω/120Ω (R12 and R19 for 3.3V and 2.5V VDD respectively) to GND on the DUT side and connected to SMA connectors through 0.1-µF series capacitors (R14 and R17). Figure 3 shows the termination scheme for this configuration.

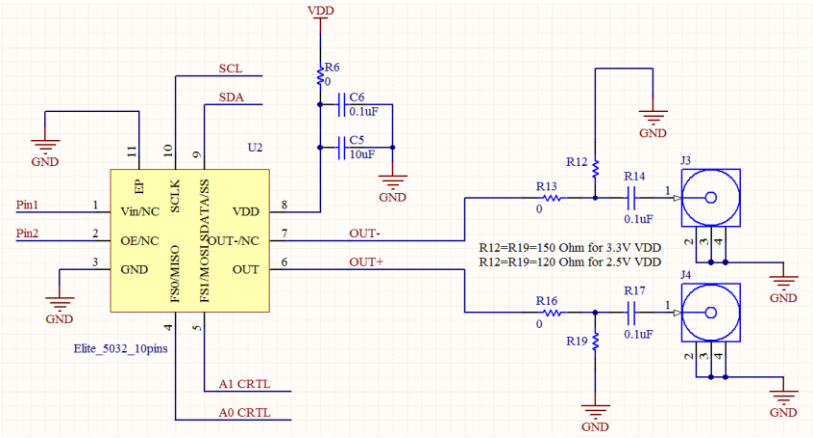


Figure 3: LVPECL output termination with 150 Ω/120 Ω to GND and measurement with AC-coupled connection to measurement instrument using 50 Ω SMA cables

5.1.3 LVPECL, Y-Termination, Active Probe

This configuration is intended for LVPECL output waveform parameters measurement using an active probe.

Figure 4 shows the termination scheme for this configuration. R20 is added to create DC voltage bias for OUT+ and OUT- with R18 (50Ω) and R8 (50Ω). R20 is 50Ω for 3.3V VDD and 18Ω for 2.5V VDD.

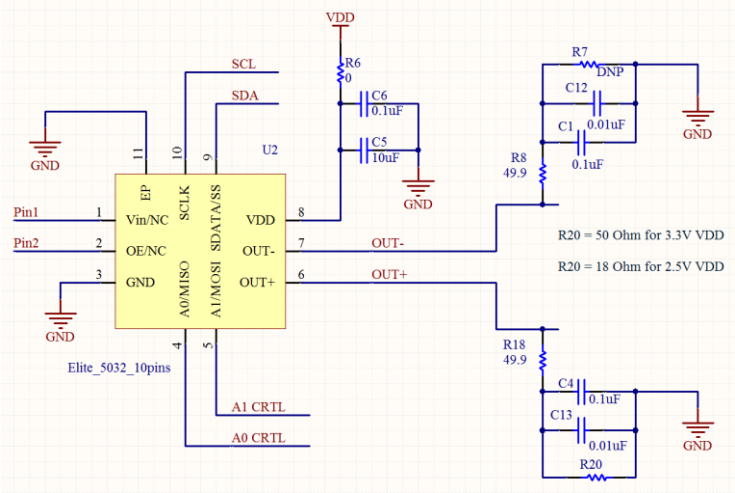


Figure 4: Y-termination scheme for LVPECL output termination for measurement using high impedance and high bandwidth active probe

5.1.4 LVDS, Standard Termination, Active Probe

This configuration is intended for LVDS output waveform parameters measurement using an active probe. A high speed active probe, as shown in Figure 4, is placed on the termination resistor pads which are on the OUT+ and OUT- traces.

Figure 5 shows differential impedance of 100Ω (R15) across OUT+ and OUT- for termination.

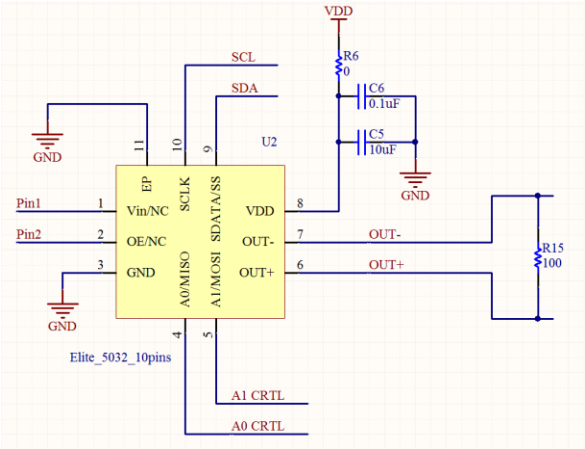


Figure 5: 100-Ω differential impedance across LVDS outputs for measurement using a high impedance and high bandwidth active probe

5.1.5 LVDS, AC-coupling Configuration, Direct to Instrument

This is default shipment configuration for evaluation boards with LVDS devices.

This configuration is useful for connecting LVDS outputs to 50-Ω input channels of the measurement instrument. The AC-coupling capacitors (R14 and R17) block the DC common mode voltage from the LVDS outputs to avoid DC current draw to the 50-Ω inputs. Figure 6 shows the termination scheme for this configuration.

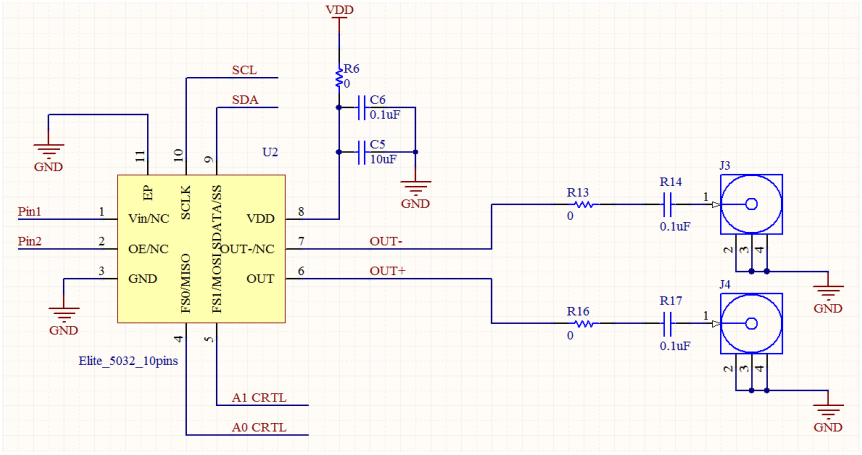


Figure 6: AC-coupled LVDS outputs are terminated by measurement instrument input 50-Ω impedance, equivalent 100Ω across OUT+ and OUT-

5.1.6 HCSL, Standard Termination, Active Probe

This configuration is intended for HCSL output waveform parameters measurement using an active probe. Output is terminated with 50Ω (R12 and R19) to GND. Series resistors R13 and R16 are used as overshoot limiter and should be in the range from 10Ω to 30Ω. A high speed active probe is placed on the termination resistor pads which are on the OUT+ and OUT- traces. Figure 7 shows the termination scheme for this configuration.

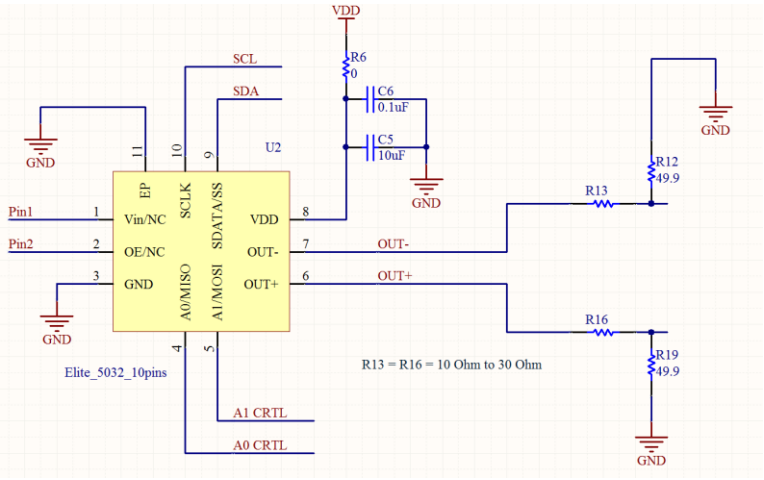


Figure 7: HCSL outputs terminated with 50Ω to GND through 10-Ω to 30-Ω series resistors for measurement using a high impedance and high bandwidth active probe

5.1.7 HCSL, Standard Termination, Direct to Instrument, DC Coupled

This is the default shipment configuration for evaluation boards with HCSL devices.

This configuration is intended for HCSL output waveform parameters measurement with a direct connection to the measurement instrument 50-Ω inputs.

Figure 8 shows the termination scheme for this configuration. Series resistors R13 and R16 are used as overshoot limiter and should be in the range of 10-Ω to 30-Ω. The connection to the instrument must be DC coupled.

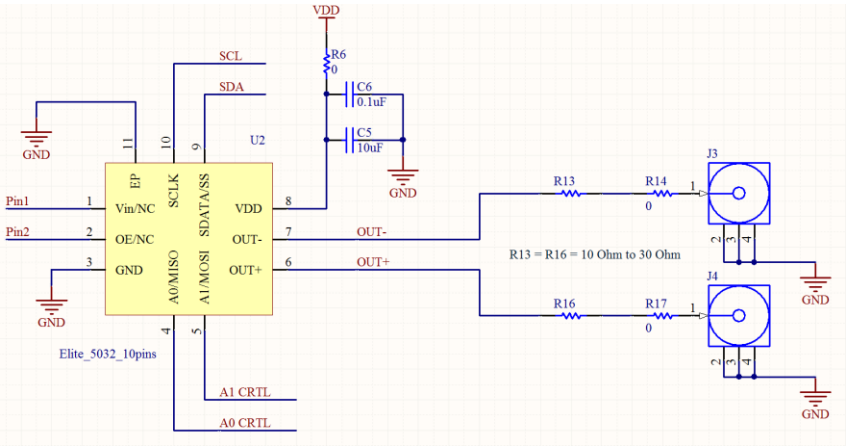


Figure 8: HCSL outputs terminated with 50 Ω to GND at measurement instrument side with 10 Ω to 30 Ω series resistors at source side

5.2 Waveform Measurement Using Active Probe

SiTime differential oscillators are high speed logic output devices with fast, sub-nanosecond rise/fall time. It is critical that the proper logic and high frequency measurement techniques are used along with the high quality active probe in order to ensure best measurement results.

SiTime recommends the following equipment for proper measurement of a differential clock waveform:

1) Differential active probe with >4GHz bandwidth, <1pF load capacitance, such as an Keysight 1134A, with high-speed differential probe heads, such as:
   a. Keysight E2675B differential browser
   b. Keysight N5381B solder-down probe tip
   c. Keysight N5425B/N5426A ZIF probe tip
2) Oscilloscope with 4GHz bandwidth or higher
3) Oscilloscope with 50 Ω inputs.

Refer to Figure 9 for a probing example of the board using an active probe.

Figure 9: Differential browser (high impedance active probe) on test points for waveform capturing on the SiT6701DM

5.3 Jitter Measurement

For jitter measurement, configurations described in 5.1.2 (LVPECL), 5.1.4 (LVDS), and 5.1.6 (HCSL) should be used. Jitter measurement technique is described in SiTime application note AN10007.

6 PC Connection and Clock Configurator Software

SiT6701DM connects to the PC with USB interface. TimeMaster software supplied with the board is compatible with Microsoft Windows-based systems: Windows 7 and Windows 10. After the connection, the board will be identified by the system automatically and the standard Windows drivers will be installed.

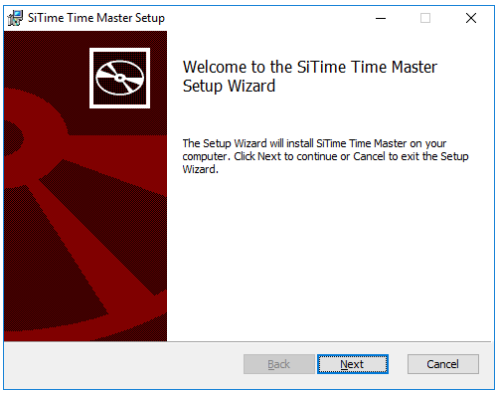
Note: TimeMaster software requires .NET Framework 4.5 or higher to be installed on the PC.

TimeMaster software can be downloaded from the SiTime web site.

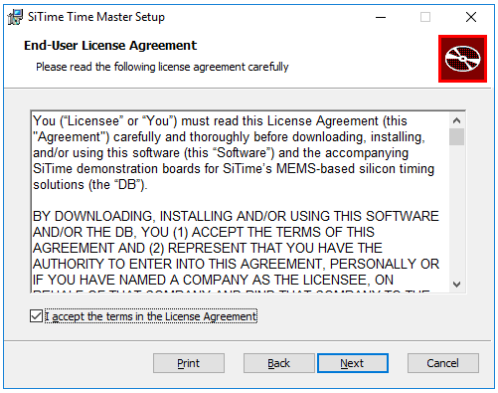
6.1 Software Installation

After the software is downloaded, the user needs to run TimeMaster_rev.1.0.msi and complete the following steps to finish installation:

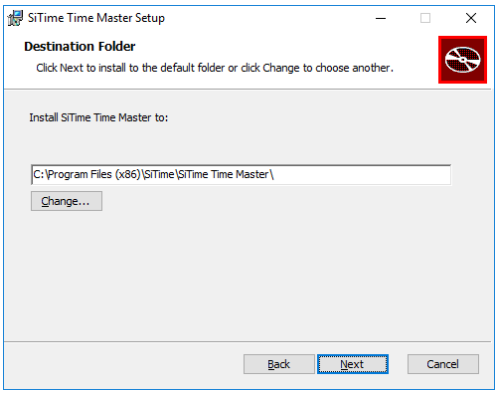
1. Click *Next* on the welcome window



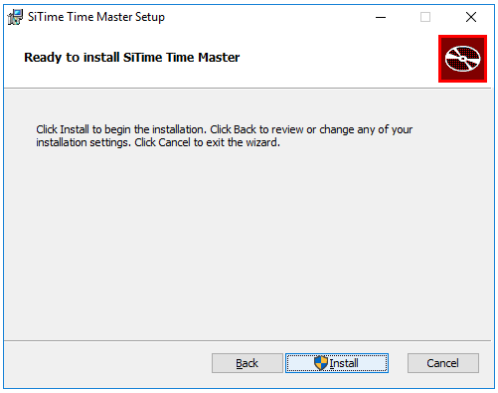
1. Select *I accept the terms in the License Agreement* and then click *Next*



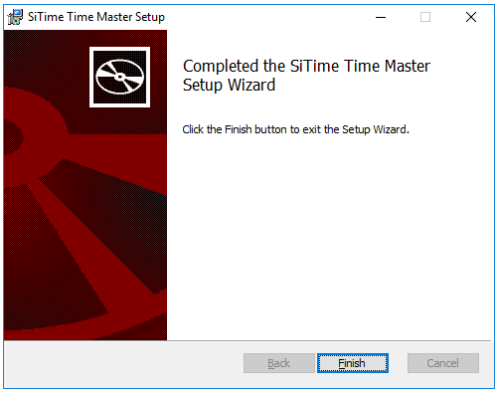
2. Select the destination folder and then click *Next*



3. Click *Install*



4. After the installation is complete, click *Finish* to close the installer window. Software installation will automatically add a shortcut on the desktop for quick software launch



6.2 Software Operation

There are two GUI startup flows that are supported:

1. **Start with the board disconnected from the PC**. GUI will start with the default look (see Figure 10) reporting that the board is disconnected. After the board is connected the user should go to menu *SystemCheck->Initialize* to initialize the system.
2. **Start with the board connected to the PC.** Software will ask to enter device options on startup (see Figure 12). Similar window is shown for the previous case after the board is connected and system initialization is launched.

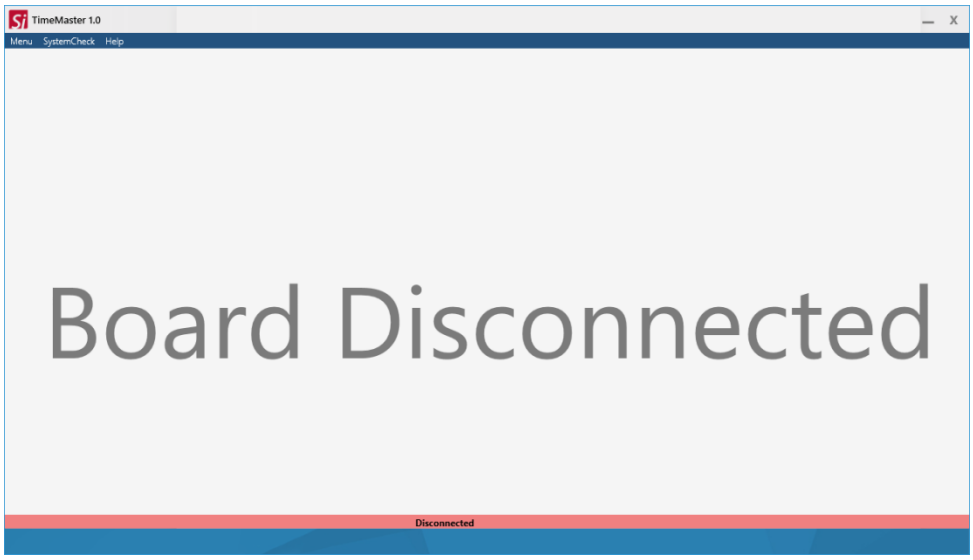


Figure 10: Startup GUI appearance when the board is disconnected

The software with start with the window shown on Figure 11 and the following options should be specified to initialize the GUI:

1. Signaling type:
    a. Select signaling type and press *Next*
2. Supply voltage:
    a. Select supply voltage and press *Configure Device*

Important note: The software does not automatically detect the output signaling type so it is important to select the correct item in the *Signaling Type* menu. If the wrong signaling type is selected, the driver settings may be programmed incorrectly during the features evaluation which will result in an incorrect output waveform.

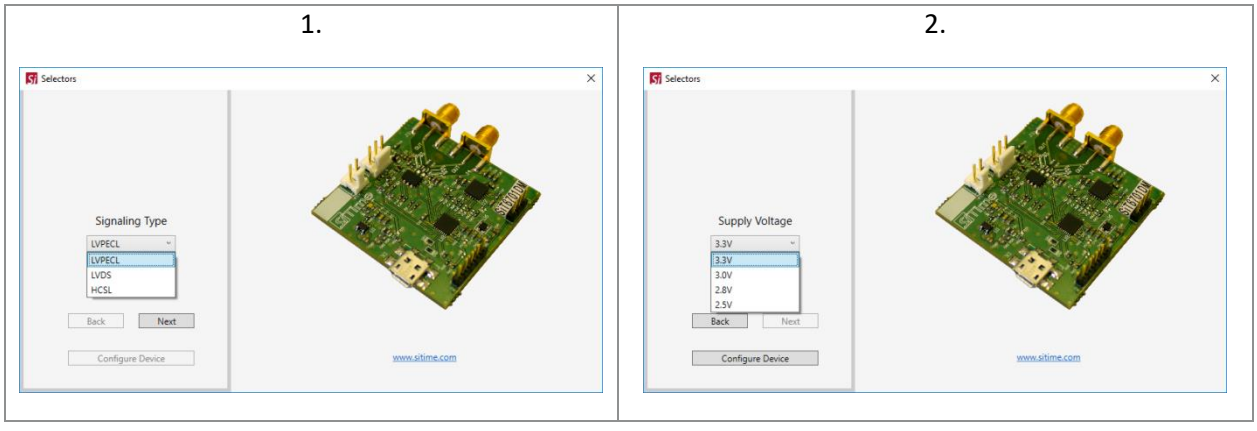


Figure 11: Device options selection window

Once all options are selected, the GUI will start the main window showing the board connection status (see Figure 12). The main GUI shows simplified block diagram of the device with frequency programming, DCO, and output enable blocks accessible by the user. Frequency and pull range values are displayed on the startup window and represent the current state of the DUT.

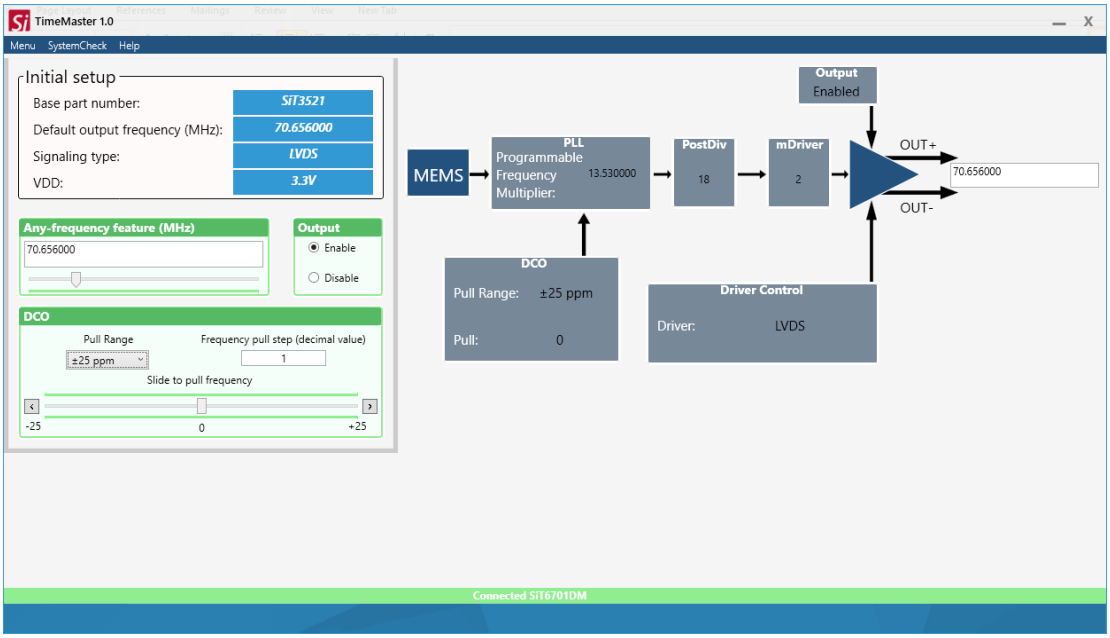


Figure 12: Startup GUI appearance when board is connected

The controls enclosed in the green-colored blocks located on the left side of the GUI represent the user-accessible features of the SiTime device:

1. Any-frequency programming:
    a. New frequency value in the range of 1 MHz to 340 MHz / 340 MHz to 725 MHz (for SiT3521/2 respectively, upper frequency limit for HCSL driver is 500 MHz) can be entered in edit box

    > **Important note:** Frequencies in the range from 300.6 MHz to 307.499 MHz and 601.201 MHz to 614.999 MHz are not supported.

    b. Frequency value can be changed by swiping slider under the edit box
2. DCO pull range and frequency pull change:
    a. Frequency pull range from 25 ppm to 3200 ppm can be selected from the drop down menu
    b. Frequency pull can be changed by swiping the slider or clicking on the buttons located to the left and right sides of slider
    c. Step field defines the slider and button sensitivity. Step defines increment/decrement value of the frequency control word written to the device (Refer to section 8.2 of the datasheet for the details)
3. OE control
    a. Sends a command to enable/disable output to the device

Note: After new device frequency or new pull range is selected, the software automatically changes DCO frequency pull to 0.

The diagram located on the right side of the GUI shows simplified block diagrams with current values for the main blocks impacting output frequency. The text box near the output driver represents nominal value of frequency calculated based on the frequency, pull range, and frequency pull range values entered in the controls on the left side.

Note: If no evaluation board with a SiTime device is connected to the SiT6701DM board or any mistake is made when selecting device options, the GUI will display the error message shown in Figure 13. In this case GUI re-initialization is required after connecting the evaluation board (menu *SystemCheck→Initialize*).

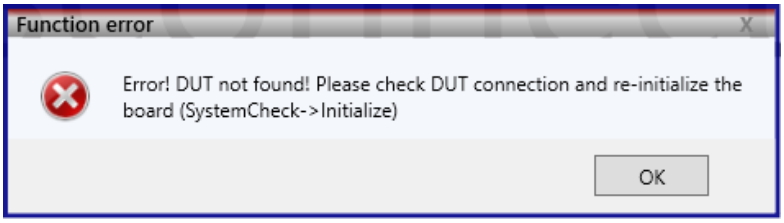
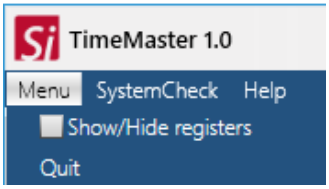


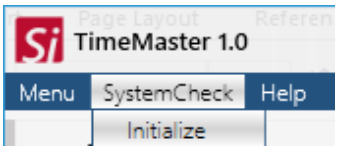
Figure 13: Error window reporting that device is not found

Menu options:

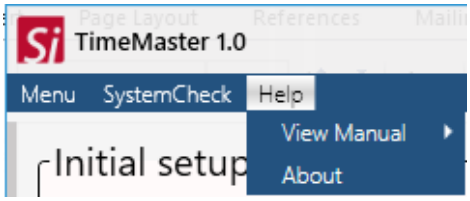
1. *Menu* tab:
    a. Checkbox: displays the SiTime device register contents
    b. *Quit:* exits the GUI



2. *SystemCheck* tab:
    a. *Initialize*: initializes the GUI. Initialization has to be run if:
        1. the board has been connected after the GUI start up
        2. the board was disconnected
        3. any mistake was made when selecting device options



3. *Help* tab:
    a. *View Manual*: opens user manual
    b. *About*: shows information about software and connected hardware



Appendix A

Figure A1: SiT6701DM rev. 1.01 schematic

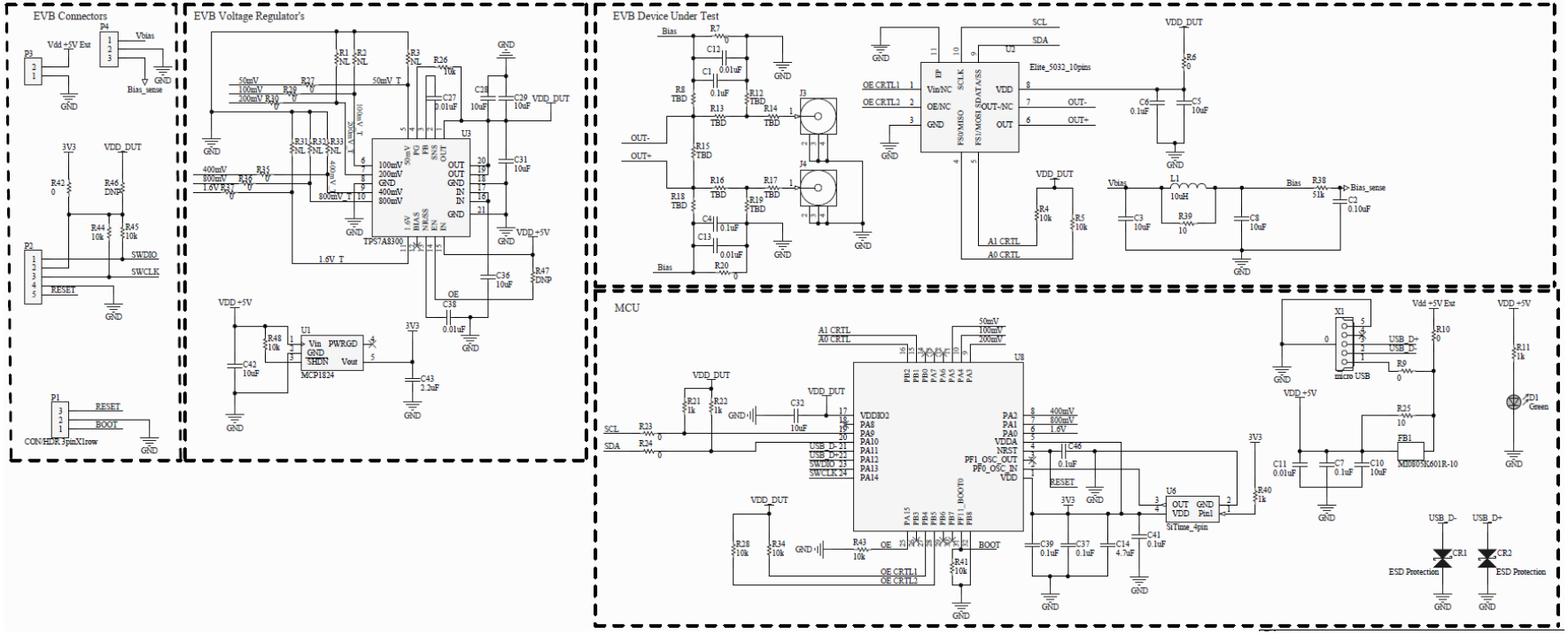


Table A1: Bill of Materials (BOM)

#	Reference Designators	Description	Qty	SMD component size	Value
1	R6, R9, R10	Resistor	3	0603	0Ω
2	R4, R5, R28, R34, R41, R43, R44, R45, R48	Resistor	9	0402	10 kΩ
3	R7, R20, R23, R24, R27, R29, R30, R35, R36, R37, R42	Resistor	11	0402	0Ω
4	R11, R21, R22, R40	Resistor	4	0603	1 kΩ
5	R26	Resistor	1	0603	10 kΩ
6	R8, R12, R13, R14, R16, R17, R18, R19	Resistor	8	0402	See Figure 1~8 for values
7	R1, R2, R3, R31, R32, R33, R46	Resistor	7	0402	Not populated
8	R15	Resistor	1	0603	See Figure 1~8 for values
9	R25, R39	Resistor	2	0603	10Ω
10	R38	Resistor	1	0603	51 kΩ
11	R47	Resistor	1	0603	Not populated
12	U1	300 mA, low voltage, low quiescent current LDO regulator	1	SOT23-5	MCP1824
13	U2	SiTime oscillator	1	10-Pin 5.0 x 3.2 mm	-
14	U3	LDO voltage regulator	1	RGW (S-PVQFN-N20)	TPS7A8300
15	U6	SiTime 4-pin standard SE oscillator	1	4-pin 2.5 x 2.0 mm	-

16	U8	ARM MCU	1	UFQFPN32	STM32F042
17	X1	Molex Cut In Micro USB Connector Type B	1	USB Micro B	Micro USB
18	L1	Inductor	1	0805	10 µH
19	C1, C4, C7, C37, C39, C41, C46	Ceramic capacitor	7	0603	0.1 µF
20	C2	Ceramic capacitor	1	0402	0.10 µF
21	C3, C10, C28, C29, C31, C32, C36, C42	Ceramic capacitor	8	0603	10 µF
22	C5, C8	Ceramic capacitor	2	0402	10 µF
23	C6	Ceramic capacitor	1	0402	0.1 µF
24	C11, C27, C38	Ceramic capacitor	3	0603	0.01 µF
25	C12, C13	Ceramic capacitor	2	0402	0.01 µF
26	C14	Ceramic capacitor	1	0603	4.7 µF
27	C43	Ceramic capacitor	1	0603	2.2 µF
28	CR1, CR2	ESD bidirectional protection diode	2	SOD882	PESD5V0U1BL
29	D1	Green LED diode	1	0603	CMD17-21VGD
30	FB1	Ferrite bite	1	0805	MI0805K601R-10
31	J3, J4	SMA connectors	2	SMA edge mount	SD-73251-115
32	P1	3-Pin Connector	1	Header 1x3 2.54 mm pitch	3-641215-3
33	P2	5-Pin Connector	1	Header 1x5 2.54 mm pitch	4-103185-0
34	P3	2-Pin Connector	1	Connector 1x2 2.54 mm pitch	3-641215-2
35	P4	3-Pin Connector	1	Connector 1x3 2.54 mm pitch	3-641215-3

Table A2: Digi-Key Part Numbers for Connectors

Connectors	Digi-Key part number	Digi-Key part number for mating connector	Digi-Key part number for associated products
USB	WM17142CT-ND	-	993-1070-ND 993-1294-ND
External Power	A30786-ND	A99613-ND	A100453CT-ND
Vbias	WM2701-ND	WM2001-ND	WM1114-ND
Output	WM5534-ND	-	-

Table 5: Revision History

Version	Release Date	Change Summary
1.01	02/15/2019	Initial release

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439