SiT6520EB Evaluation Board User Manual

Contents

1 Introduction

The SiT6520EB evaluation board (EVB) is designed to assist users in evaluating programmable Chorus™ clock generators: SiT9121x and SiT9128x.

2 SiT6520EB Features

- Powered from USB port or external power supply
- 3x2 jumper blocks for VDDO, VDD and VDDA – select 1.8 V, 2.5 V, 3.3 V or external power supply status LEDs for USB power supply and GPIOs status signals
- Each of the 4 DIFF/8 SE outputs are accessible via edge mount high bandwidth SMA connectors
- Each output pair has AC couple option onboard
- Output termination options can be populated to support LVCMOS, HCSL, LPHCSL, LVDS and LVPECL

3 SiT6520EB Support Collateral

The SiT6520EB evaluation board is provided with the following collateral:

- SiT6520EB EVB User Manual

4 Connector Descriptions

Table 1 lists the SiT6520EB EVB connectors.

Table 1. SiT6520EB Connectors

Connector Designators	Description
Power + Control	USB Type C connectors (P3) for device programming and +5V supply
Power	3-pin Headers P4, 2-pin connectors (P2) for external +5V power supply
Outputs	SMA connectors (J1 through J8) for synthesized clock outputs
External +5V or USB power supply	3-pin Headers (P4), default USB selection
USB-C	USB-C Connector
Header for selection VDDA Ext or LDO	3-pin Headers (P25), default LDO selection
Header for selection VDDD Ext or LDO	3-pin Headers (P26), default LDO selection
Header for selection VDDO0 Ext or LDO	3-pin Headers (P19), default LDO selection

Connector Designators	Description
Header for selection VDDO1 Ext or LDO	3-pin Headers (P17), default LDO selection
Header for selection VDDO2 Ext or LDO	3-pin Headers (P20), default LDO selection
Header for selection VDDO3 Ext or LDO	3-pin Headers (P18), default LDO selection
Header for selecting the SiT6520EB I^2C or SPI	3-pin Header (P4)
Header for configuring the SiT6520EB into I^2C and SPI Mode (I^2C Mode is default one)	10-pin Header (P15)
GPIO0	3-pin Header (P12)
GPIO1	3-pin Header (P11)
GPIO2	3-pin Header (P10)
GPIO8	3-pin Header (P13)
GPIO9	3-pin Header (P14)
External Power sources Headers	2-pin Headers (P2, P5, P21, P22, P23, P24, P27 and P28)
Header for selection VDDA 1.8V, 2.5V or 3.3V	6-pin Headers (X6)
Header for selection VDDD 1.8V, 2.5V or 3.3V	6-pin Headers (X5)
Header for selection VDDO0 1.8V, 2.5V or 3.3V	6-pin Headers (X1)
Header for selection VDDO1 1.8V, 2.5V or 3.3V	6-pin Headers (X2)
Header for selection VDDO2 1.8V, 2.5V or 3.3V	6-pin Headers (X3)
Header for selection VDDO3 1.8V, 2.5V or 3.3V	6-pin Headers (X4)
Outputs Termination Header	2-pin Headers (P6, P7, P8, P19)

5 Jumper Default List

Table 2 lists the default positions of the jumpers on the EVB.

Table 2. Jumper Default List

Jumper Location	Type	I = Installed O = Open	Jumper Location	Type	I = Installed O = Open
P1	3-Pin	1 to 2	**P19**	3-Pin	1 to 2
P2	2-Pin	O	**P20**	3-Pin	1 to 2
P4	3-Pin	1 to 2	**P21**	2-Pin	O
P5	2-Pin	O	**P22**	2-Pin	O
P6	2-Pin	O	**P23**	2-Pin	O
P7	2-Pin	O	**P24**	2-Pin	O
P8	2-Pin	O	**P25**	3-Pin	1 to 2
P9	2-Pin	O	**P26**	3-Pin	1 to 2
P10	3-Pin	O	**P27**	2-Pin	O
P10	3-Pin	O	**P28**	2-Pin	O
P10	3-Pin	O	**X1**	3-Pin Dual row	O
P10	3-Pin	O	**X2**	3-Pin Dual row	O
P10	3-Pin	O	**X3**	3-Pin Dual row	O
P15	5-Pin, Dual row	5 to 6, 7 to 8	**X4**	3-Pin Dual row	O
P16	2-Pin	I	**X5**	3-Pin Dual row	O
P17	3-Pin	1 to 2	**X6**	3-Pin Dual row	O
P18	3-Pin	1 to 2			

6 Default Resistor Connection from FTDI to SiT9121x and SiT9128x

Table 3 lists the default resistor connection from FTDI to the SiT9512x device on the EVB.

Table 3. Default Resistor Connection from FTDI to DUT on the SiT6520EB

Signal name	Resistors	S = 0 ohm Short O = DNP
CLK_12M	R1	S
OUT3N	R20	S
OUT1N	R21	S
OUT3P	R31	S
OUT1P	R33	S
OUT2N	R34	S
OUT0P	R35	S
OUT2P	R42	S
OUT0N	R43	S
P6 CON 2pinX1row	R79	S
P7 CON 2pinX1row	R80	S
P8 CON 2pinX1row	R81	S
P9 CON 2pinX1row	R82	S

7 Status LEDs

Table 4 lists the Status LEDs on the SiT6520EB EVB shown in Figure 1.

Table 4. SiT6520EB Status LEDs

Location	Color	Status Function indication
D3	Orange	Main USB +5V present
D1-D6	Green	GPIOs

***Note:** All LEDs are illuminated when corresponding voltages are present.

Figure 1. Status LEDs

8 SiT6520EB Power Supply

The device under test (DUT) analog supply voltage (VDDIN) and DUT outputs supply voltages (VDDOx) on the SiT6520EB are configured to 3.3 V by default, whereas the DUT PLLs supply voltage (VDD) is configured to 1.8 V. The on-board supplies/LDOs are configurable to 1.8 V, 2.5 V and 3.3 V with the Jumper option as shown in Figure 2. Please refer to the SiT9121x and SiT9128x datasheets for configuring the supply voltages on the VDDA/VDD and VDDOx pins and to the Table 5 for on board configuration options:

Table 5. SiT6520EB Supply Configuration

Variant	VDD	VDDA	VDDOx
SiT9121x and SiT9128x	1.8 V / 2.5 V / 3.3 V	1.8 V / 2.5 V / 3.3 V	1.8 V / 2.5 V / 3.3 V

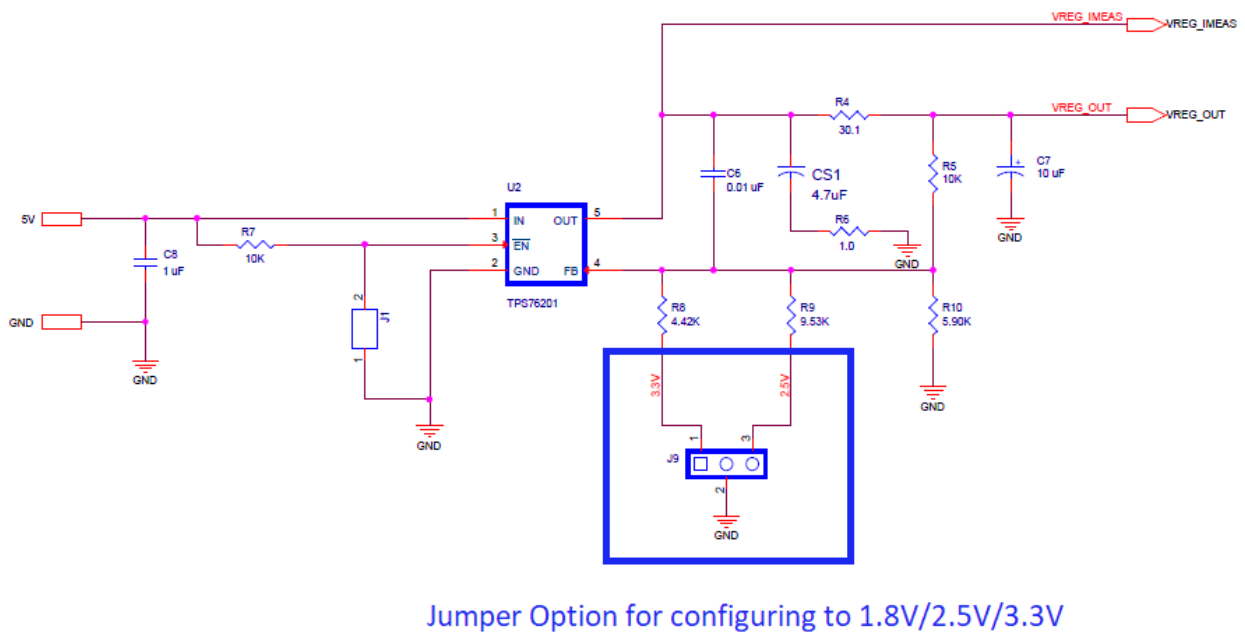


Figure 2. Supply Regulator for VDDIN/VDDOx

Note: For changing the VDDIN (J9) and VDDOx supply, connect the corresponding Jumpers to below settings:

1. 3.3 V - Connect the 3-Pin Jumper from 1 to 2.
2. 2.5 V - Connect the 3-Pin Jumper from 2 to 3.
3. 1.8 V - Remove the Jumper.

There is a provision for connecting external supplies after bypassing the on-board regulators for all the supplies as shown in Figure 3.

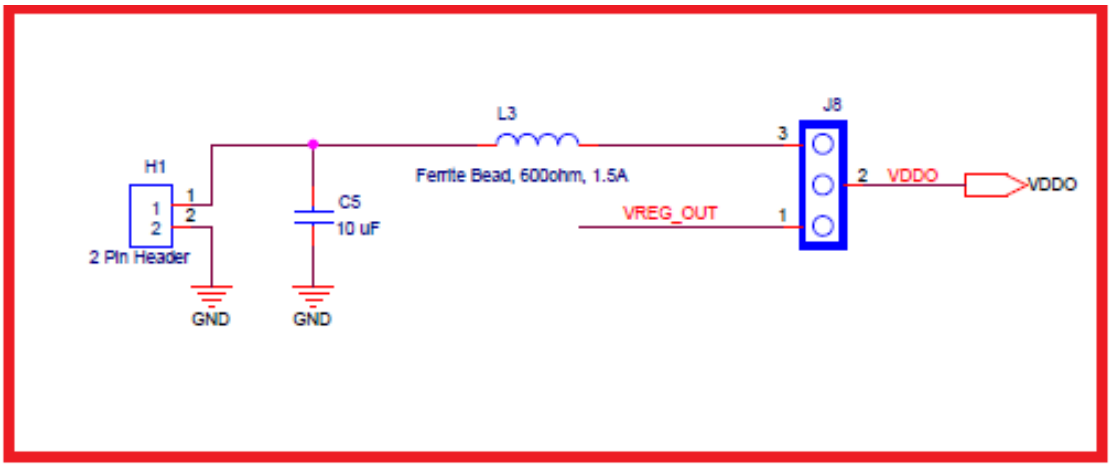


Figure 3. External Supply Connection Provision

PLLs supply circuitry is shown in Figure 4.

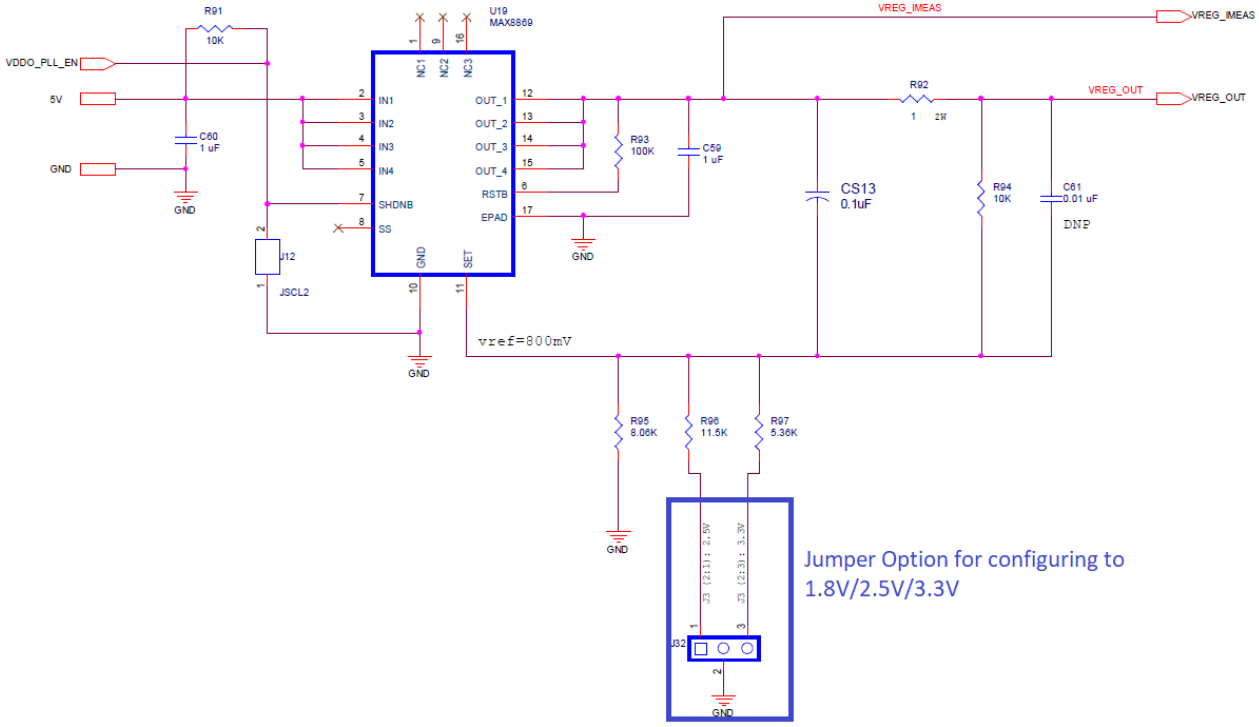


Figure 4. Supply Regulator for PLLs

Note: For changing the VDD (J32) supply, connect the Jumper to below settings:

1. 3.3 V - Connect the 3-Pin Jumper from 2 to 3.
2. 2.5 V - Connect the 3-Pin Jumper from 1 to 2.
3. 1.8 V - Remove the Jumper.

9 I²C/SPI Mode Connection

The 10 pin Header J76 (Figure 5) is mainly used for configuring the SiT6520EB into I²C and SPI mode. (I²C mode is the default mode)

For I²C Mode of Operation:

1. SCLK_OUT is shorted to SCLK in J76.
2. SDAIO_OUT is shorted to SDAIO in J76.
3. CSB_OUT is shorted to CSB in J76.

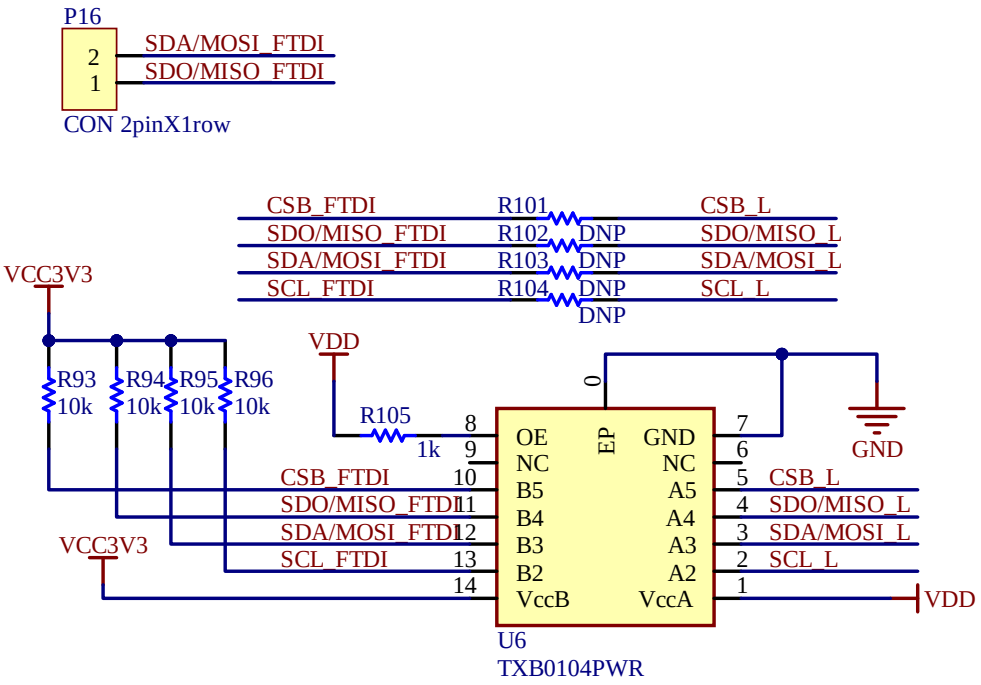


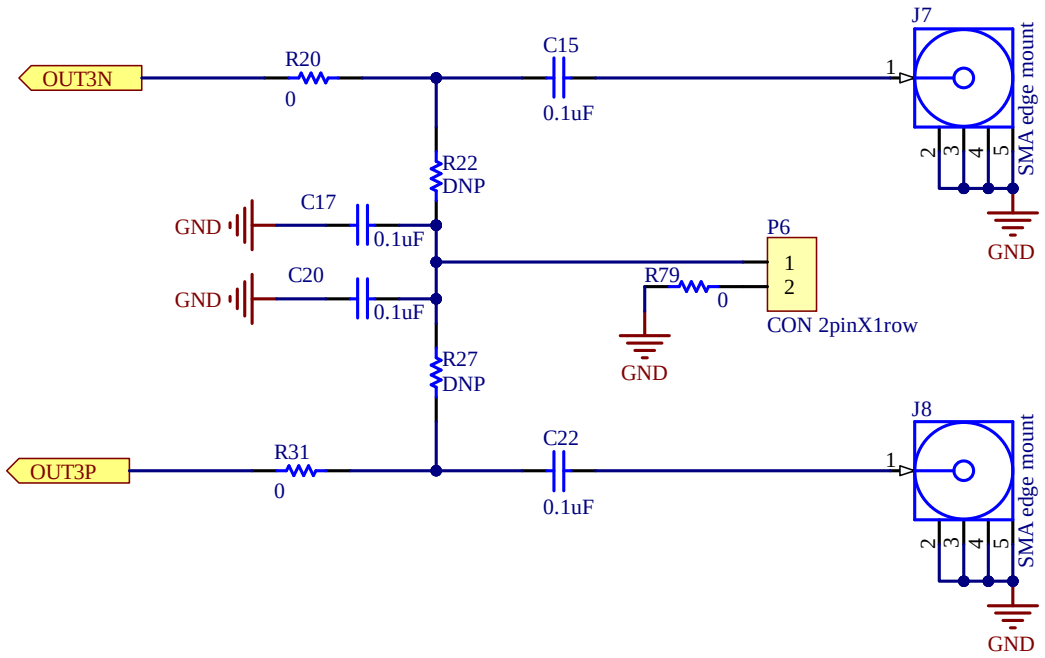
Figure 5. Supply Regulator for PLLs

For SPI Mode of Operation:

1. SCLK_OUT is shorted to SCLK in J76.
2. SDAIO_OUT is shorted to SDAIO in J76.
3. CSB_OUT is shorted to CSB in J76.
4. SDO_OUT is shorted to SDO in J76.
5. JSCL1 Jumper should be removed.
6. JVDD1 Jumper should be changed from (2 to 3) to (1 to 2).
7. J73 Jumper should be changed from (1 to 2) to (2 to 3).

10 Clock Outputs

When shipped from the factory, each of the twenty output drivers (10 differential pairs) is ac-coupled to its respective SMA connector. This is the default configuration. The output clock termination circuit is shown in Figure 6 below. If dc coupling is required, the corresponding 0.1 µF ac coupling capacitor can be replaced with a zero Ω resistor. Figure 6 shows the Output Clock Termination Circuit for one of the 10 output pairs.



Output Configuration	C15 C22	R20 R31	R22 R27	R79	Jumper P6
LVCMOS	0.1 uF	33 Ohm	DNP	0 Ohm	Open
LVDS	0.1 uF	0 Ohm	DNP	0 Ohm	Open
LVPECL	0.1 uF	0 Ohm	150 Oh	0 Ohm	Open
HSCL	0 Ohm	33 Ohm	50 Ohm	0 Ohm	GND
LVPECL Y-term	0.1 uF	0 Ohm	50 Ohm	50 Ohm	GND

Figure 6. Output Clock Termination Circuit

10.1 Output Differential Termination

LVDS (default configuration), LVPECL, HCSL, and LPHCSL differential signaling types can be supported by changing the output termination circuits.

10.1.1 LVDS, CML

The board is shipped to support LVDS, CML in its default differential. The signals are ac coupled with ceramic 0.1 µF capacitors instead of the corresponding series resistors RSExx (Refer to Table 6) which are not populated.

Table 6. Output Port RSExx Resistors

Output Port #	0	1	2	3	4	5	6	7	8	9	10
0.1 µF capacitors	RSE21 RSE22	RSE17 RSE19	RSE1 RSE5	RSE2 RSE6	RSE4 RSE7	RSE3 RSE8	RSE10 RSE14	RSE9 RSE13	RSE11 RSE15	RSE12 RSE16	RSE18 RSE20

Output termination resistors as shown in Table 7 are not populated.

Table 7. Output Port Not-Populated Resistors

Output Port #	0	1	2	3	4	5	6	7	8	9	10
Not Populated Resistors	**R176 R178**	**R143 R145**	**R113 R117**	**R114 R118**	**R115 R119**	**R116 R120**	**R129 R133**	**R130 R134**	**R131 R135**	**R132 R136**	**R144 R146**

10.1.2 LVPECL

For LVPECL output configuration, ceramic capacitors 0.1 µF are placed instead of correspondent series resistors RSExx (Refer to Table 6). Termination resistor values depending on the output driver VDD level are shown in Table 8.

Table 8. Output Port Termination Resistors for LVPECL

Output Port #	0	1	2	3	4	5	6	7	8	9	10
Resistors	R176 R178	R143 R145	R113 R117	R114 R118	R115 R119	R116 R120	R129 R133	R130 R134	R131 R135	R132 R136	R144 R146
VDD, 3.3V	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω
VDD, 2.5V	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω

Also, ensure that jumpers JSCLxx as per Table 9 are populated to allow a path to GND.

Table 9. Output Port Jumpers to GND

Output Port #	0	1	2	3	4	5	6	7	8	9	10
Jumpers to GND	JSCL23	JSCL21	JSCL13	JSCL14	JSCL15	JSAL16	JSCL17	JSCL18	JSCL19	JSCL20	JSCL22

10.1.3 HCSL

For HCSL output configuration, series resistors RSExx (Refer to Table 6). 33 Ω should be used for each output port. Please note each lane per pair should be terminated by 50 Ω to GND on the receiver side.

11 Quick Start

- Confirm jumpers are installed as shown in Table 2.
- Connect a USB cable from SiT6520EB, J3 to your PC.
- Default Output Driver Configuration is LVDS and Output Driver Supplies are configured to 3.3 V.
- Default VDD Supply on the EVB is configured to 1.8 V and default VDDIN supply on the EVB is configured to 3.3 V.
- The FTDI chip on the EVB is configured to I^2C as the default communication protocol.
- EVB default configuration is shown in Figure 7.

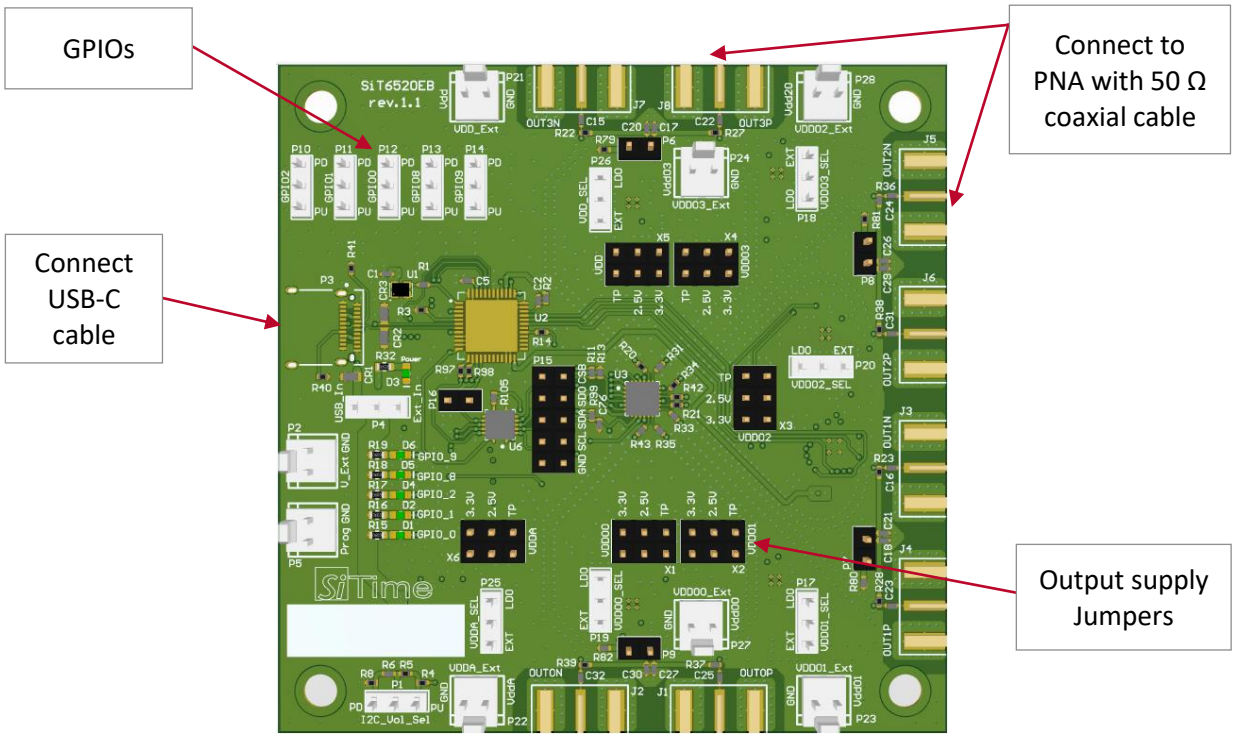


Figure 7. SiT6520EB Starter Connection Diagram

The general guidelines for single USB power supply operation are listed below:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA respectively at +5V
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤ 470 mA.
  Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5V drops gracefully by less than 10%, the EVB will still work

Appendix A: EVB Schematic Diagrams

EVB Top Level Diagram

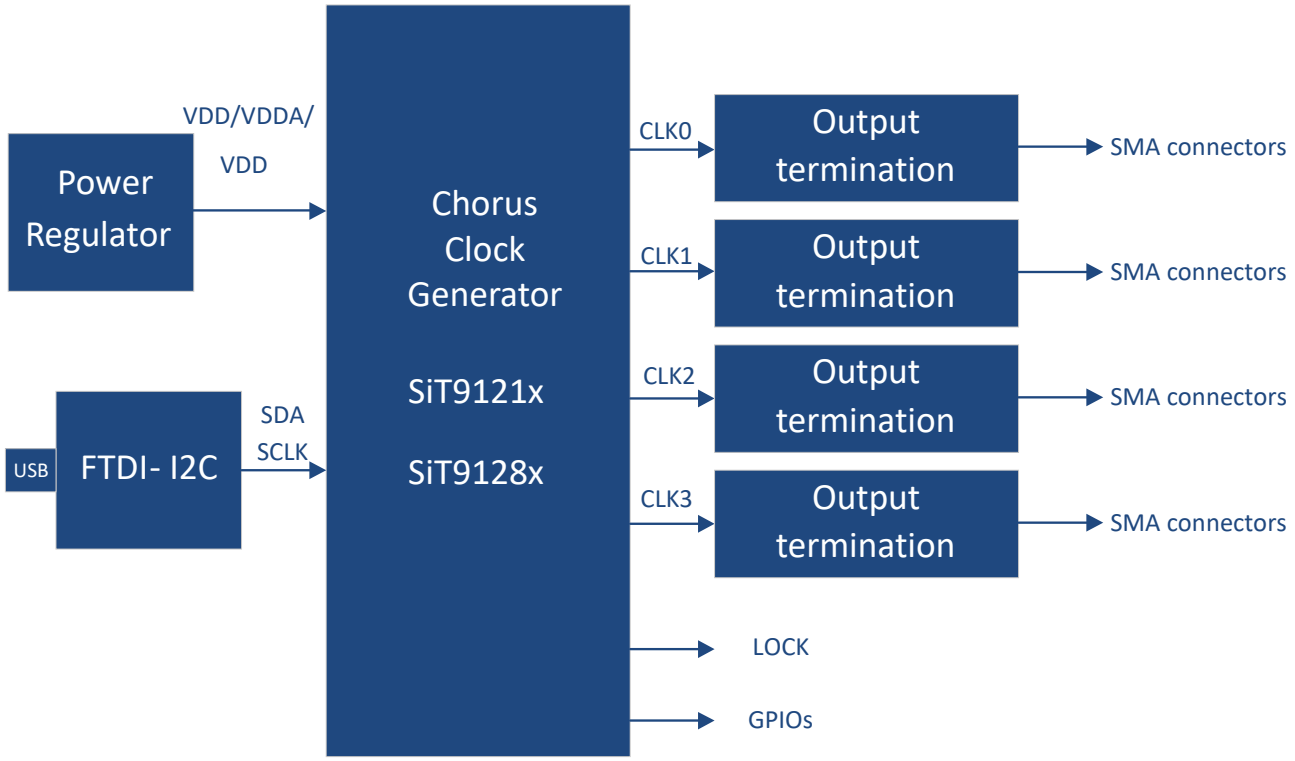


Figure A1. SiT6520EB Top Level Diagram

Power Supply

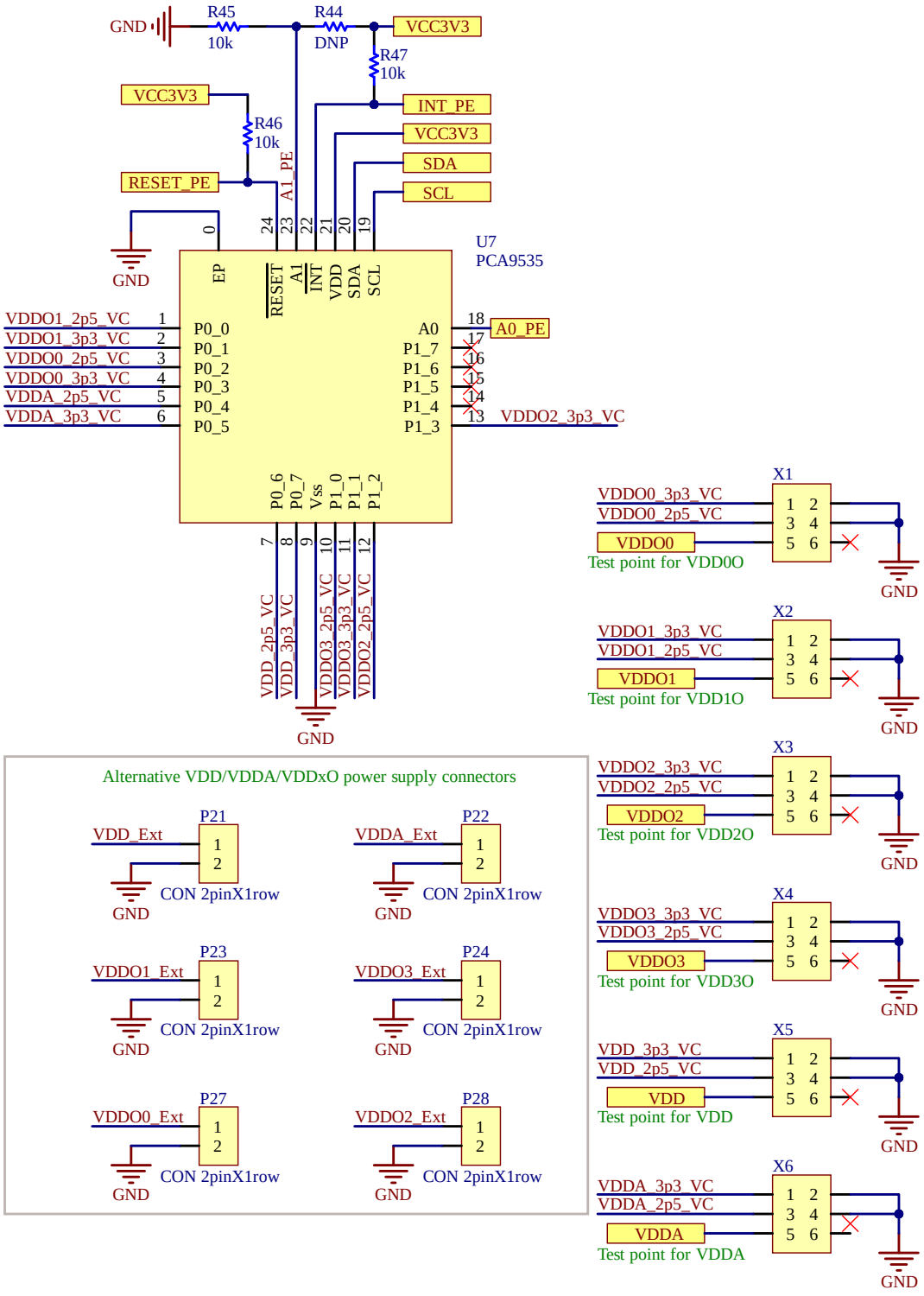


Figure A2. SiT6520EB Power Supply Diagram

VDDA Supply

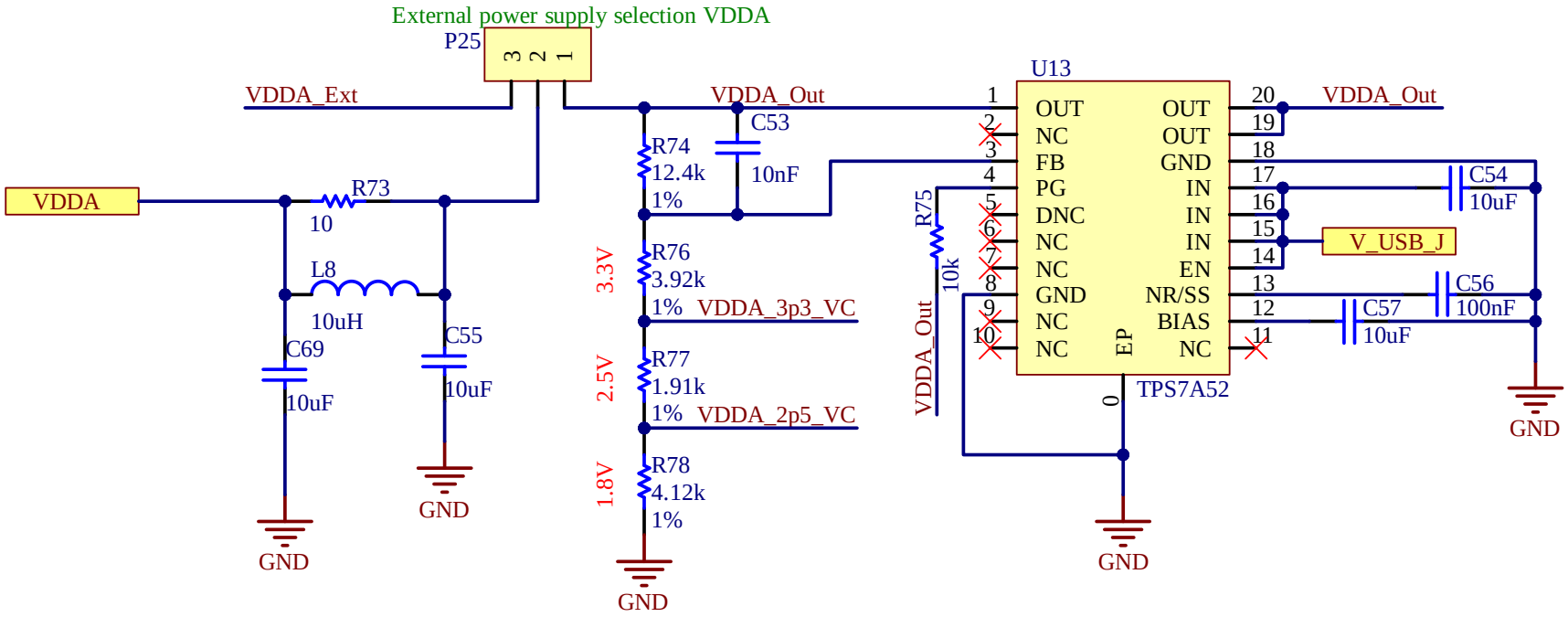


Figure A3. SiT6520EB VDDA

VDD Supply

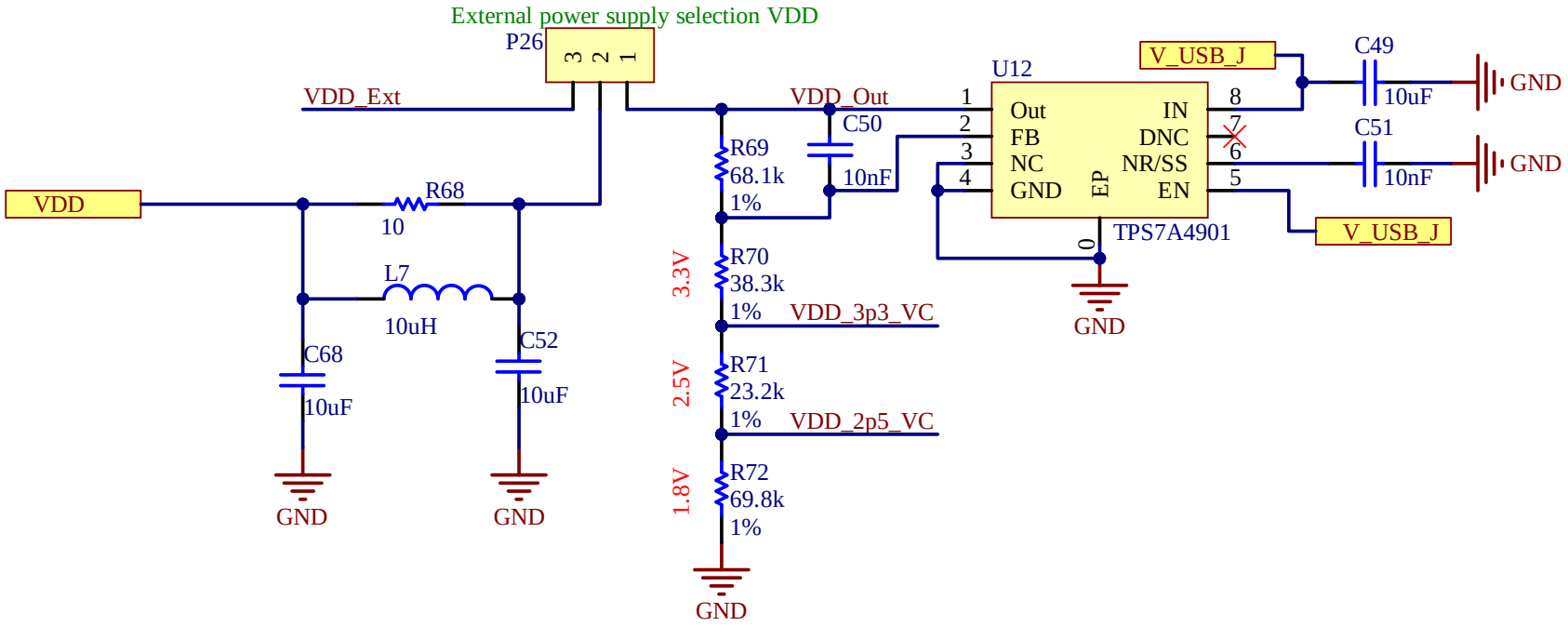


Figure A4. SiT6520EB VDD Supply Diagram

VDD0O Supply

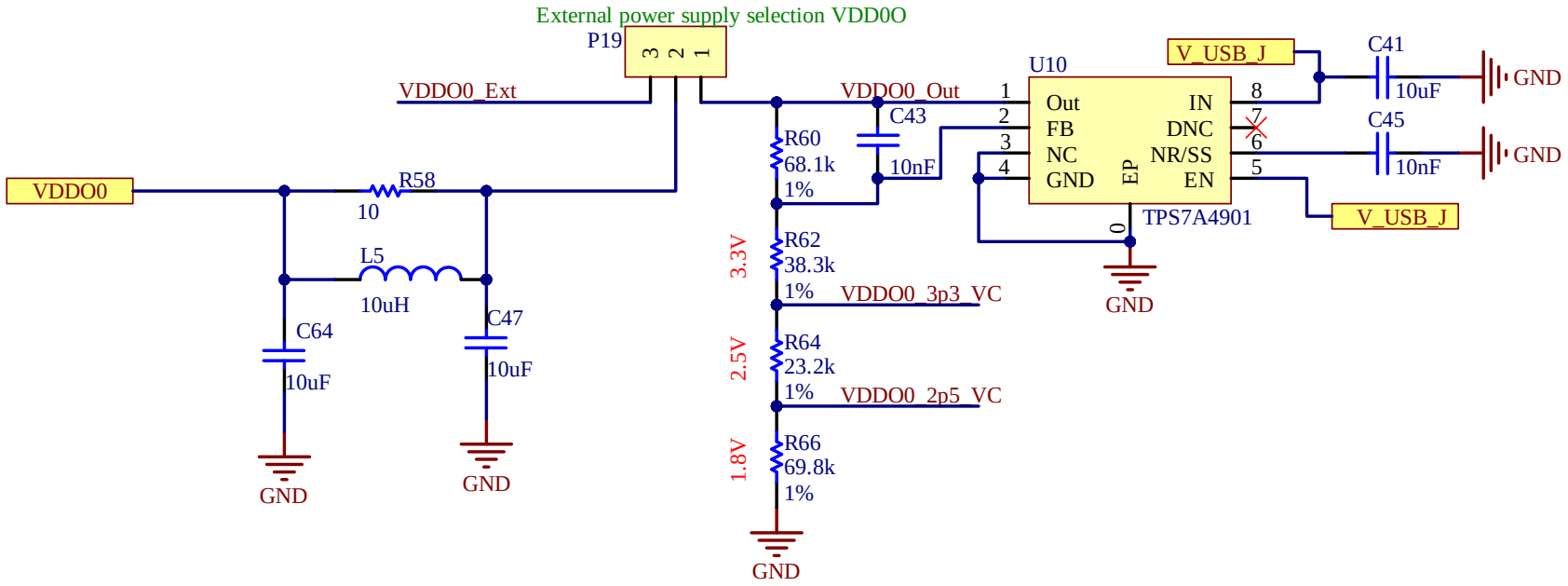


Figure A5. SiT6520EB VDD0O Supply Diagram

VDD1O Supply

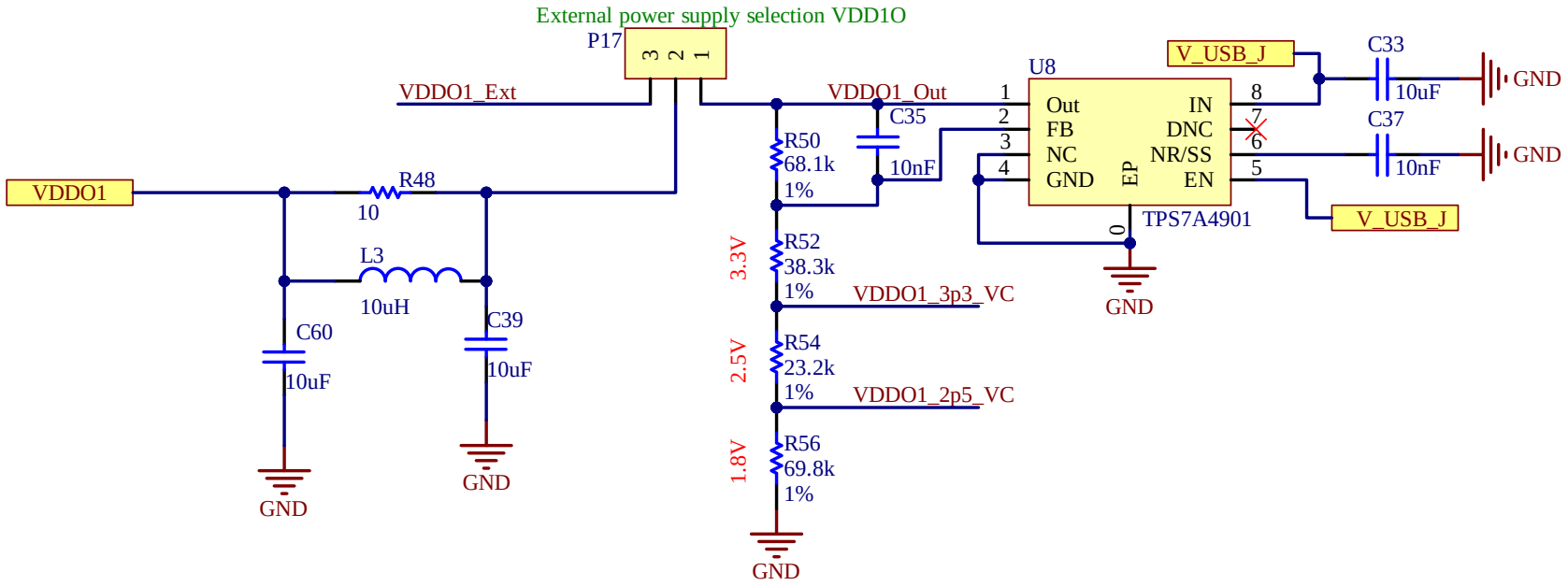


Figure A6. SiT6520EB VDD1O Supply Diagram

VDD2O Supply

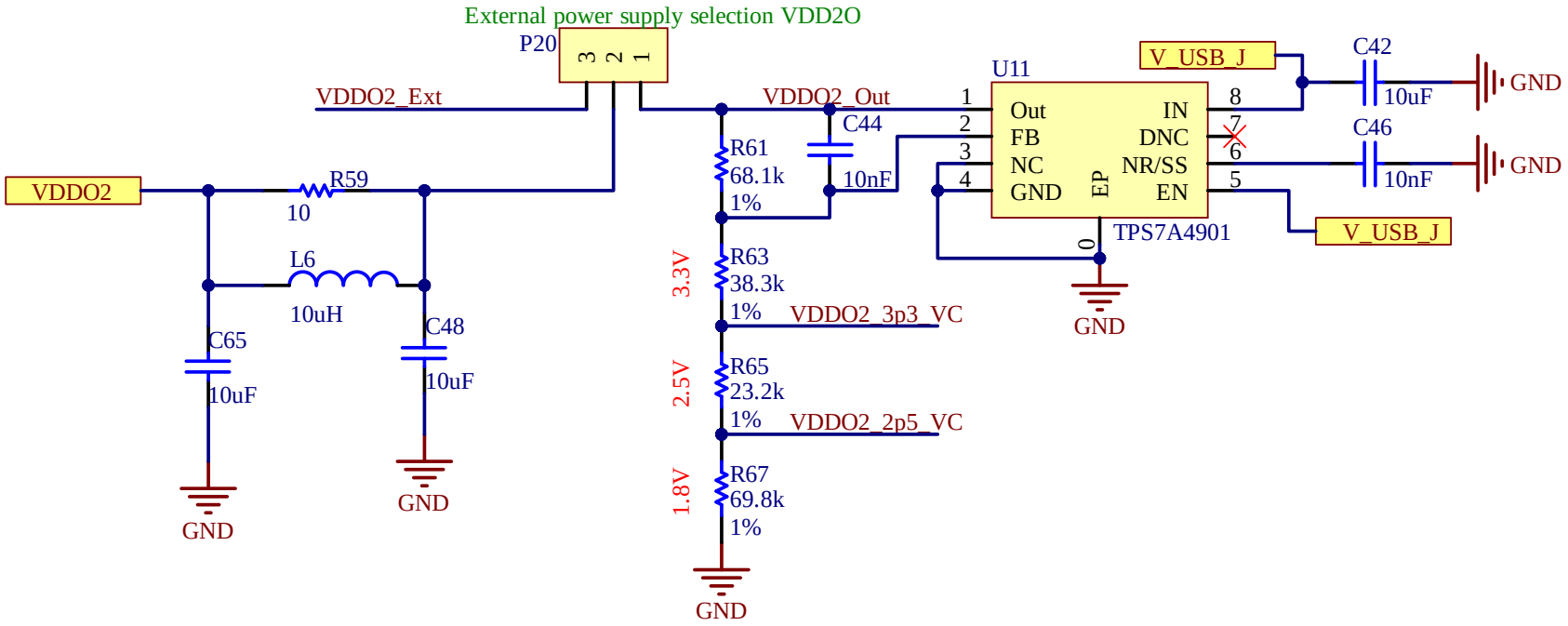


Figure A7. SiT6520EB VDD2O Supply Diagram

VDD3O Supply

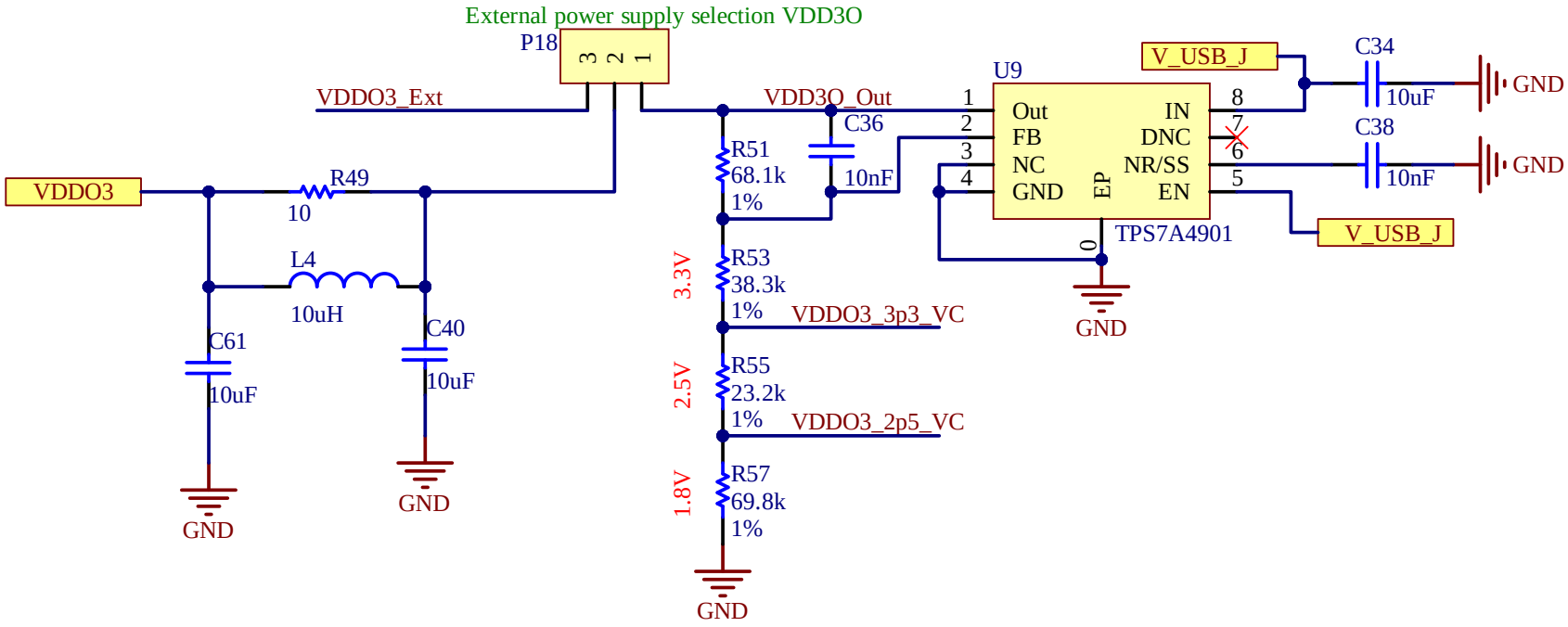


Figure A8. SiT6520EB VDD3O Supply Diagram

FTDI Supply

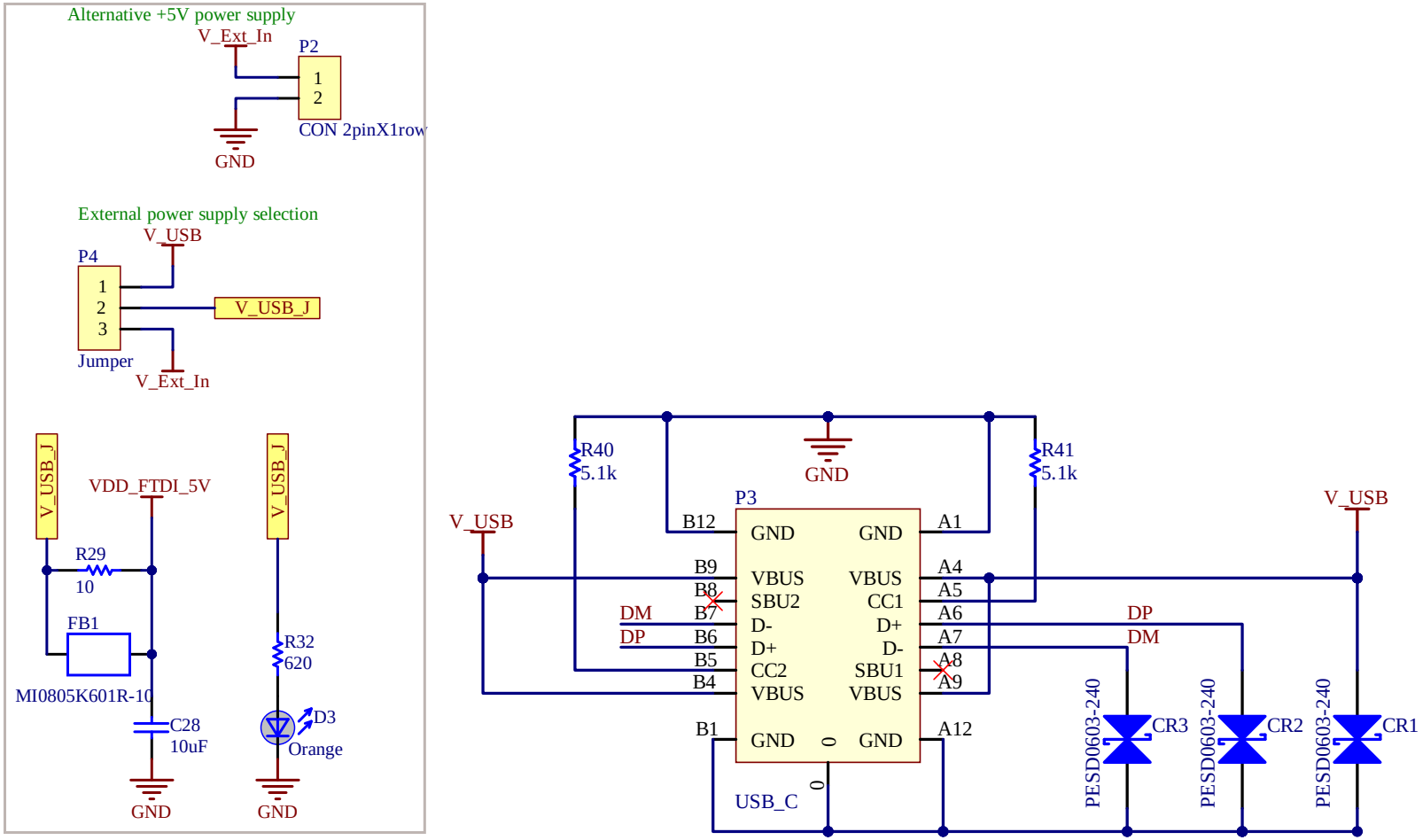
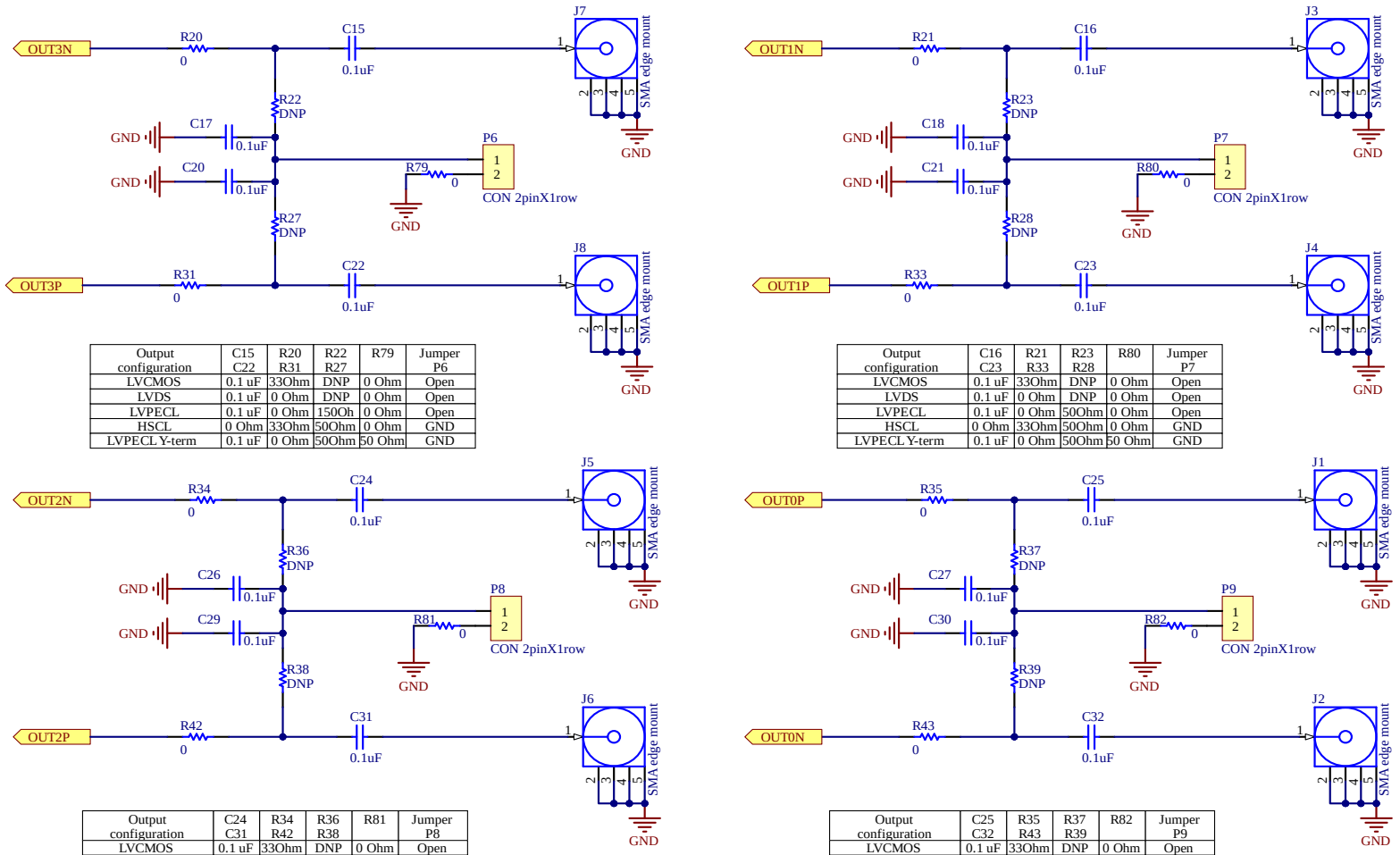


Figure A9. SiT6520EB FTDI Supply Diagram

OUTPUT CLKS



Output configuration	C15 C22	R20 R31	R22 R27	R79	Jumper P6
LVCMOS	0.1 uF	33Ohm	DNP	0 Ohm	Open
LVDS	0.1 uF	0 Ohm	DNP	0 Ohm	Open
LVPECL	0.1 uF	0 Ohm	150Oh	0 Ohm	Open
HSCL	0 Ohm	33Ohm	50Ohm	0 Ohm	GND
LVPECL Y-term	0.1 uF	0 Ohm	50Ohm	50 Ohm	GND

Output configuration	C16 C23	R21 R33	R23 R28	R80	Jumper P7
LVCMOS	0.1 uF	33Ohm	DNP	0 Ohm	Open
LVDS	0.1 uF	0 Ohm	DNP	0 Ohm	Open
LVPECL	0.1 uF	0 Ohm	50Ohm	0 Ohm	Open
HSCL	0 Ohm	33Ohm	50Ohm	0 Ohm	GND
LVPECL Y-term	0.1 uF	0 Ohm	50Ohm	50 Ohm	GND

Output configuration	C24 C31	R34 R42	R36 R38	R81	Jumper P8
LVCMOS	0.1 uF	33Ohm	DNP	0 Ohm	Open
LVDS	0.1 uF	0 Ohm	DNP	0 Ohm	Open
LVPECL	0.1 uF	0 Ohm	50Ohm	0 Ohm	Open
HSCL	0 Ohm	33Ohm	50Ohm	0 Ohm	GND
LVPECL Y-term	0.1 uF	0 Ohm	50Ohm	50 Ohm	GND

Output configuration	C25 C32	R35 R43	R37 R39	R82	Jumper P9
LVCMOS	0.1 uF	33Ohm	DNP	0 Ohm	Open
LVDS	0.1 uF	0 Ohm	DNP	0 Ohm	Open
LVPECL	0.1 uF	0 Ohm	50Ohm	0 Ohm	Open
HSCL	0 Ohm	33Ohm	50Ohm	0 Ohm	GND
LVPECL Y-term	0.1 uF	0 Ohm	50Ohm	50 Ohm	GND

Figure A10. SiT6520EB OUTPUT CLKS Diagram

STATUS LEDS – 2

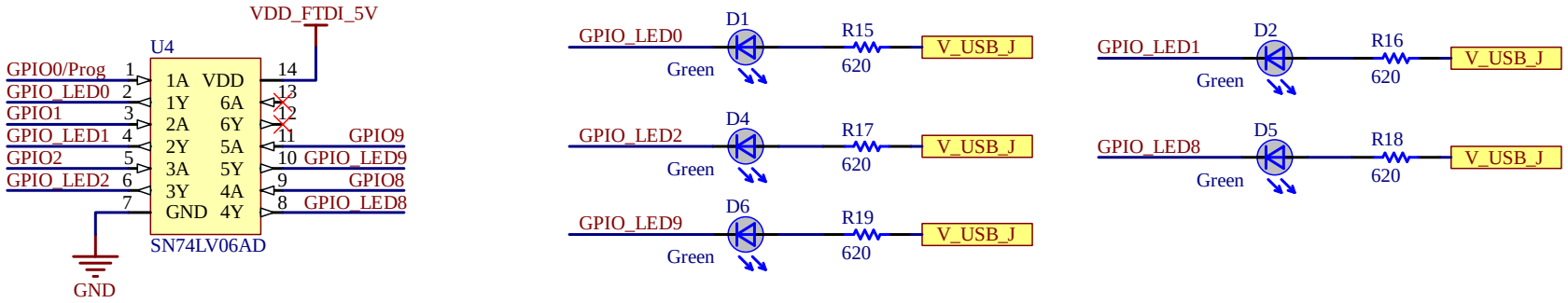


Figure A11. SiT6520EB STATUS LEDS – 2

Chorus SiT912xx DUT

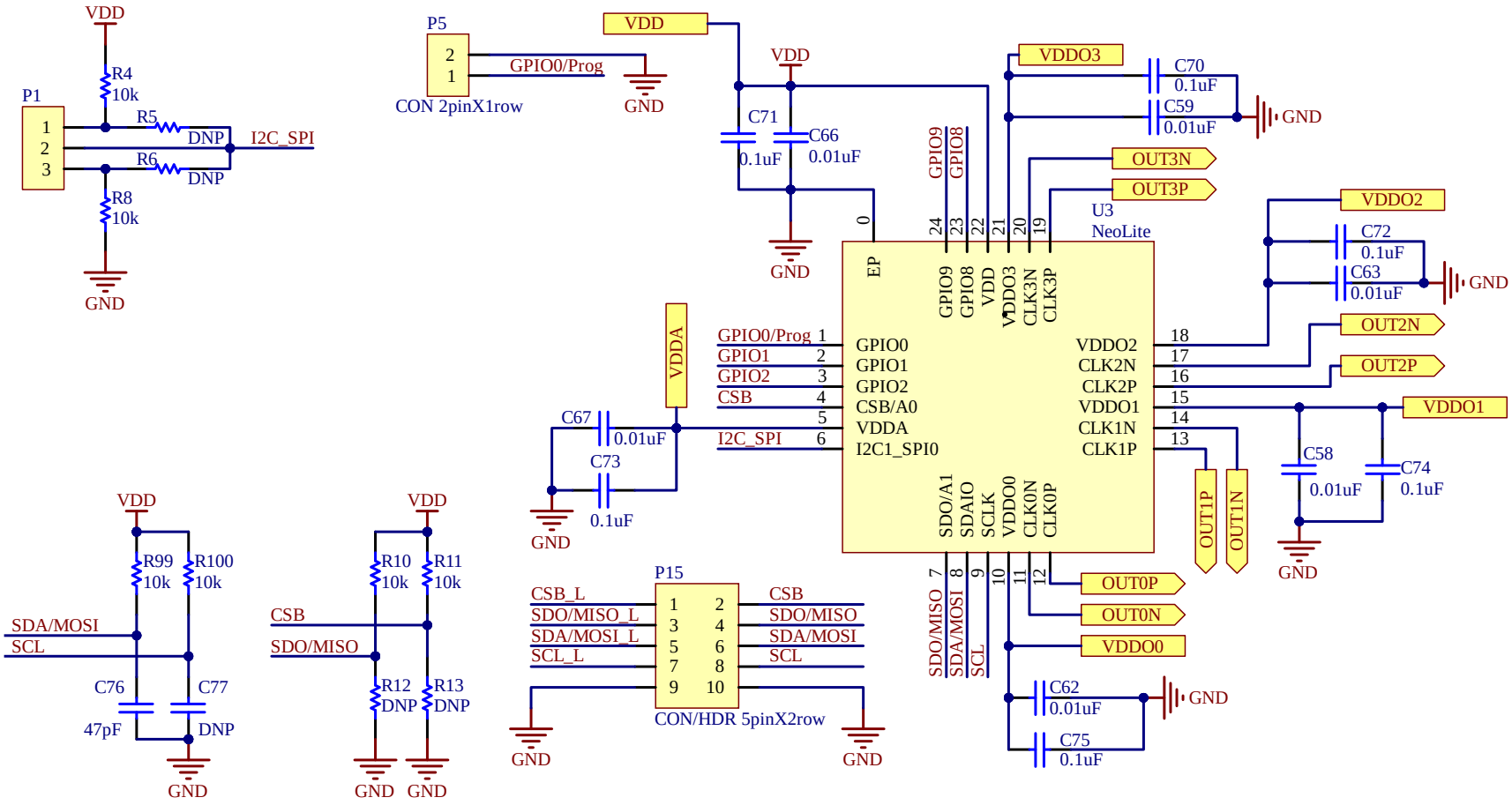


Figure A12. QFN Chorus SiT912xx DUT Diagram

FTDI

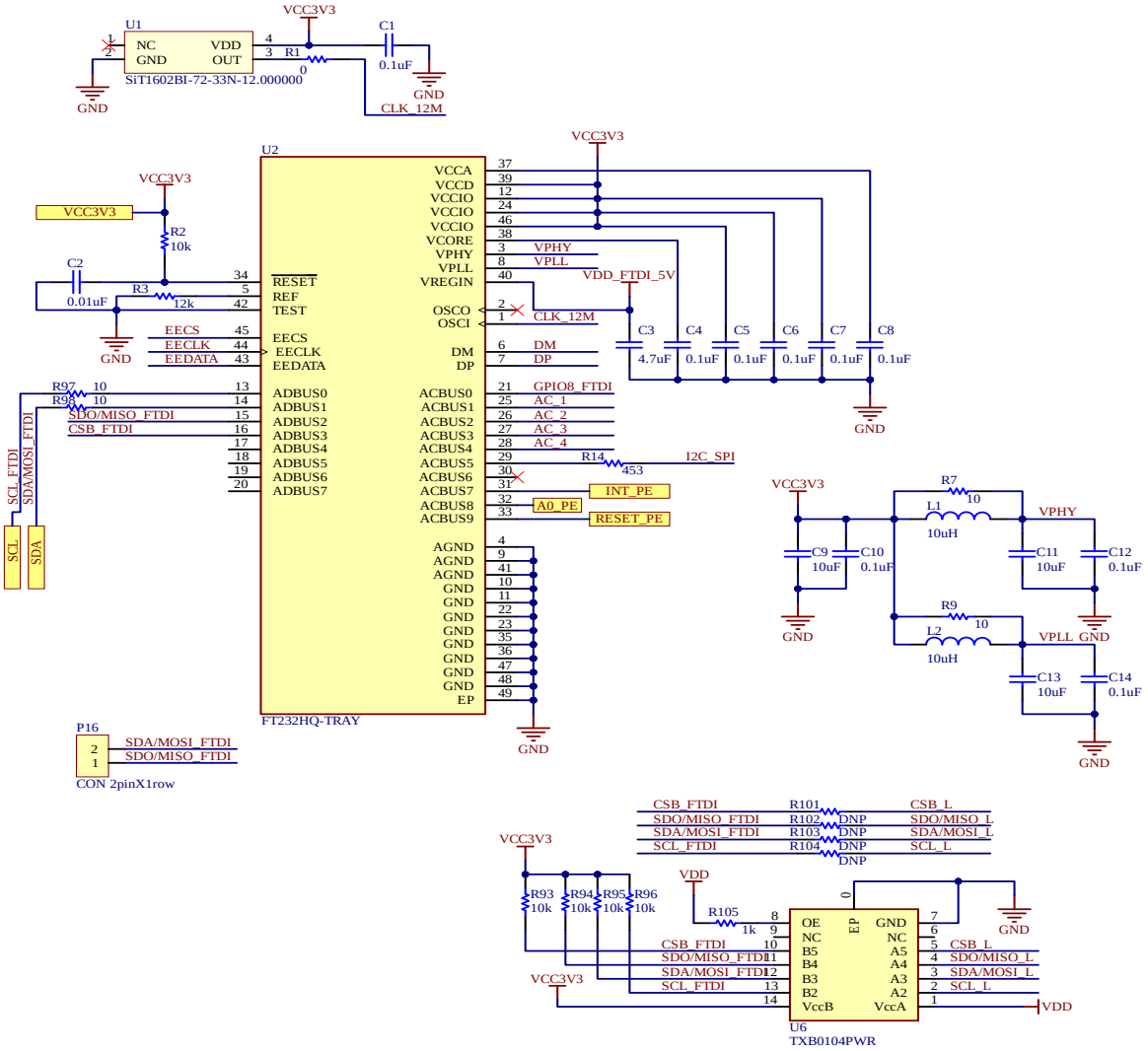


Figure A13. SiT6520EB FTDI Diagram

Appendix B: EVB Top View

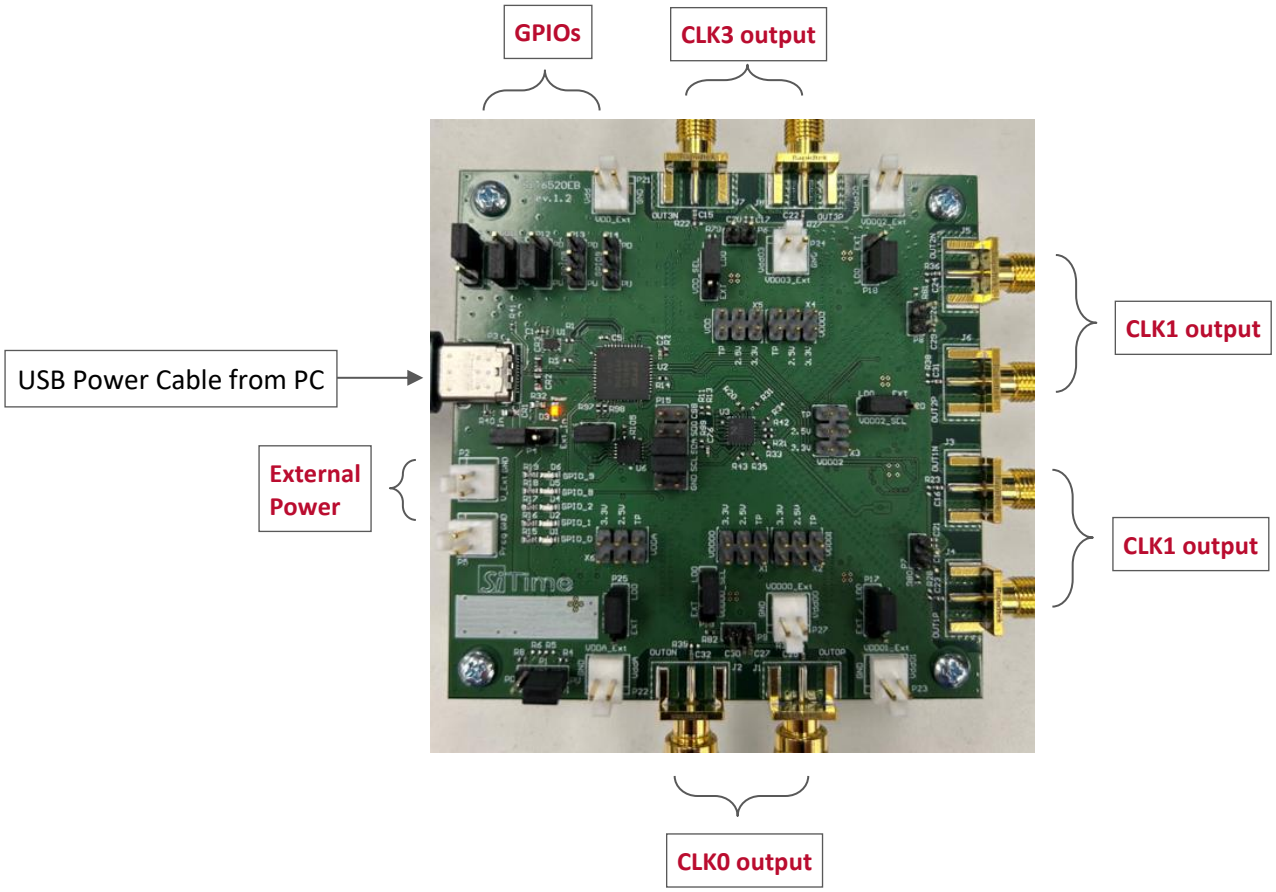


Figure B1. SiT6520EB Top View

Table 10: Revision History

Version	Release Date	Change Summary
1.0	15-Apr-2024	Original doc

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439