SiT6503EB Evaluation Board (EVB) HW User Manual

Contents

1 Introduction

The SiT6503EB Evaluation Board (EVB) is designed for evaluating the following programmable clock generator, jitter cleaners, and networking synchronizers.

- SiT95141
- SiT95143
- SiT95145
- SiT95148

2 SiT6503EB Features

- Supports SiT95141, SiT95143, SiT95145, and SiT95148
- Powered from USB port or external power supply
- Programmable VDDO supplies for 11 outputs selectable from 3.3, 2.5, or 1.8 V
- Status LEDs for power supplies status signals of SiT6503EB
- Each of the 11 outputs accessible via edge mount high bandwidth SMA connectors
- 4 pairs of edge mount SMA connectors for feeding external differential or single-ended clocks inputs
- Supports full configuration flexibility of the device via standard I^2C or SPI interface with a Windows hosted Time Master for Clocks GUI

3 SiT6503EB Support Collateral

The SiT6503EB Evaluation Board is provided with the following collateral:

- SiT6503EB EVB HW User Manual
- TimeMaster GUI self-installing executable
- TimeMaster GUI User Manual

4 Connectors Descriptions

Table 1 lists the SiT6503EB EVB connectors.

Table 1. SiT6503EB connectors

Connector Designators	Description
Power + Control	USB Type B connectors (J3) for Device programming and +5V supply
Power	USB Type B connectors (J4) for +5V supply, 2-pin connectors (J80, J7) for external +5V power supply
Inputs	SMA connectors (J35 through J42) for receiving external clock signals
Outputs	SMA connectors (J43 through J64) for synthesized clock outputs
External FTDI supply	2-pin connector (H13)
External +3.3V (VDD Left) Input receiver supply	2-pin connector (H1)
External +3.3V (VDD PLL) supply	2-pin connector (H12)
External Output VDD Supply	2-pin connectors (H2 through H11)

Connector Designators	Description
Common Mode to GND Headers in output terminations	2-pin Headers (JSCL13 through JSCL23)
Output LDO Regulators Enable Inputs to GND Headers	2-pin Headers (J2, JSCL3 through JSCL11), shorted by default for LDO outputs enabling
Left Supply LDO Regulators Enable Inputs to GND Headers	2-pin Headers (J1), shorted by default for LDO outputs enabling
Header for internal use only	2-pin Header (JSCL 1), shorted by default
Headers for I^2C bus Pull-up	2-pin Headers (JSCL 2, JSCL 12), shorted by default
Header	1-pin Header (J5)
Header for PLL supply LDO regulator output Shut Down	2-pin Header (J12)
Header for configuring the SiT6503EB into I^2C and SPI Mode (I^2C Mode is default one)	10-pin Header (J76)
PullUp vs PullDown switch Headers	3-pin Headers (J67 through J69, J72 through J74, J81, JVDD1)
Signals switch Header	3-pin Header (J71)
PLL supply voltage source switching Header	3-pin Header (J31)
PLL supply voltage levels switching Header	3-pin Header (J32)
Left supply voltage source switching Header	3-pin Header (J8)
Left supply voltage levels switching Header	3-pin Header (J9)
FTDI supply voltages source switching Header	3-pin Header (J78)
FTDI supply voltage levels switching Header	3-pin Header (J30)
USB – External Power sources switching Headers	3-pin Headers (J79, J6)
Outputs supply voltage source switching Header	3-pin Headers (J10, J77, J14, J16, J18, J20, J22, J24, J26, J28)
Outputs supply voltage levels switching Header	3-pin Headers (J11, J13, J15, J17, J19, J21, J23, J25, J27, J29)

5 Test Points Descriptions

Table 2 describes all Test Point (TP)s on the EVB.

Table 2. SiR6503EB Test Points description

Connector Designators	Description
GND Test Points	1-pin Headers (TP3, TP4, TP5, TP9)
Test Points for internal use only	1-pin Headers (J82 through J86)
Reserved Test Points	1-pin Headers (TP6, TP8)

6 Jumpers Default List

Table 3 lists the default positions of the Jumpers on the EVB.

Table 3. Jumper Default List

Jumper Location	Type	I = Installed O = Open	Jumper Location	Type	I = Installed O = Open	Jumper Location	Type	I = Installed O = Open
JSCL1	2-Pin	I	**J1**	2-Pin	I	**J27**	3-Pin	1 to 2
JSCL2	2-Pin	I	**J2**	2-Pin	I	**J28**	3-Pin	1 to 2
JSCL3	2-Pin	I	**J6**	3-Pin	2 to 3	**J29**	3-Pin	1 to 2
JSCL4	2-Pin	I	**J8**	3-Pin	1 to 2	**J30**	3-Pin	1 to 2
JSCL5	2-Pin	I	**J9**	3-Pin	1 to 2	**J31**	3-Pin	1 to 2
JSCL6	2-Pin	I	**J10**	3-Pin	1 to 2	**J32**	3-Pin	O
JSCL7	2-Pin	I	**J11**	3-Pin	1 to 2	**J67**	3-Pin	O
JSCL8	2-Pin	I	**J12**	2-Pin	O	**J68**	3-Pin	O
JSCL9	2-Pin	I	**J13**	3-Pin	1 to 2	**J69**	3-Pin	O
JSCL10	2-Pin	I	**J14**	3-Pin	1 to 2	**J71**	3-Pin	O
JSCL11	2-Pin	I	**J15**	3-Pin	1 to 2	**J72**	3-Pin	O
JSCL12	2-Pin	I	**J16**	3-Pin	1 to 2	**J73**	3-Pin	1 to 2
JSCL13	2-Pin	O	**J17**	3-Pin	1 to 2	**J74**	3-Pin	O
JSCL14	2-Pin	O	**J18**	3-Pin	1 to 2	**J76**	10-Pin Header	1 to 2, 3 to 4, 7 to 8, 9 to 10
JSCL15	2-Pin	O	**J19**	3-Pin	1 to 2	**J77**	3-Pin	1 to 2
JSCL16	2-Pin	O	**J20**	3-Pin	1 to 2	**J78**	3-Pin	1 to 2
JSCL17	2-Pin	O	**J21**	3-Pin	1 to 2	**J79**	3-Pin	1 to 2
JSCL18	2-Pin	O	**J22**	3-Pin	1 to 2	**J80**	2Pin	O
JSCL19	2-Pin	O	**J23**	3-Pin	1 to 2	**J81**	3-Pin	O

Jumper Location	Type	I = Installed O = Open	Jumper Location	Type	I = Installed O = Open	Jumper Location	Type	I = Installed O = Open
JSCL20	2-Pin	O	**J24**	3-Pin	1 to 2	**JVDD1**	3-Pin	2 to 3
JSCL21	2-Pin	O	**J25**	3-Pin	1 to 2			
JSCL22	2-Pin	O	**J26**	3-Pin	1 to 2			
JSCL23	2-Pin	O						

7 Default Resistor Connection from FTDI to SiT95148

Table 4 lists the default resistor connection from FTDI to the SiT95148 Device on the EVB.

Table 4. Default Resistor connection from FTDI to DUT on the SiT6503EB

Signal name	Resistors	S = 0 ohm Short O = DNP
Flexio1_dut	R150	S
Flexio2_dut	R152	S
Flexio3_dut	R154	S
Flexio4_dut	R156	S
Flexio5_dut	R158	S
Flexio8_dut	R160	S
Flexio12_dut	R162	S
Flexio13_dut	R164	S
Flexio14_dut	R166	S
Flexio15_dut	R168	S
I2C1_SPIO_DUT	R170	S
RSTB_DUT	R172	S
ACBUS0	R175	O
ADBUS4	R151	O
ACBUS1	R153	O
ACBUS2	R155	O
ADBUS5	R157	O
ADBUS6	R159	O
ADBUS7	R161	O

Signal name	Resistors	S = 0 ohm Short O = DNP
ACBUS3	R163	O
ACBUS4	R165	O
I2C1_SPIO	R169	S
RSTB	R171	S

8 Status LEDs

Table 5 lists the Status LEDs on the SiT6503EB EVB shown in Figure 1.

Table 5. SiT6503EB Status LEDs

Location	Color	Status Function indication
D5	Blue	Main USB +5V present
D6	Blue	Reserved USB +5V present (Is not populated normally)
D12	Green	FTDI VDD (+5V) present
D13	Green	+3.3V is present

***Note:** All LEDs are illuminated when corresponding voltages are present.

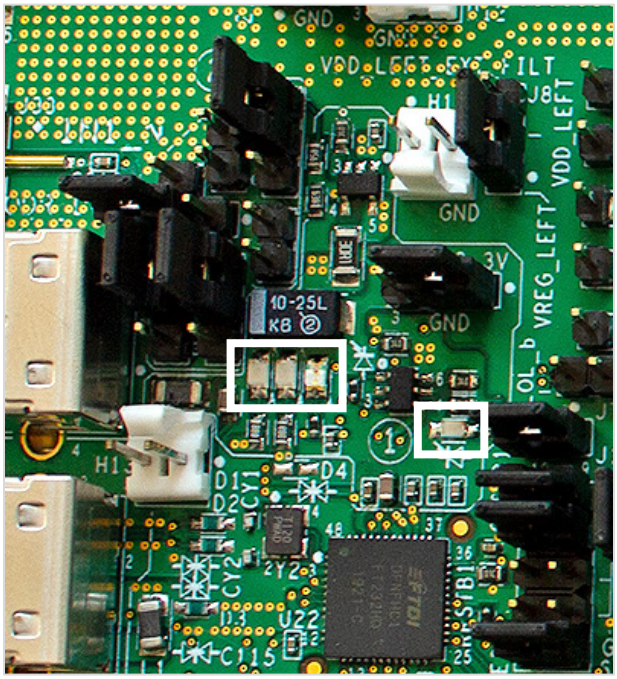

Figure 1. Status LEDs

9 SiT6503EB Power Supplying

Device under Test (DUT) Analog supplying voltage (VDDIN) and DUT outputs supplying voltages (VDDOx) on the SiT6503EB are configured to 3.3 V by default, whereas DUT PLLs supplying voltage VDD supply is configured to 1.8 V. The on board supplies/LDO's are configurable to 1.8 V, 2.5 V and 3.3 V with the Jumper option as shown in Figure 2. Please refer to SiT95148 datasheet for configuring the supply voltages on the VDDIN/VDD and VDDOx pins and to the Table 6 for on board configuration options for SiT95148:

Table 6. SiT6503EB Supply configuration

Variant	VDD	VDDIN	VDDOx
SiT95148	1.8 V	2.5 V / 3.3 V	1.8 V / 2.5 V / 3.3 V

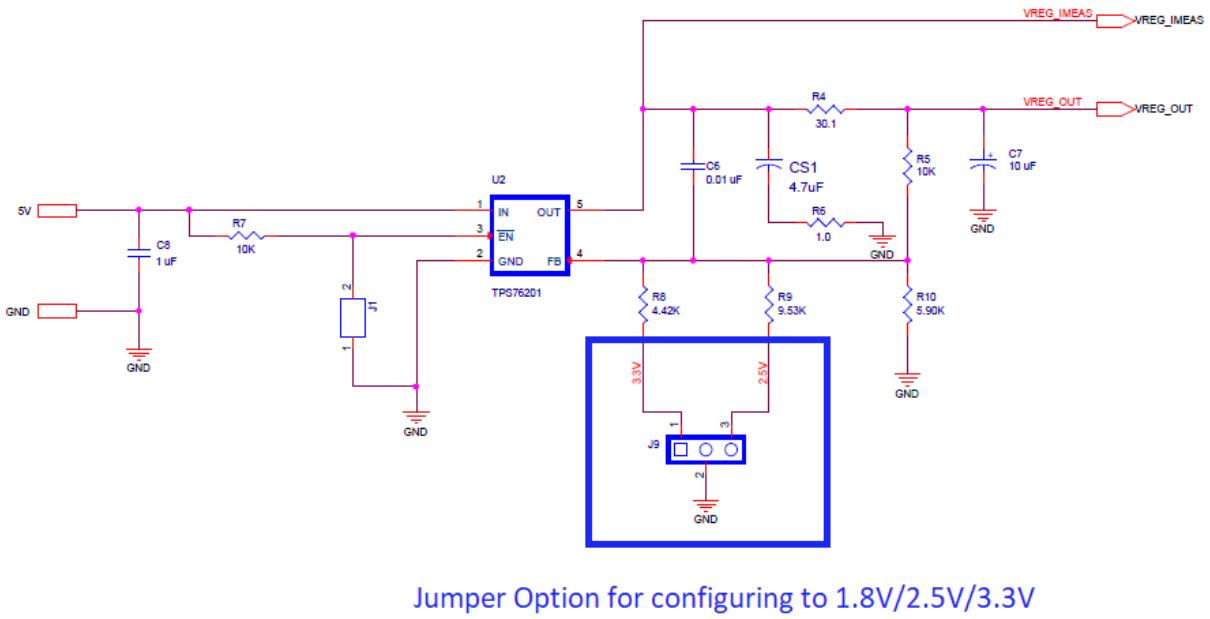

Figure 2. Supply Regulator for VDDIN/VDDOx

Note: For changing the VDDIN (J9) and VDDOx Supply, connect the corresponding Jumpers to below settings:

1) 3.3 V - Connect the 3-Pin Jumper from 1 to 2.
2) 2.5 V - Connect the 3-Pin Jumper from 2 to 3.
3) 1.8 V - Remove the Jumper.

There is a provision for connecting external supplies after bypassing the on board regulators for all the supplies as shown in Figure 3.

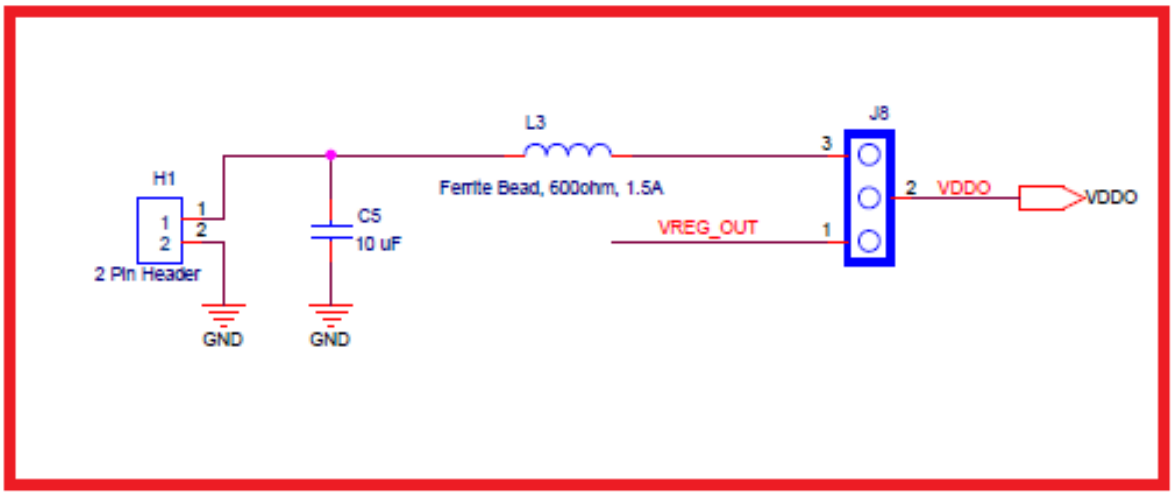

Figure 3. External Supply Connection Provision

PLLs supply circuitry is shown in Figure 4.

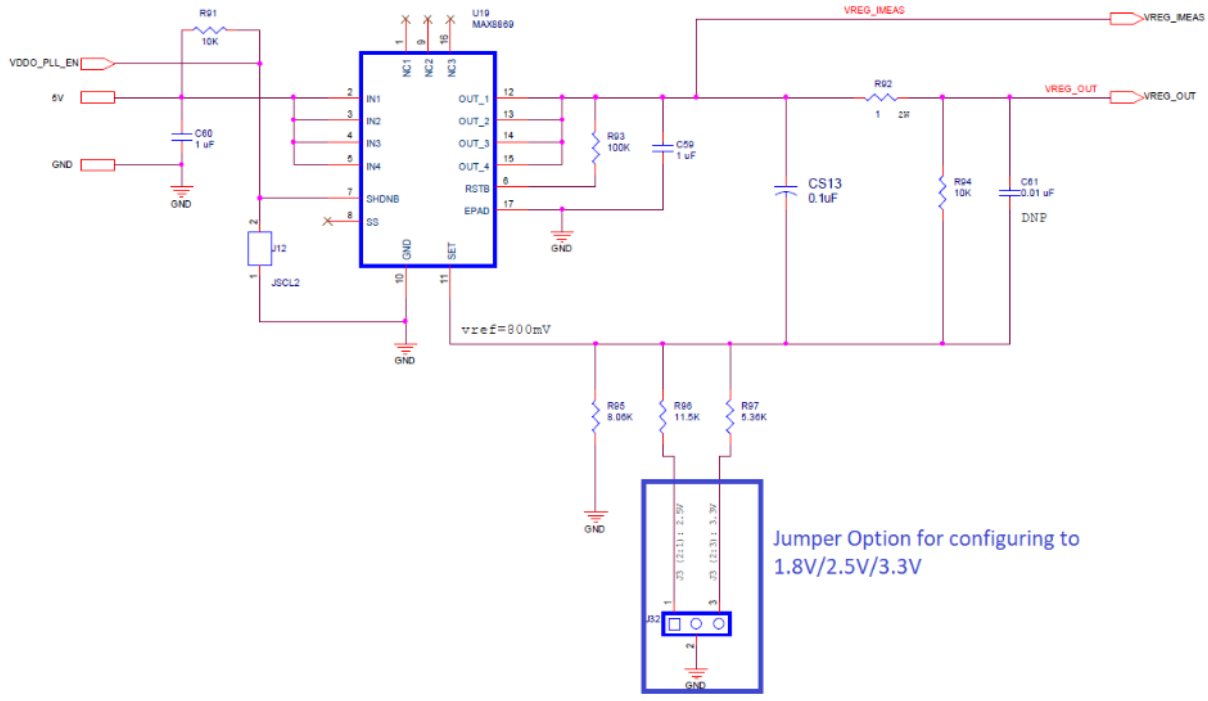

Figure 4. Supply Regulator for PLLs

Note: For changing the VDD (J32) Supply, connect the Jumper to below settings:

1) 3.3V - Connect the 3-Pin Jumper from 2 to 3.
2) 2.5V - Connect the 3-Pin Jumper from 1 to 2.
3) 1.8V - Remove the Jumper.

10 I²C/SPI Mode Connection

The 10 pin Header J76 (Figure 5) is mainly used for configuring the SiT6503EB into I²C and SPI Mode (I²C Mode is default one)

For I²C Mode of Operation:

1) SCLK_OUT is shorted to SCLK in J76.
2) SDAIO_OUT is shorted to SDAIO in J76.
3) CSB_OUT is shorted to CSB in J76.

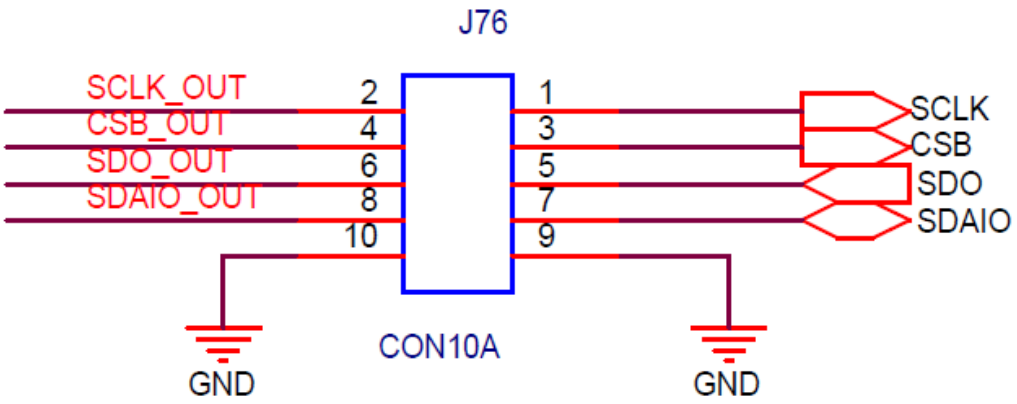

Figure 5. Supply Regulator for PLLs

For SPI Mode of Operation:

1) SCLK_OUT is shorted to SCLK in J76.
2) SDAIO_OUT is shorted to SDAIO in J76.
3) CSB_OUT is shorted to CSB in J76.
4) SDO_OUT is shorted to SDO in J76.
5) JSCL1 Jumper should be removed.
6) JVDD1 Jumper should be changed from (2 to 3) to (1 to 2).
7) J73 Jumper should be changed from (1 to 2) to (2 to 3).

11 Clock Inputs

The SiT6503EB has eight inputs (4 differential pairs) with SMA connectors (IN0_P, IN0_N, IN1_P, IN1_N, IN2_P, IN2_N, IN3_P, IN3_N) for receiving external clock signals. All input clocks are AC-coupled and 50 Ω terminated as shown in Figure 6 below. This represents four differential input clock pairs. Single-ended clocks can be used by driving the 'P' side of the differential pair with the 'N' input floating. Figure 6 shows the Input Clock Termination Circuit for one of the 4 pairs.

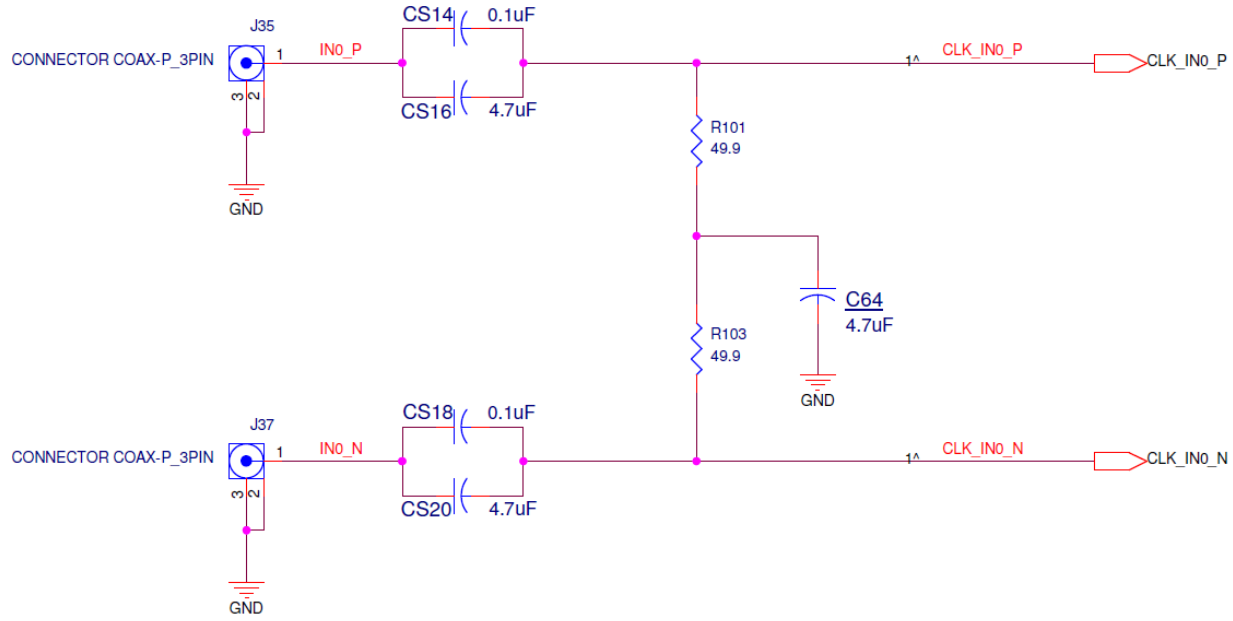

Figure 6. Input Clock Termination Circuit

12 Clock Outputs

When shipped from factory, each of the twenty output drivers (10 differential pairs) is AC-coupled to its respective SMA connector – this is the default configuration. The output clock termination circuit is shown in Figure 7 below. If dc coupling is required, the corresponding 0.1 uF AC coupling capacitor can be replaced with a zero Ω resistor. Figure 7 shows Output Clock Termination Circuit for one of the 10 output pairs.

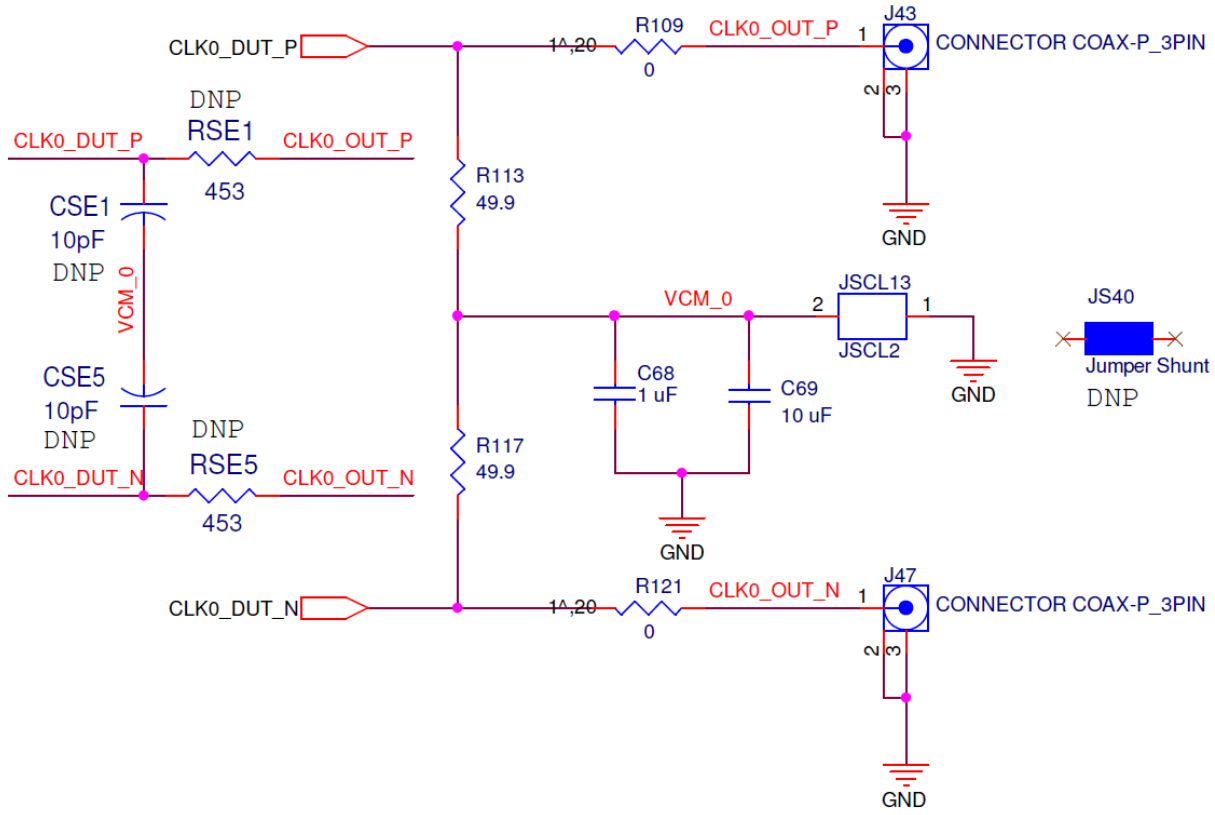

Figure 7. Output Clock Termination Circuit

12.1 Output Differential Termination

LVDS (default configuration), LVPECL, HCSL, and CML differential signaling types can be supported by changing the output termination circuits.

12.1.1 LVDS, CML

The board is shipped to support LVDS, CML in its default differential. The signals are AC coupled with ceramic 0.1 uF capacitors instead of the corresponding series resistors RSExx (Refer to Table 7) which are not populated.

Table 7. Output Port RSExx Resistors

Output Port #	0B	1B	0	1	2	3	4	5	6	7	0T
0.1 uF capacitors	RSE21 RSE22	RSE17 RSE19	RSE1 RSE5	RSE2 RSE6	RSE4 RSE7	RSE3 RSE8	RSE10 RSE14	RSE9 RSE13	RSE11 RSE15	RSE12 RSE16	RSE18 RSE20

Output termination resistors as shown in Table 8 are not populated.

Table 8. Output Port Not Populated Resistors

Output Port #	0B	1B	0	1	2	3	4	5	6	7	0T
Not Populated Resistors	R176 R178	R143 R145	R113 R117	R114 R118	R115 R119	R116 R120	R129 R133	R130 R134	R131 R135	R132 R136	R144 R146

12.1.2 LVPECL

For LVPECL output configuration ceramic capacitors 0.1 uF are placed instead of correspondent series resistors RSExx (Refer to Table 7). Termination resistor values depending on the output driver VDD level are shown in Table 9.

Table 9. Output Port Termination Resistors for LVPECL

Output Port #	0B	1B	0	1	2	3	4	5	6	7	0T
Resistors	R176 R178	R143 R145	R113 R117	R114 R118	R115 R119	R116 R120	R129 R133	R130 R134	R131 R135	R132 R136	R144 R146
VDD, 3.3V	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω	150 Ω
VDD, 2.5V	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω	120 Ω

Also, ensure that jumpers JSCLxx as per Table 10 are populated to allow path to GND.

Table 10. Output Port Jumpers to GND

Output Port #	0B	1B	0	1	2	3	4	5	6	7	0T
Jumpers to GND	JSCL23	JSCL21	JSCL13	JSCL14	JSCL15	JSAL16	JSCL17	JSCL18	JSCL19	JSCL20	JSCL22

12.1.3 HCSL

For HCSL output configuration series resistors RSExx (Refer to Table 7). 33 Ω should be used for each output port. Please note each lane per pair should be terminated by 50 Ω to GND on the receiver side.

13 Quick Start

- Install SiT95148 Software GUI on your Windows PC
- Confirm jumpers are installed as shown in Table 3
- Connect a USB cable from SiT6503EB, J3 to your PC
- Launch the SiT95148 Software GUI
- Refer to the accompanying SiT95148 Software User Manual to configure your frequency plan on the SiT6503EB
- Default Output Driver Configuration is LVDS and Output Driver Supplies are configured to 3.3 V

- Default VDD Supply on the EVB is configured to 1.8 V and default VDDIN supply on the EVB is configured to 3.3 V
- The FTDI chip on the EVB is configured to I^2C as the default communication protocol
- EVB default configuration is shown in Figure 8.

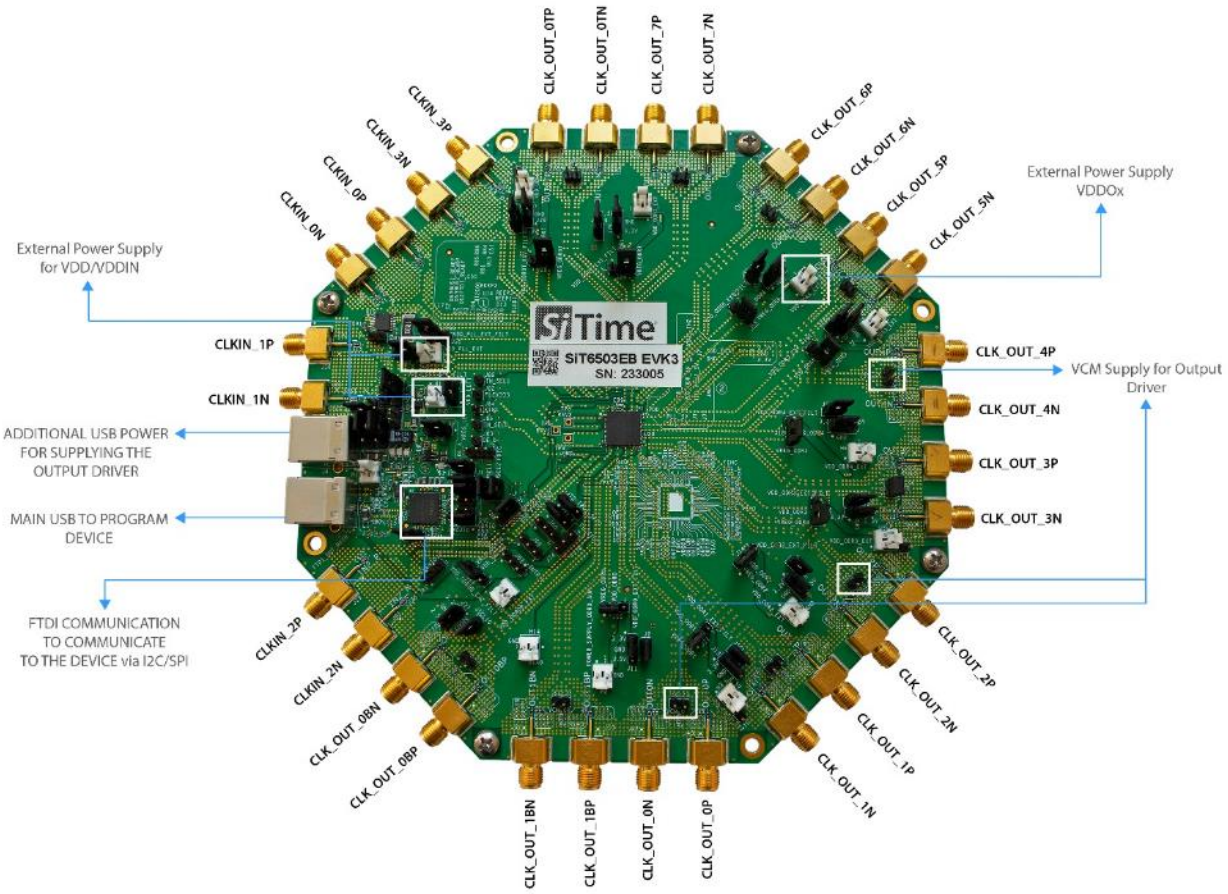

Figure 8. SiT6503EB Starter Connection Diagram

The general guidelines for single USB power supply operation are listed below:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA respectively at +5V
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤ 470 mA.
  Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5 V drops gracefully by less than 10%, the EVB will still work

Appendix A: EVB Schematic Diagrams

EVB Top Level Diagram

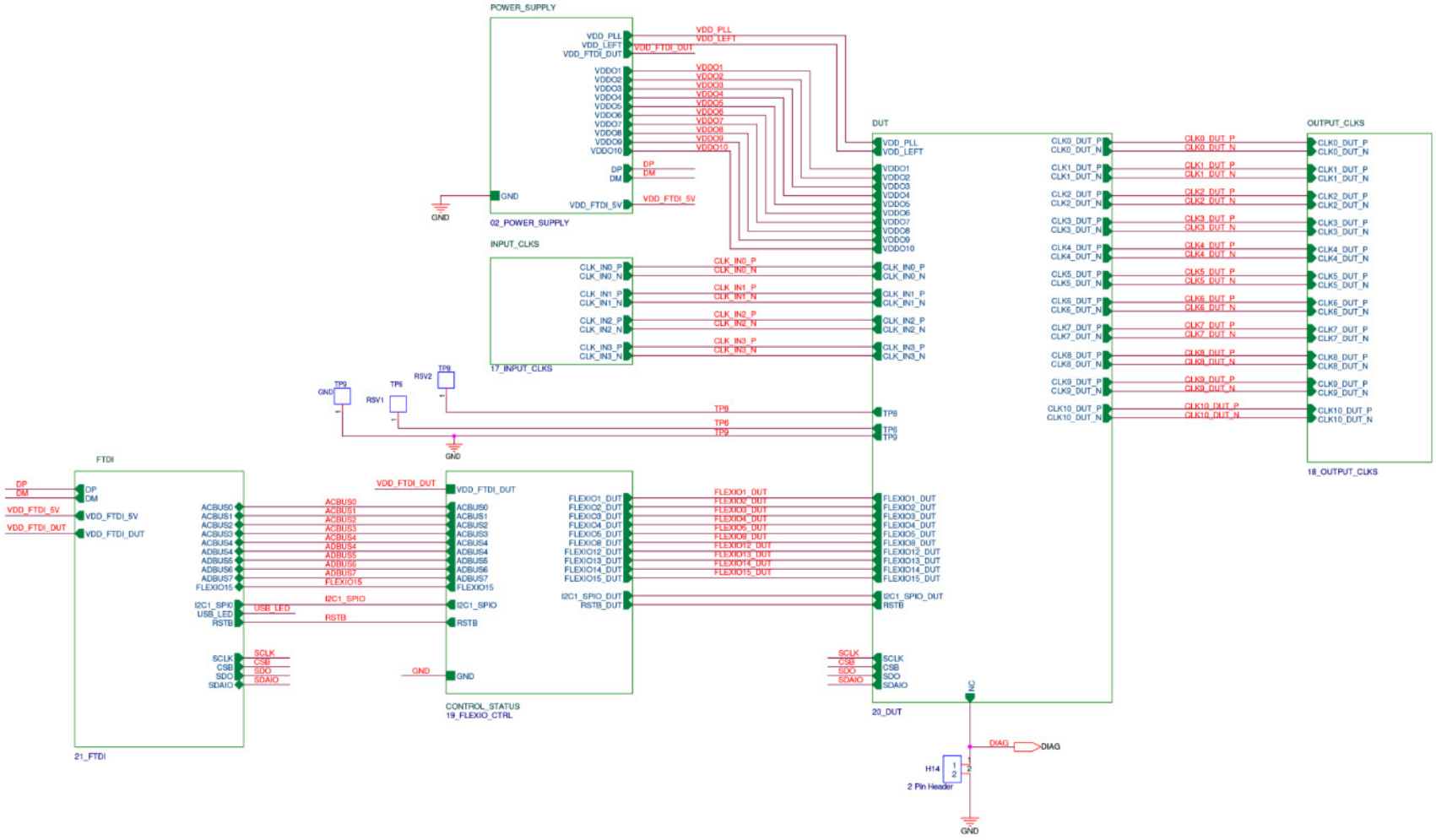

Figure A1. SiT6503EB Top Level Diagram

Power Supply

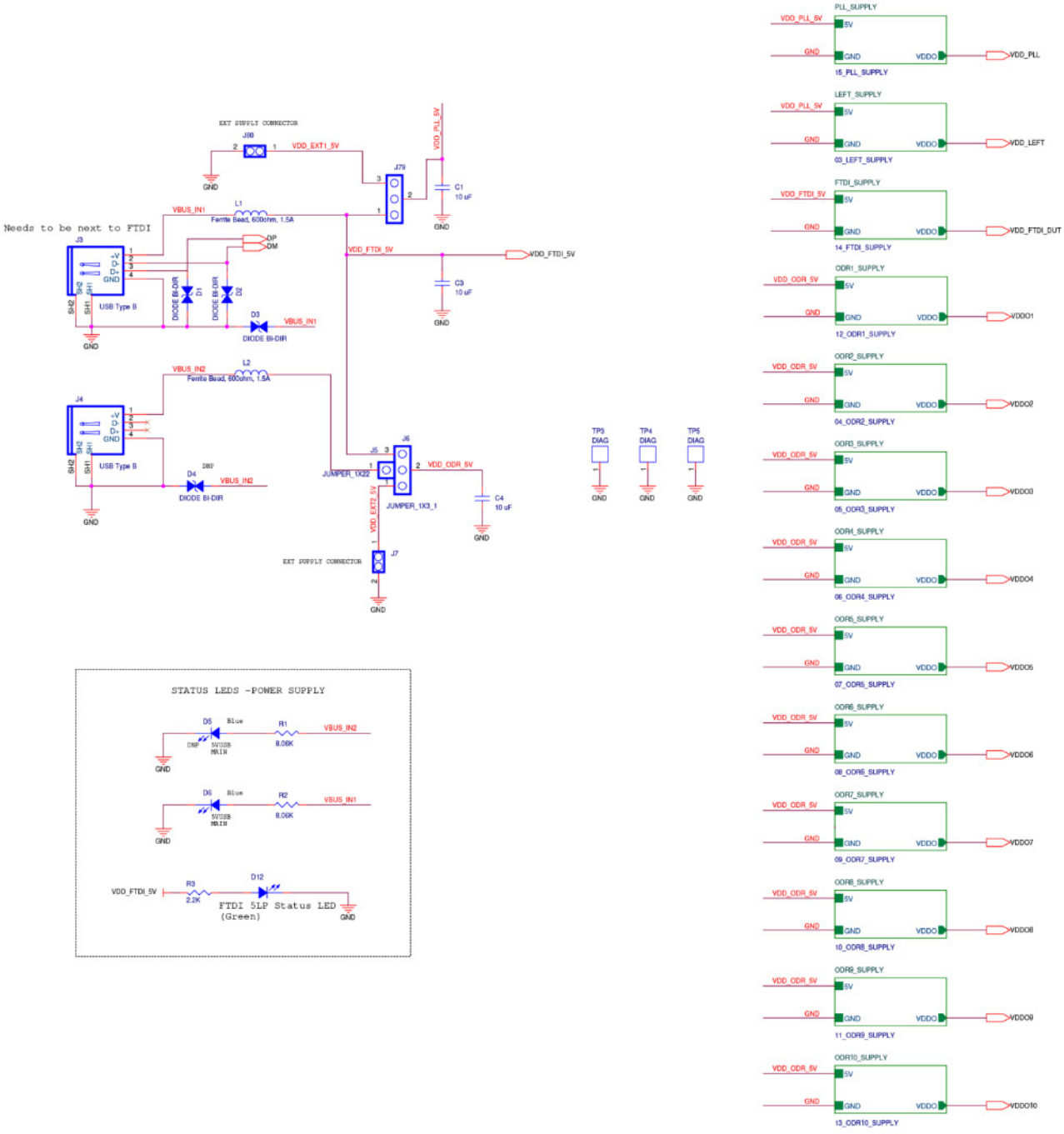

Figure A2. SiT6503EB Power Supply Diagram

Left Supply

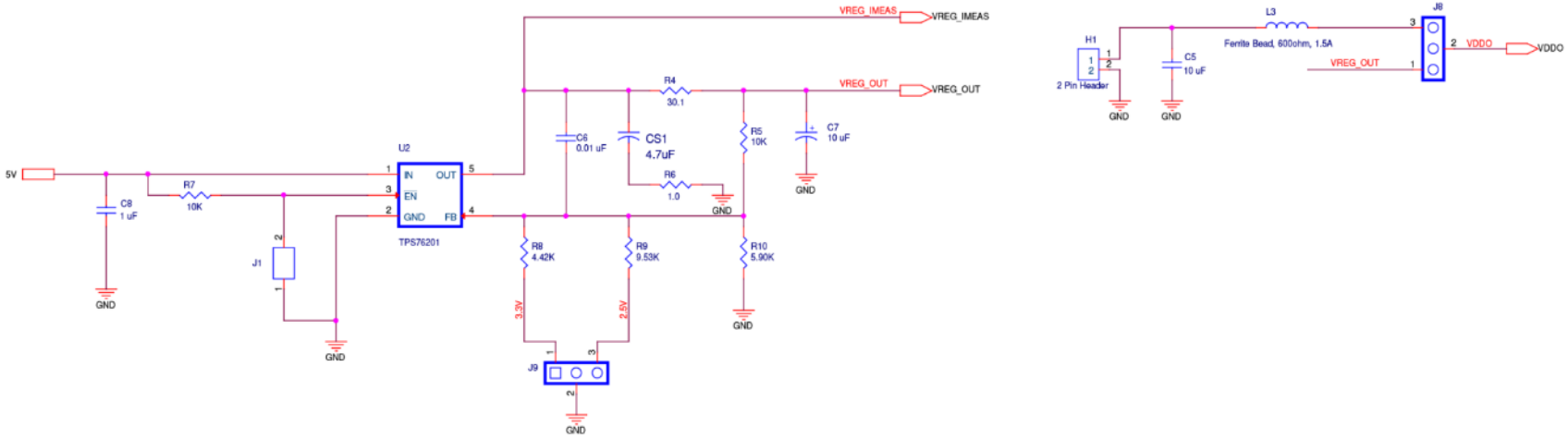

Figure A3. SiT6503EB Left Supply Diagram

ODR1 Supply

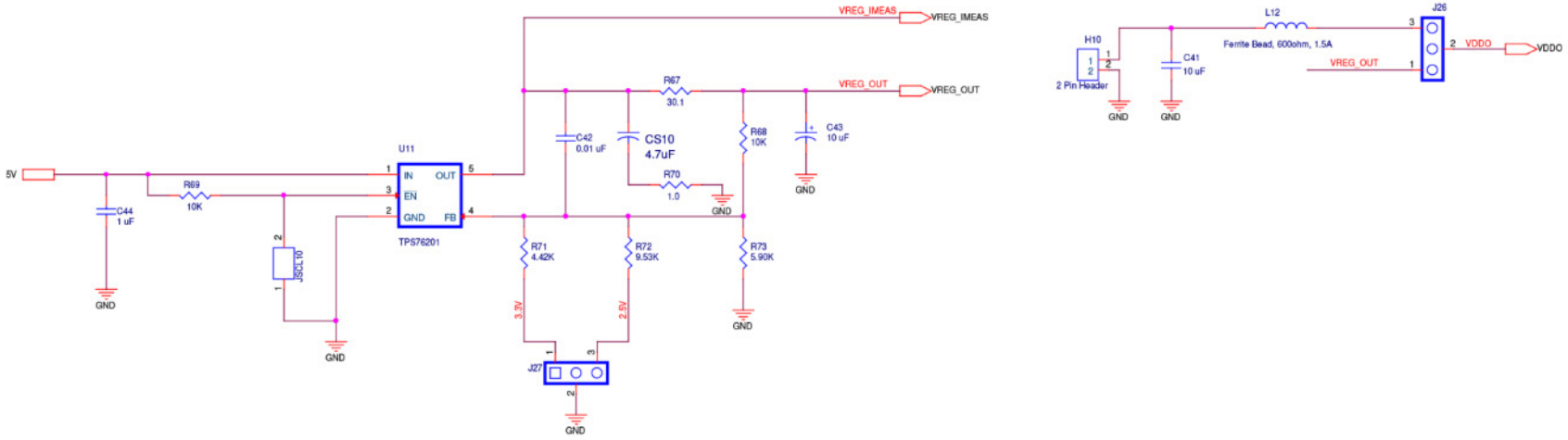

Figure A4. SiT6503EB ODR10 Supply Diagram

ODR2 Supply

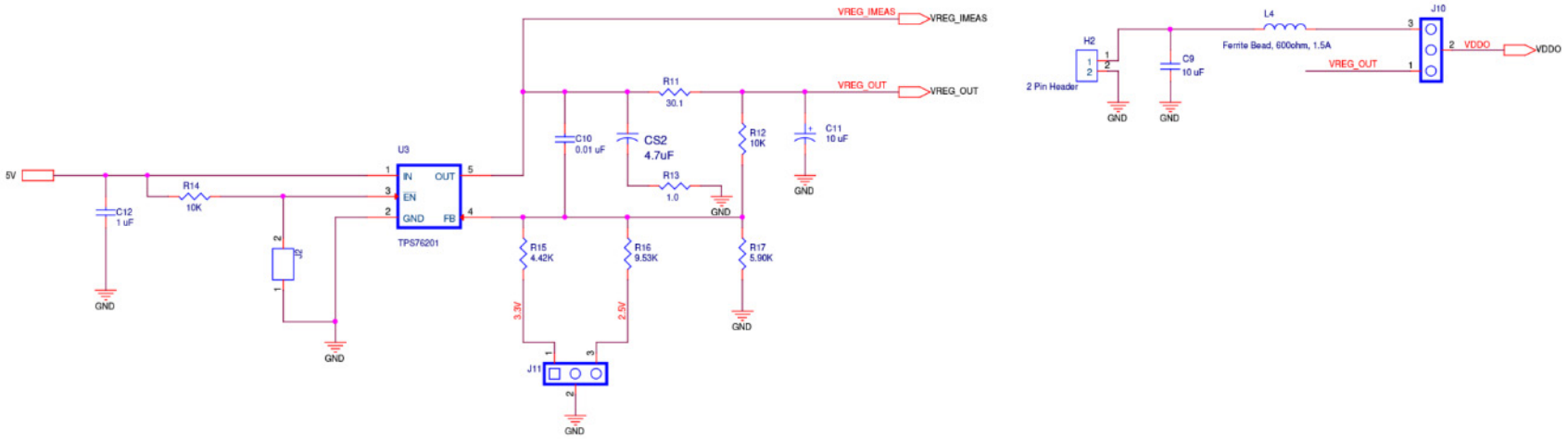

Figure A5. SiT6503EB ODR0 Supply Diagram

ODR3 Supply

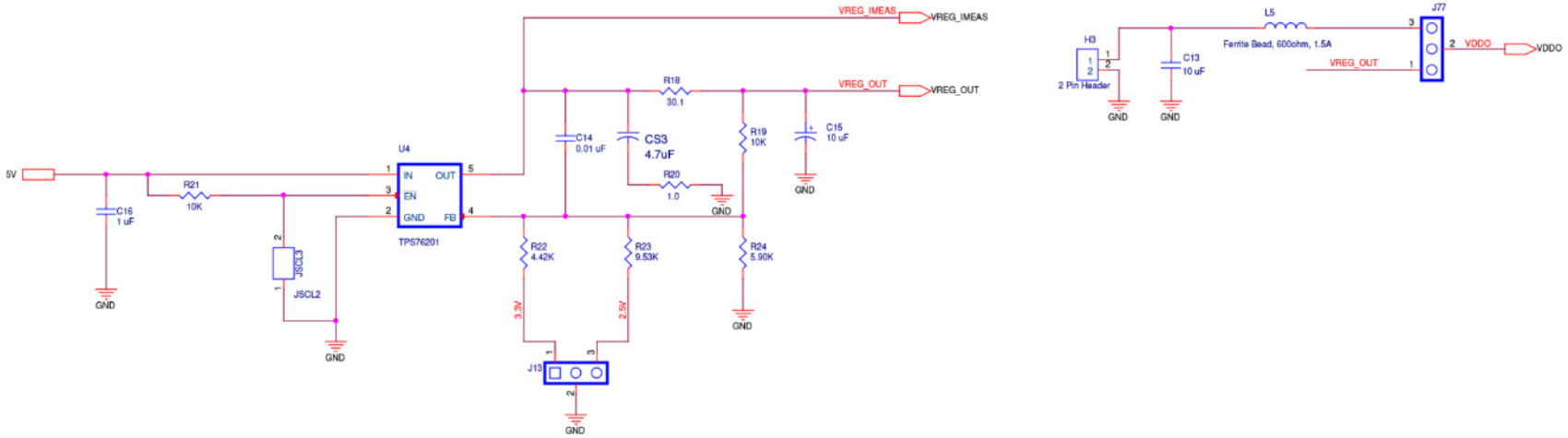

Figure A6. SiT6503EB ODR1 Supply Diagram

ODR4 Supply

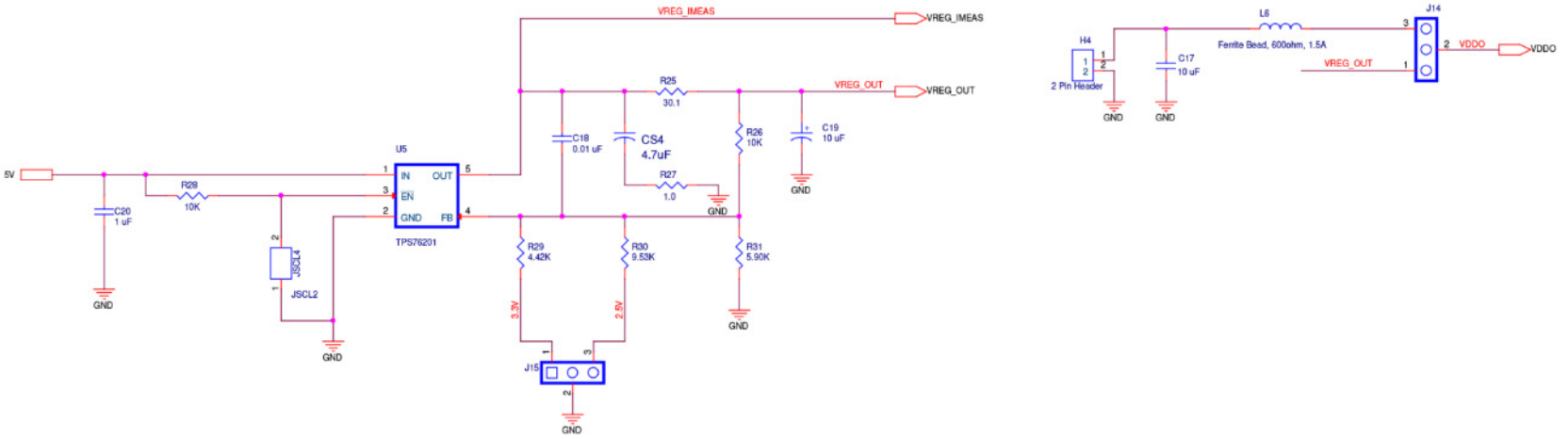

Figure A7. SiT6503EB ODR2 Supply Diagram

ODR5 Supply

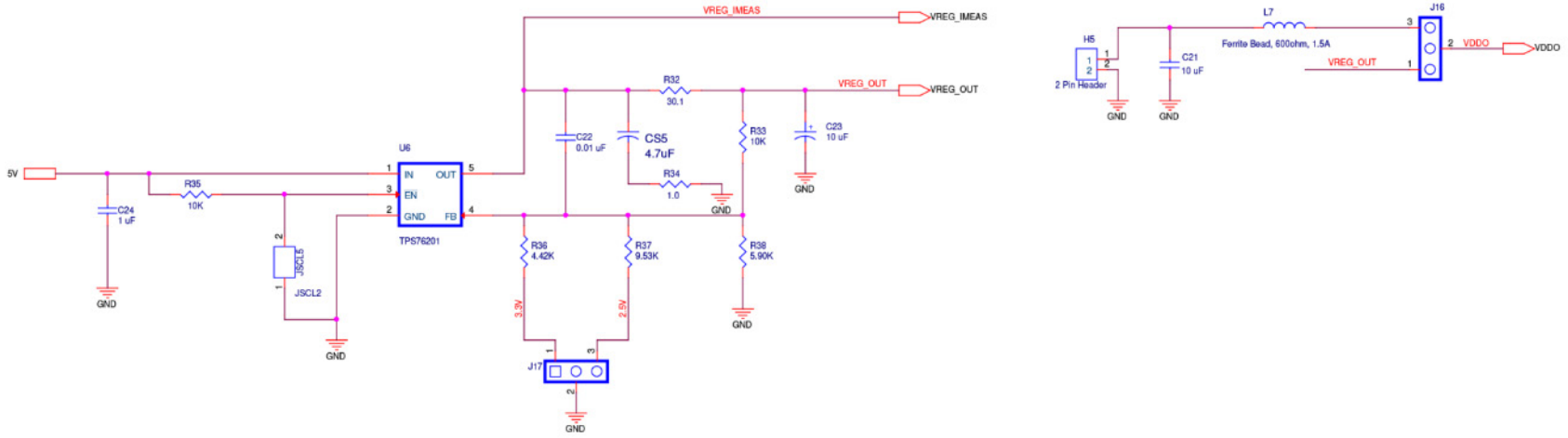

Figure A8. SiT6503EB ODR3 Supply Diagram

ODR6 Supply

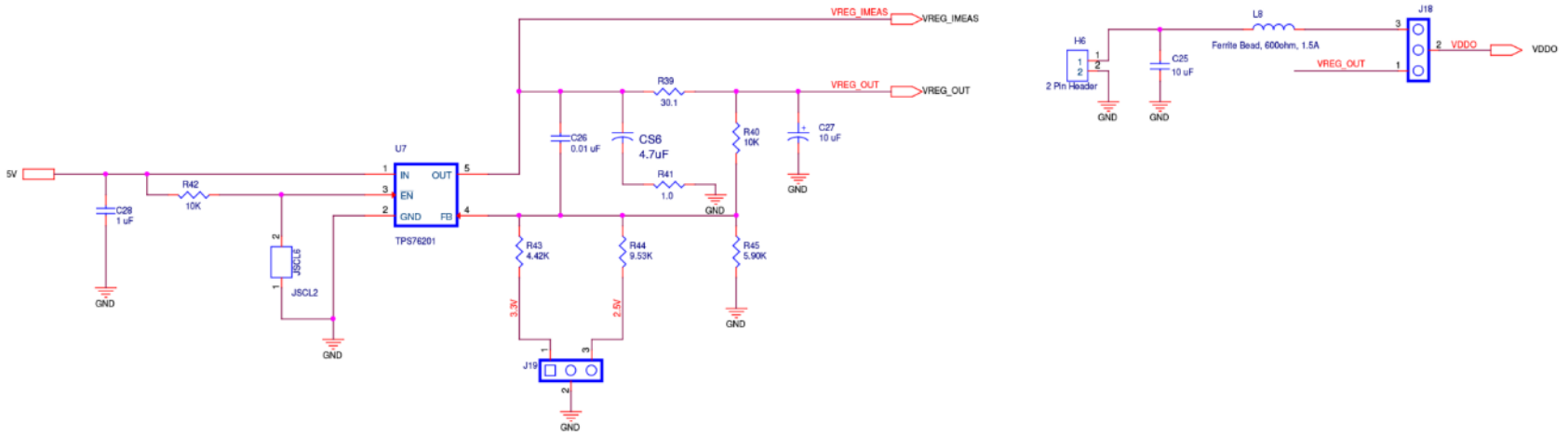

Figure A9. SiT6503EB ODR4 Supply Diagram

ODR7 Supply

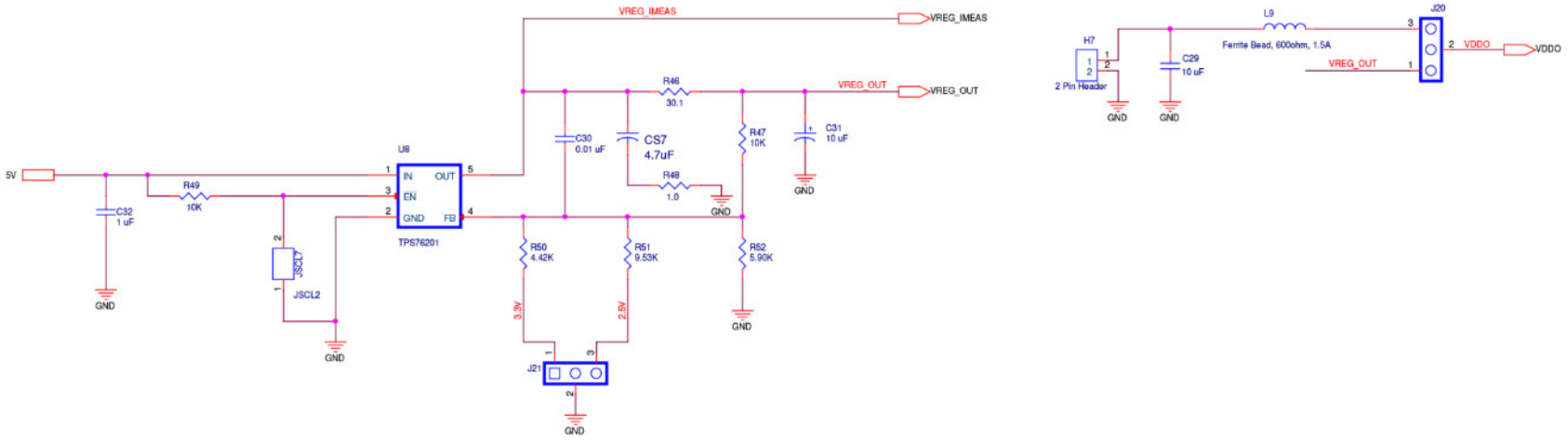

Figure A10. SiT6503EB ODR5 Supply Diagram

ODR8 Supply

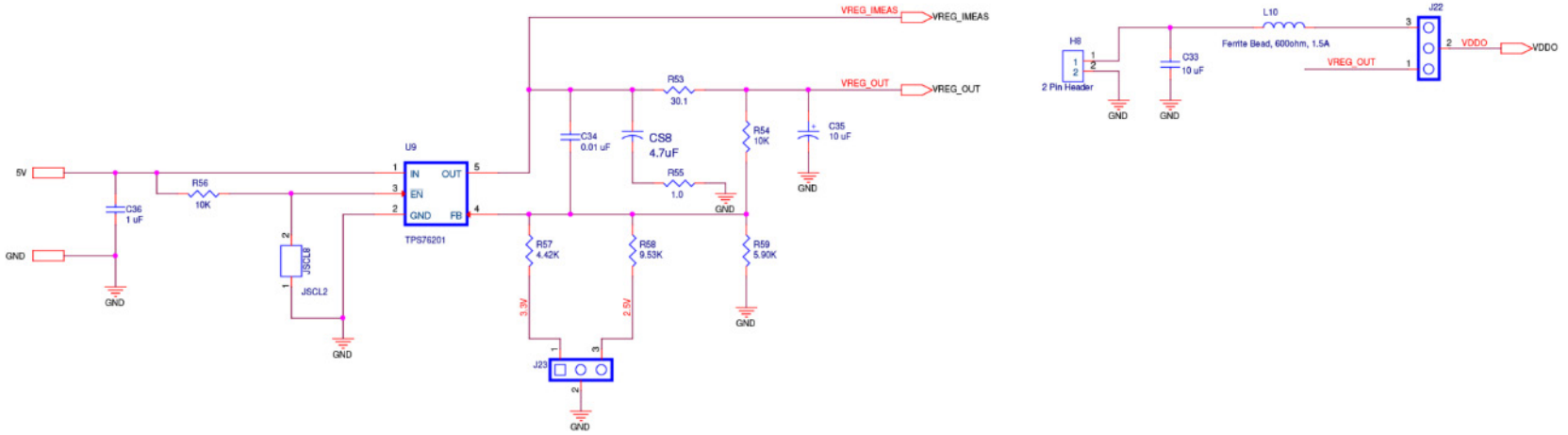

Figure A11. SiT6503EB ODR6 Supply Diagram

ODR9 Supply

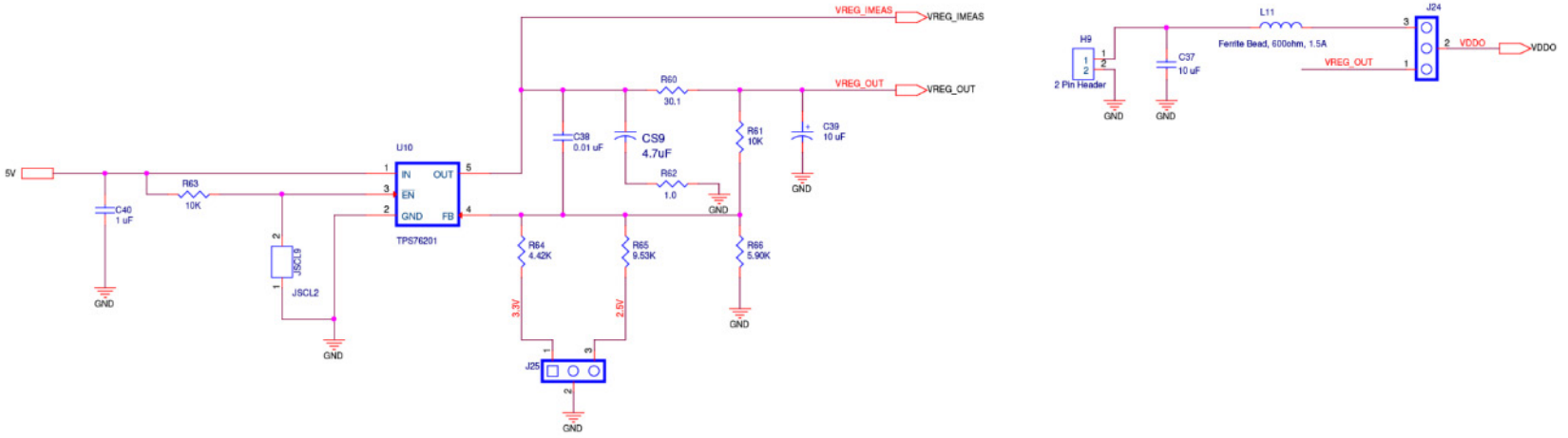

Figure A12. SiT6503EB ODR7 Supply Diagram

ODR10 Supply

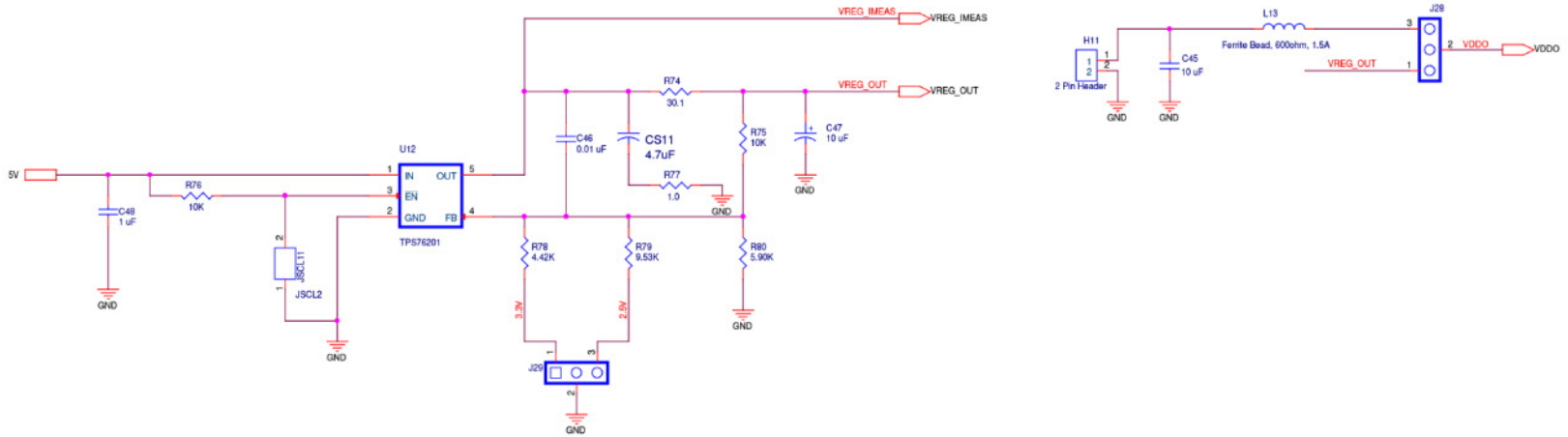

Figure A13. SiT6503EB ODR10 Supply Diagram

FTDI Supply

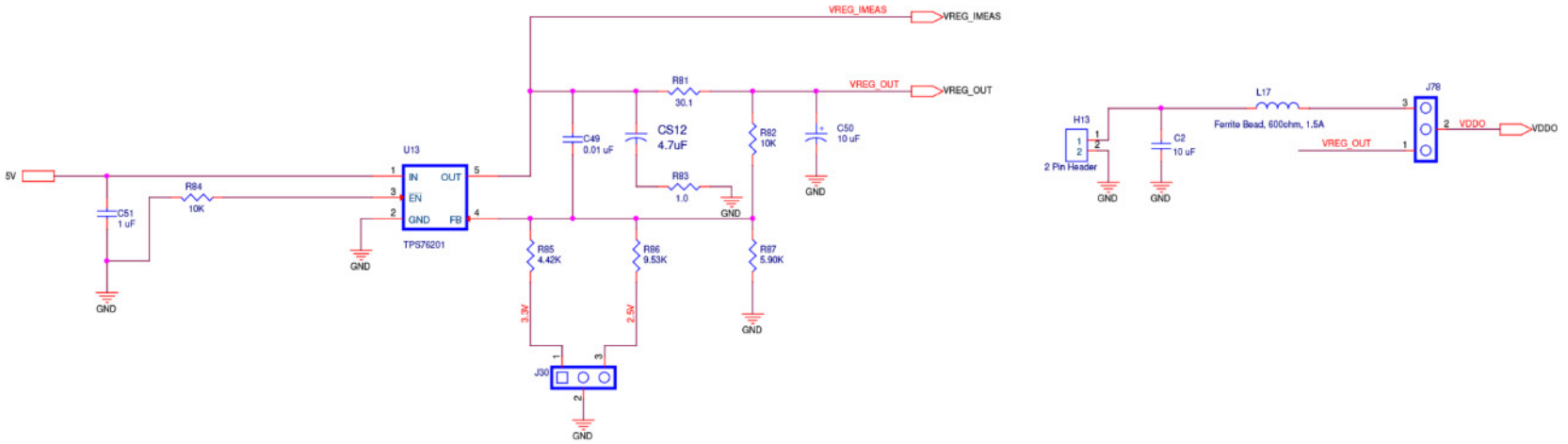

Figure A14. SiT6503EB FTDI Supply Diagram

PLLs Supply

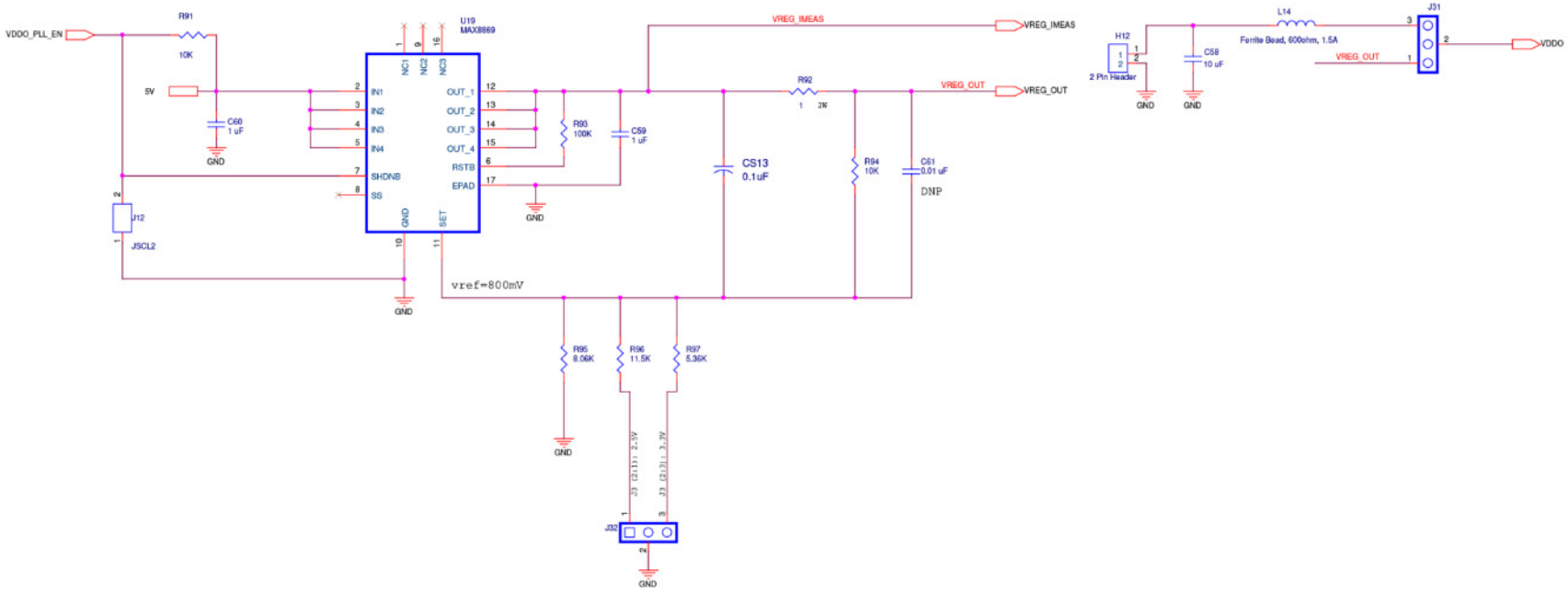

Figure A15. SiT6503EB PLLs Supply Diagram

INPUT CLKS

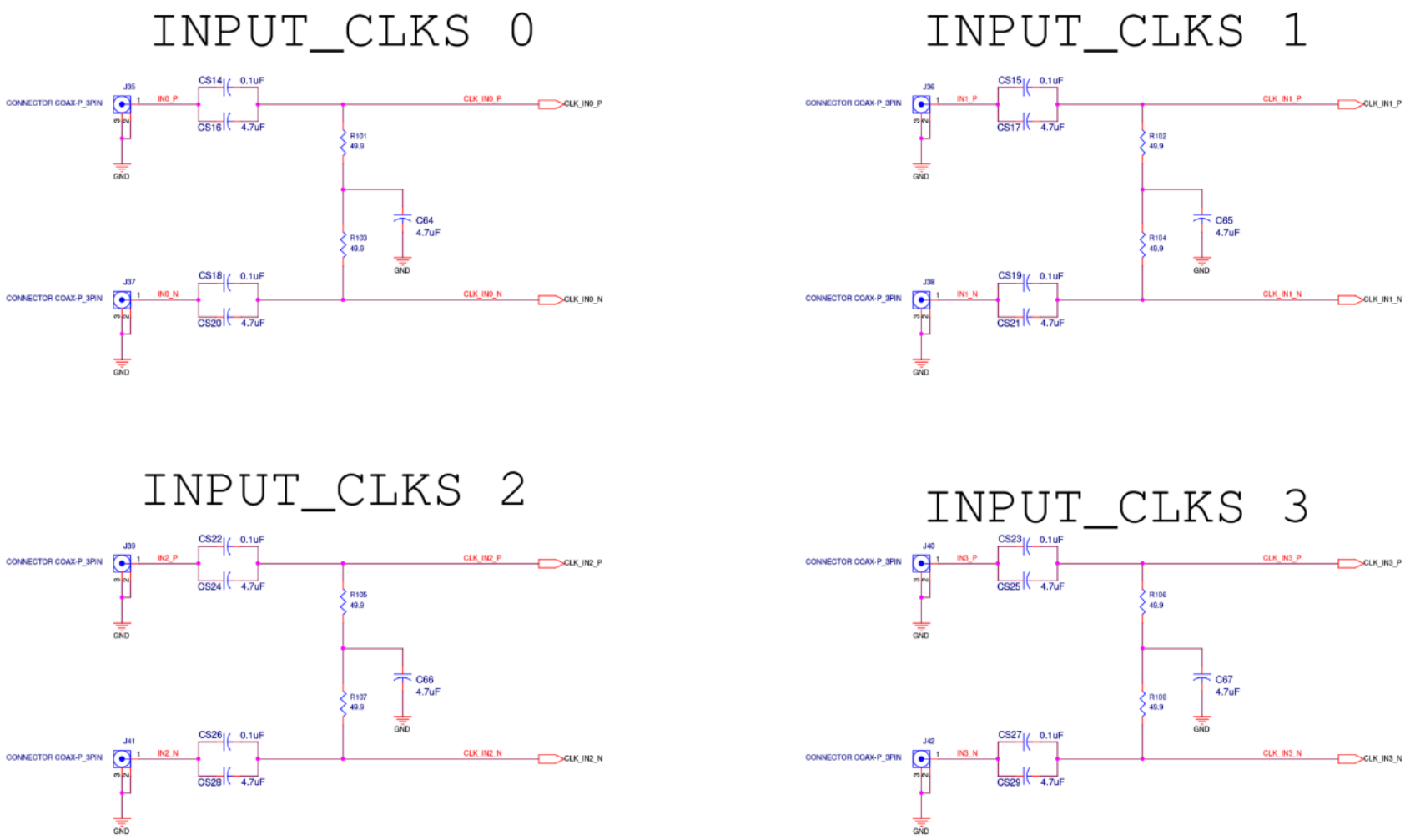

Figure A16. SiT6503EB INPUT CLKS Diagram

OUTPUT CLKS

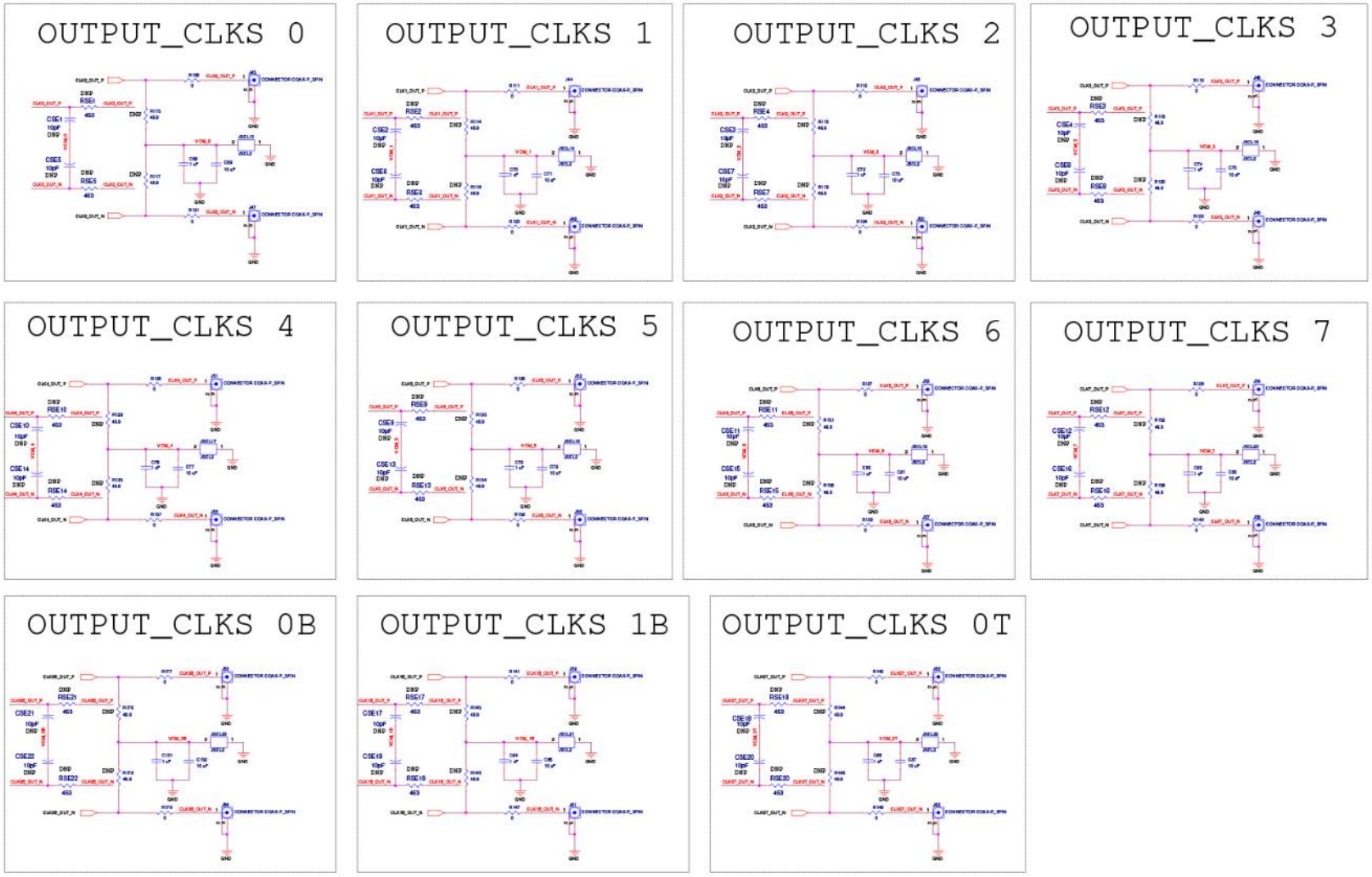

Figure A17. SiT6503EB OUTPUT CLKS Diagram

STATUS LEDS – 2

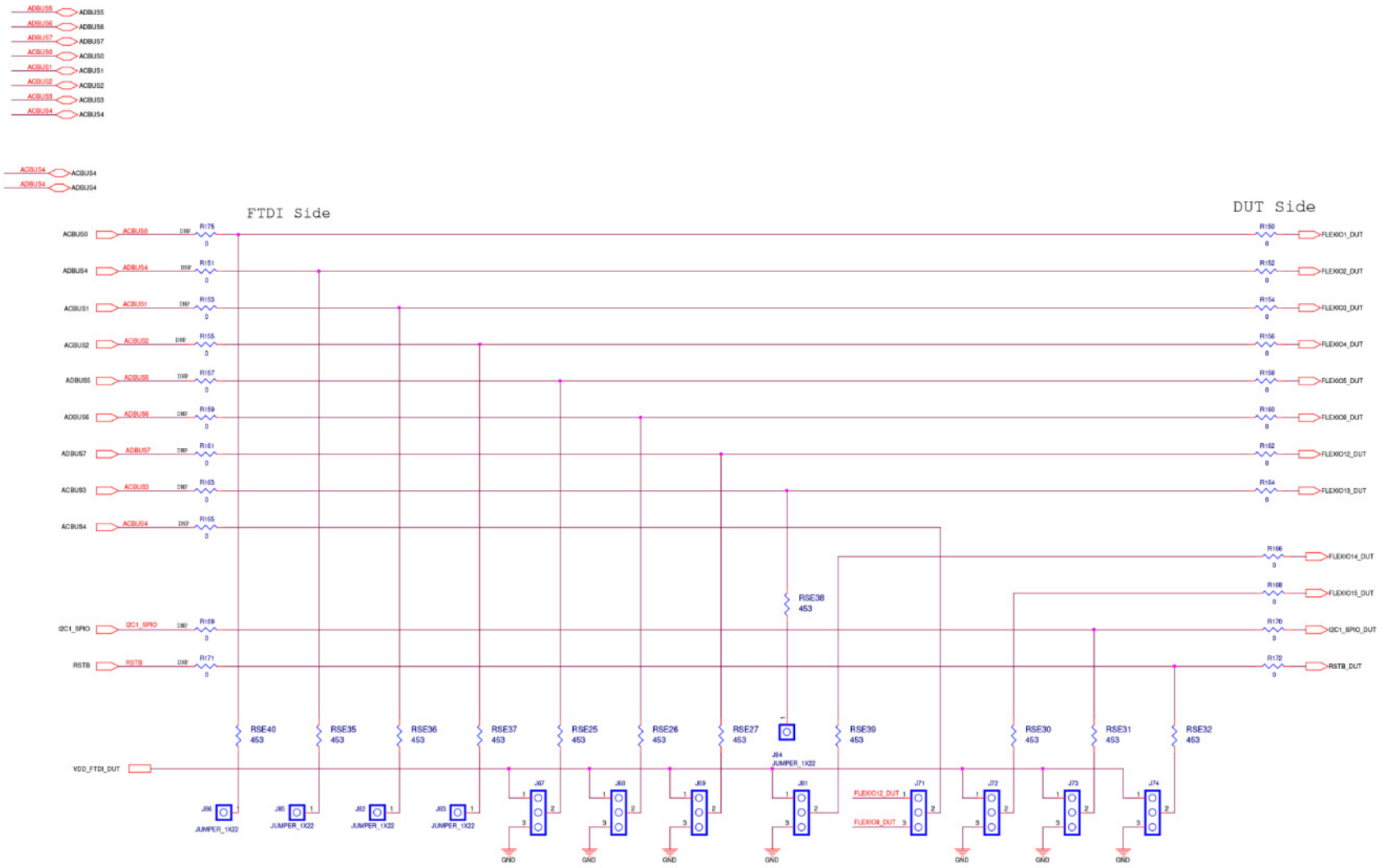

Figure A18. SiT6503EB STATUS LEDS – 2

QFN SiT95148 DUT

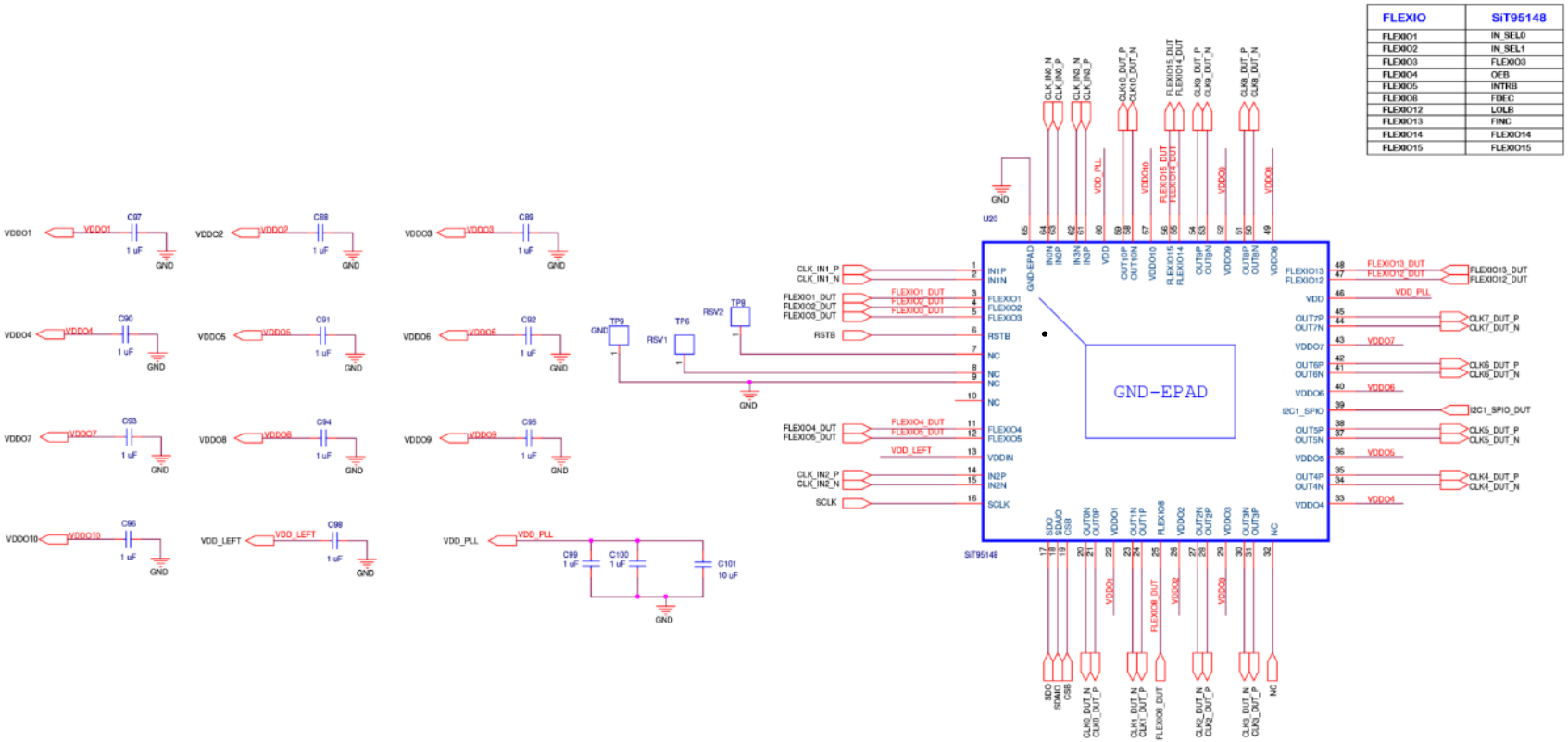

Figure A19. QFN SiT95148 DUT Diagram

FTDI

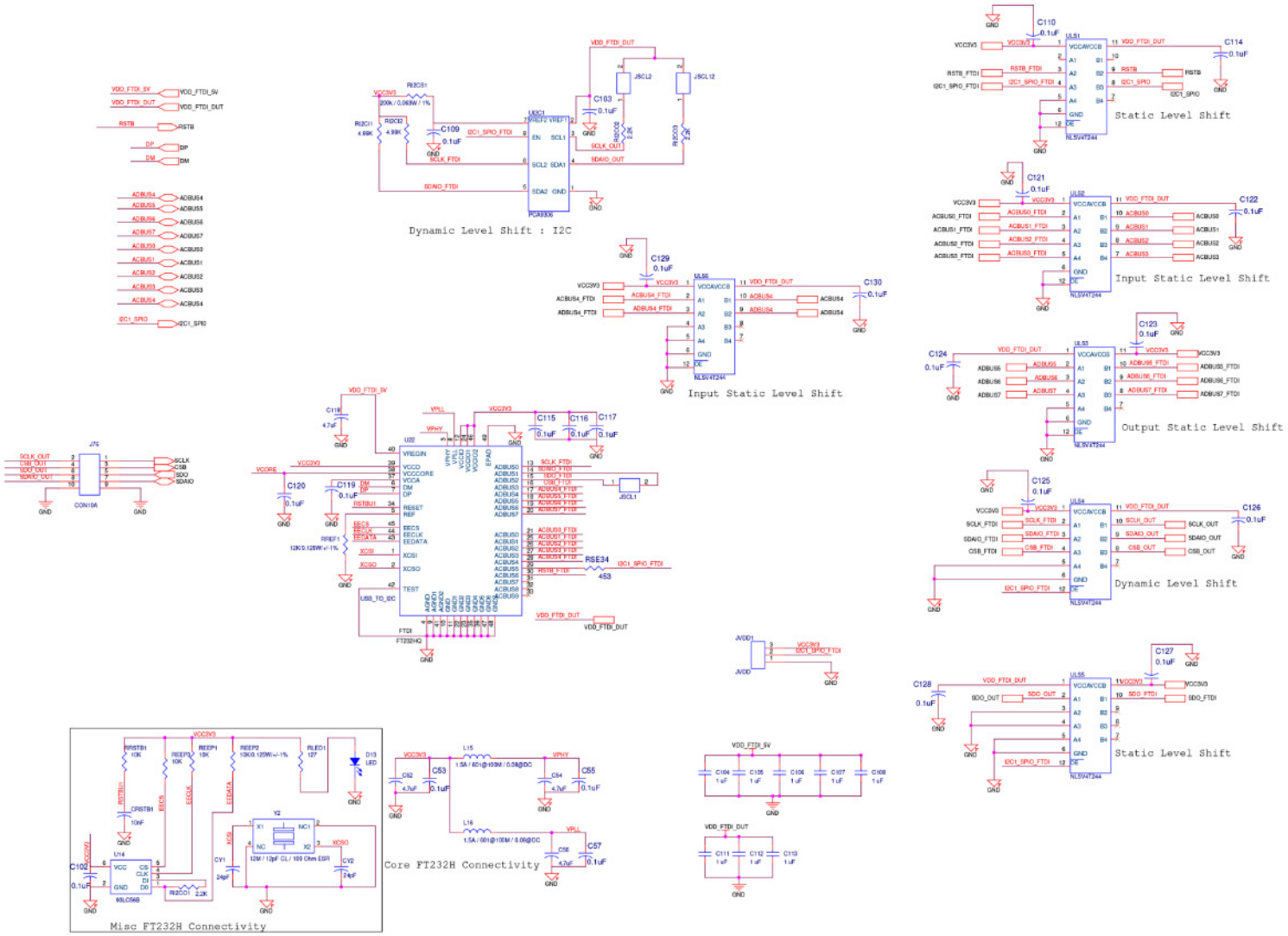

Figure A20. SiT6503EB FTDI Diagram

Appendix B: EVB Top View

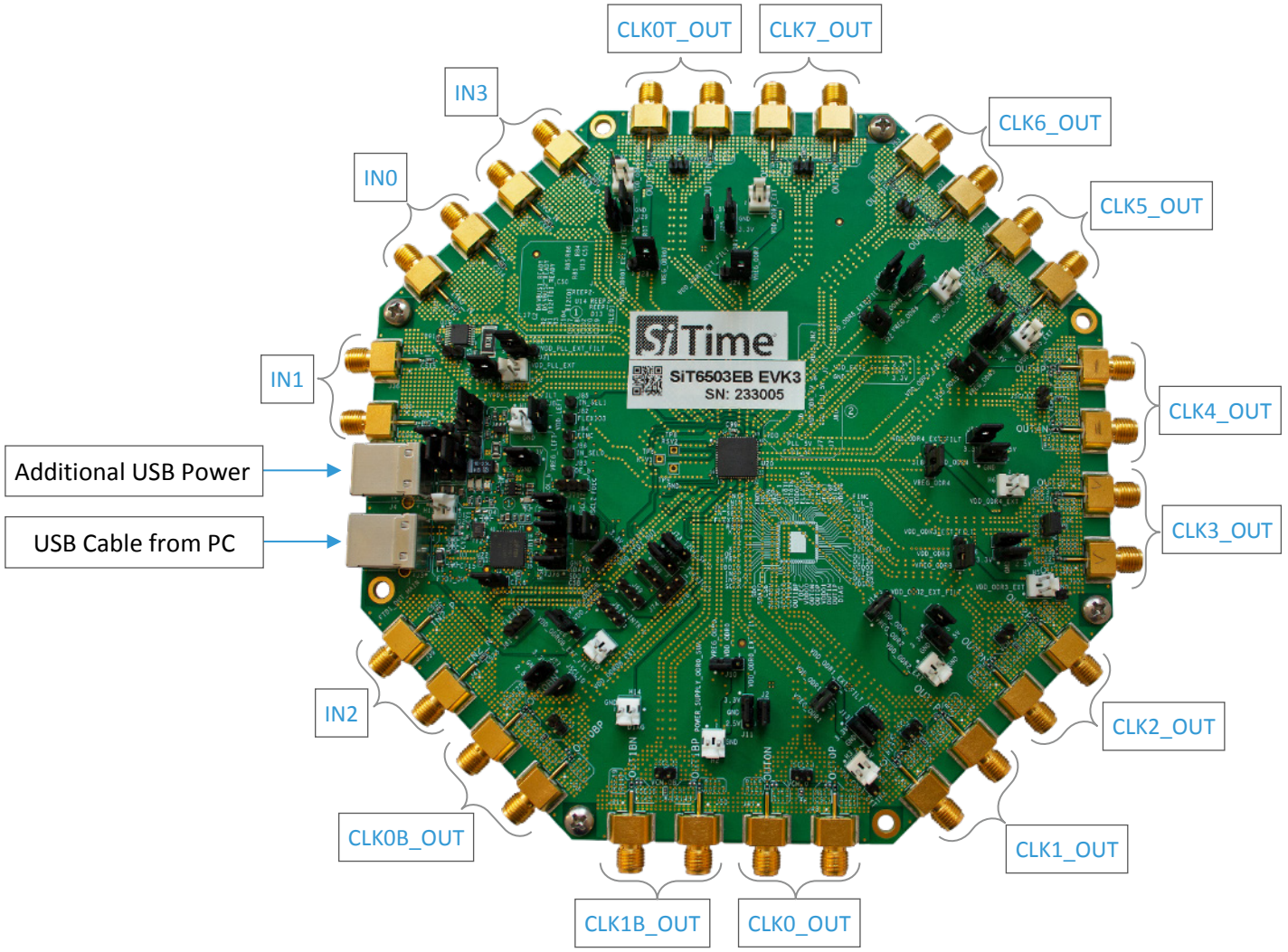

Table 11. Revision History

Version	Release Date	Change Summary
1.01	11/26/2019	Original doc
1.02	08/06/2020	Tables 7 – 10 changed Correct EVB Figures 8 and A17 Updated board images Minor edits

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