Cascade™ MEMS Clocks | Frequency Asked Questions

1. 5G and Timing

1.1. What is 5G and its vision?

5G is envisioned to deliver mobile broadband with extreme speeds and capacity, ultra-high reliability and low latency, and support massive machine-to-machine connectivity, according to 3GPP and other industry organizations.

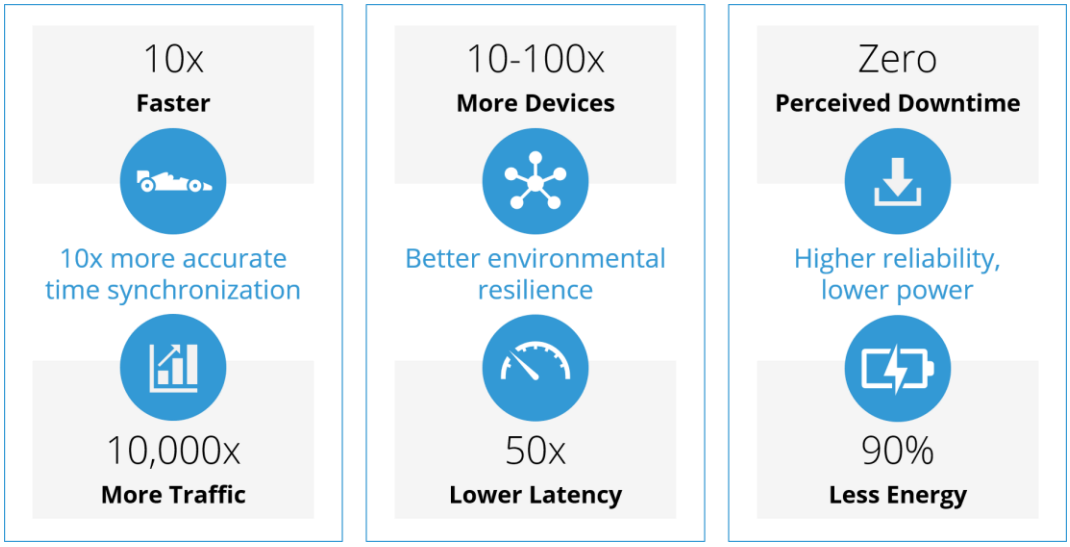

Figure 1: 5G Vision and Timing Needs

Various industry sources have previously communicated that 5G requires 10 times more network equipment because of the use of (a) millimeter wave radios with short coverage distance to deliver ultra-high bandwidth, i.e. more radios are required to get same levels of coverage as previous cellular technologies and (b) edge servers to reduce latency and deliver data faster/closer to consumers.

Three industry trends underpin the evolution and the deployment of the 5G infrastructure to support 10x more equipment:

- Higher bandwidth: 5g network uses new technologies such as massive MIMO and 400G optical transports to support 10x faster mobile download and 10,000x more traffic
- Cloudification: 5G replies on a cloud-based infrastructure such as carrier-grade Ethernet to connect all the equipment to achieve maximum cost and bandwidth efficiency
- Densification: 5G needs to deploy much closer to the end users, resulting in equipment being placed in uncontrolled environments – roadside, rooftop, building basements, co-location with street lighting, traffic lights, stadiums, etc.

The higher bandwidth, cloudification and densification of the 5G network leads to 10x more stringent requirements on timing.

1.2. What is new about timing in 5G?

5G cloudification requires a time-sensitive network (TSN) with end-to-end time synchronization accuracy of 130 ns to deliver 5G connectivity through cloud infrastructure. Not only is this requirement 10 times more stringent than the 1500 ns requirement in 4G, and but it also must be delivered over Ethernet infrastructure using packet-based IEEE 1588 precision timing protocol (PTP). High performance timing solutions such as network synchronizers, precision TCXOs and OCXOs are critical to delivering this extremely tight synchronization requirement.

In addition to synchronization solutions, 5G also needs extremely low noise and low jitter timing components to support high bandwidth equipment such as 400G optical modules and massive MIMO radios.

1.3. Why is reliable and resilient timing critical to 5G?

Extremely reliable, environmentally resilient timing components are critical to deliver the 5G vision of ultra-bandwidth and massive machine-to-machine communication that must provide zero downtime.

5G achieves higher mobile download speed, more capacity and lower latency through network densification, by adding more cell sites, more communication equipment, and more edge servers closer to the consumers.

Network densification also means that equipment is placed in whatever is space available, such as on rooftops and top of streetlamps, or in roadside cabinets and building basements. The deployment of 5G equipment in these uncontrolled environments requires environmentally-resilient timing components and sub-systems that can deliver 130-ns end-to-end timing synchronization while being subjected to environmental stressors such as airflow, rapid temperature change, high temperature, vibration, and poor power supply.

Densification also means that many of the 5G equipment are in inaccessible locations where any equipment failure may result in prolonged service degradation or outage. Highly reliable timing components and subsystems are critical to 5G network reliability.

1.4. What role does SiTime play in 5G?

SiTime offers a complete portfolio of MEMS timing solutions that include low jitter XOs, precision TCXOs, OCXOs, clock generators, jitter cleaners and network synchronizers. These MEMS solutions are 10 times more reliable and environmentally resilient than traditional quartz-based timing components. Used standalone or together, they deliver the most stable timing under environmental stressors—airflow, rapid temperature change, high temperature, vibration, and poor power supply—for every network node.

2. Product, Market and Technology Overview

2.1. What is Cascade?

Cascade is an innovative MEMS-based clock-system-on-a-chip (ClkSoC™) platform. The Cascade family of MEMS clocks consist of clock generators, jitter cleaners and network synchronizers.

Clocks are the timing heartbeat of communication infrastructure equipment. A traditional clock device uses a quartz-based oscillator or resonator as an input reference for frequency synthesis and jitter cleaning. By integrating a MEMS resonator, the Cascade clock-system-on-a-chip eliminates the dependency on quartz, along with quartz related performance and reliability issues. It brings the benefits of MEMS to 5G RAN, core/edge/access networks and datacenter applications, such as 10 times higher reliability and environmental resilience.

2.2. How large is the market for Cascade?

The Cascade clock-system-on-a-chip targets the $1B silicon clocks market. The size of the market is a SiTime estimate.

2.3. How do Cascade products fit within SiTime's existing product portfolio?

Cascade represents a natural extension of SiTime's timing portfolio from oscillators (frequency control) to clocks.

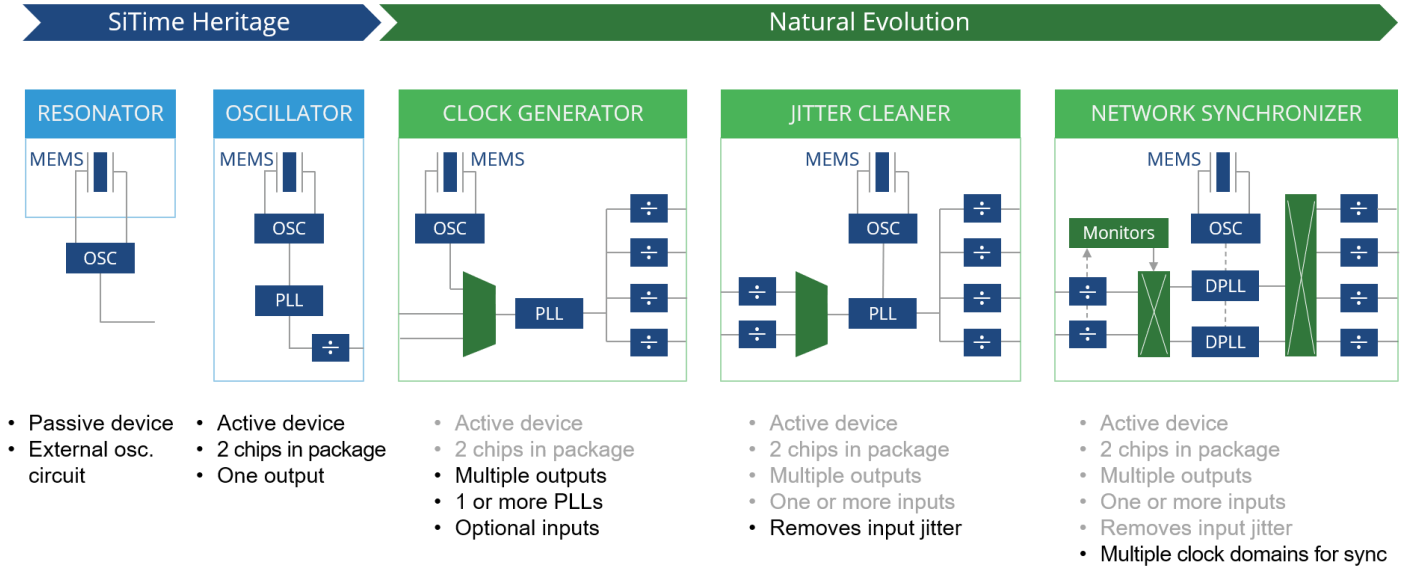

Figure 2: SiTime Core's Core Competence is a Foundation to All Timing Devices

SiTime has shipped over 1.5 billion units of MEMS oscillators. These are one output devices that leverage SiTime's core competence in MEMS resonators, analog design, and system expertise. Cascade clocks are based on the same core competence, but with more outputs and digital clock management features.

Cascade targets the same market and customer base as SiTime's oscillators in communications and enterprise, industrial, aerospace and defense.

2.4. What markets benefit from Cascade products?

With Cascade, SiTime brings the benefits of MEMS to 5G connectivity and datacenters.

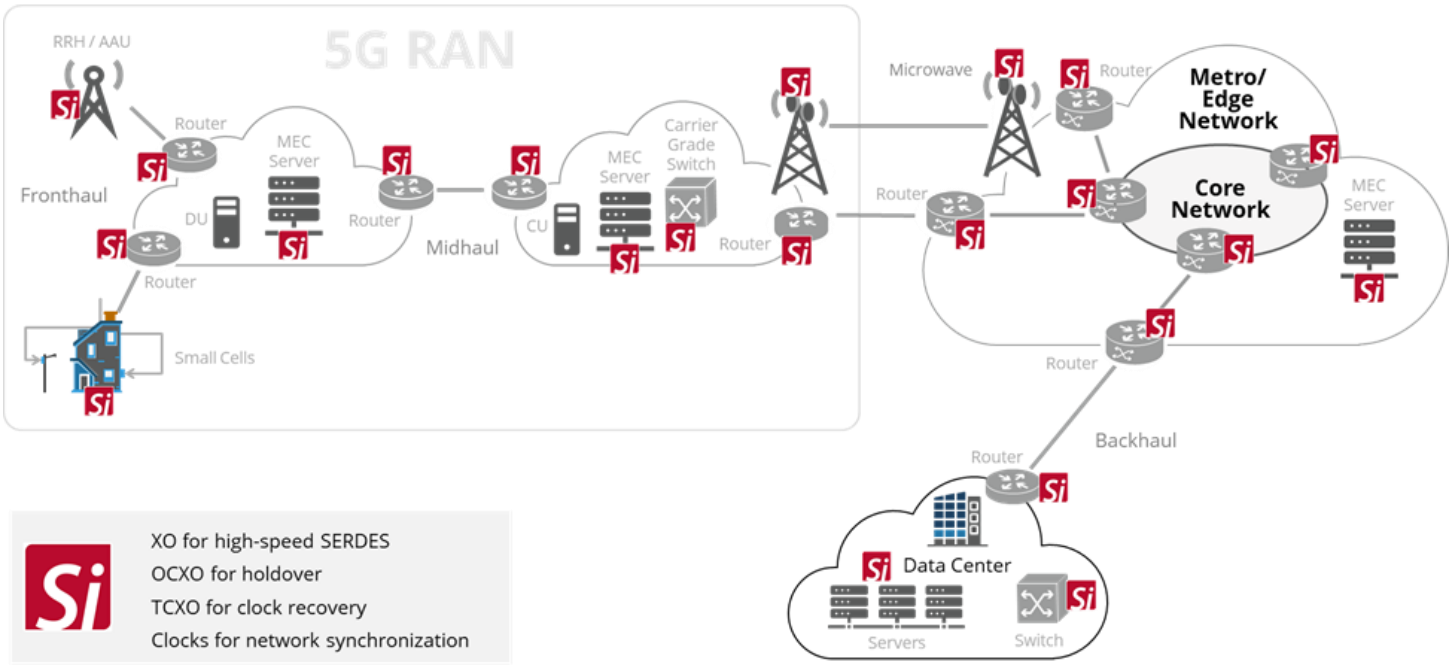

Figure 3: MEMS Solution for Every Network Node

Cascade clock devices are optimized for high reliability communications and enterprise applications. They can be used standalone to consolidate multiple timing components into a single device to provide the highest level of integration. When used together with SiTme's precision TCXO and OCXO, the Cascade devices deliver a complete synchronization (SyncE and IEEE 1588/eCPRI) clock solution for time-sensitive networking (TSN) systems in 5G RAN, wireline (core/metro/edge) and datacenters.

The Cascade clock-system-on-a-chip families also complement SiTime's full portfolio of kHz and MHz oscillators for industrial and aerospace/defense applications.

2.5. How do Cascade clocks work?

The Cascade clock-system-on-a-chip combines SiTime's third-generation MEMS resonator with low noise PLLs to deliver exceptional reliability, environmental resilience, and rich features in a single device.

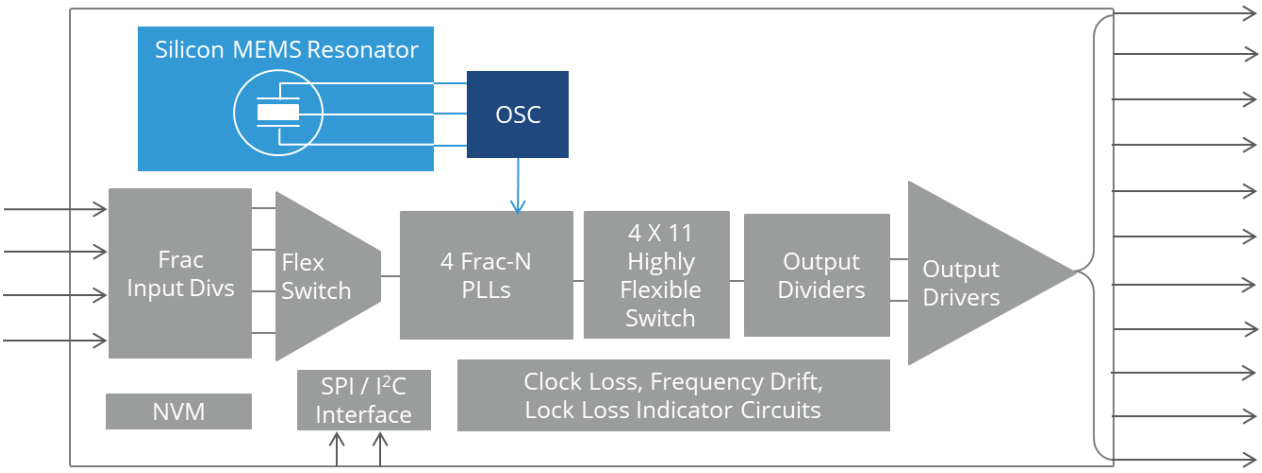

Figure 4: Cascade Clock Architecture

Three key elements of the Cascade clock-system-on-a-chip include:

- Integrated MEMS resonator that eliminates issues with external quartz such as capacitive mismatch, activity dips, susceptibility to shock, vibration, and EMI
- Four PLLs, up to four independent clock domains and programmable PLL loop bandwidth for synchronization applications
- Four inputs, up to 11 outputs with flexible frequency translation to support maximum consolidation of timing components in a design

The Cascade clock-system-on-a-chip are equally well suited for other high reliability applications such as broadcast systems, test instrumentation and power grid infrastructure.

2.6. What products are available with the launch of the Cascade Platform?

The Cascade clock-system-on-a-chip platform includes three product categories and five products.

- Clock generators: 10-output SiT95141 and 11-output SiT95143 for timing component consolidation
- Jitter cleaner: 10-output SiT9145 for removing input clock jitter and distributing cleaned-up clocks within a system
- Network synchronizers: 8-output SiT95147 and 11-output SiT95148 featuring 4 independent clock domains for SyncE and IEEE 1588 applications in addition to jitter cleaning and clock distribution functions

2.7. What are the key differentiators of Cascade products?

Communications and enterprise systems have previously used clock ICs with quartz references to integrate multiple timing functions and distribute clock signals in the system. SiTime's Cascade clock-

system-on-a-chip utilizes a new, all-silicon clock architecture and provides more integration by replacing the quartz reference with an internal MEMS resonator.

With SiTime's proven MEMS technology, the Cascade clock-system-on-a-chip enables:

- 10 times higher reliability, eliminating quartz-related field failures
- 10 times more resilience to supply noise, EMI, shock, vibration, and board bending
- Simplifies design, reduces BOM, speeds up system development
- 35% space saving

The Cascade clock-system-on-a-chip ships in two forms for optimal supply chain considerations:

- Blank ISP (in-system programmable) devices provide maximum flexibility in use cases and inventory management
- Pre-programmed devices enable system boot up without software configuration for maximum simplicity in design and manufacturing

2.8. What are the key features and specifications of Cascade products?

Cascade clock-system-on-a-chip includes 5 products with different features for different applications.

Table 1: Cascade Product Summary

Category	Part #	# of Inputs	# of Outputs	# of PLLs	# of Clock Domains	Jitter Cleaning	Prog. Loop Bandwidth	Hitless Switching	Low Wander Mode
Clock Generator	SiT95141	4	10	4	1	-	-	-	-
	SiT95143		11		4				
Jitter Cleaner	SiT95145	4	10	4	1	✓	✓	✓	-
Network Synchronizer	SiT95147	4	8	4	4	✓	✓	✓	✓
	SiT95148		11						

Cascade Clock-system-on-a-chip platform key specs and features:

- Integrated MEMS resonator that eliminates quartz related performance and reliability issues
- Flexible input to output frequency translation with jitter attenuation, 4 inputs, up to 11 outputs
- Wide output frequency support
  - Differential outputs from 8 kHz to 2.1 GHz
  - LVCMOS outputs from 8 kHz to 250 MHz
  - 1 PPS (pulse-per-second) on one output
- Wide input frequency support
  - Differential input from 8 kHz to 750 MHz
  - LVCMOS input from 8 kHz to 250 MHz

- Individually configurable output formats and VDD Supply
    - LVPECL, CML, HCSL, LVDS or LVCMOS
    - 1.8V, 2.5V or 3.3V
- Programmable jitter attenuation bandwidth for each PLL: 1 mHz to 4 kHz
- Synchronized, holdover or free run operation modes
- Hitless clock inputs with auto or manual switching
    - Sub 50 ps phase build out mode transients
    - Phase propagation with programmable slopes
    - Frequency ramp for plesiochronous clocks
    - Robust and fast cycle slip and frequency step detection for input frequency steps (clean frequency tracking for large frequency steps)
- Locks to gapped clock inputs to support OTN
- Programmable frequency ramp slopes for switching plesiochronous clocks
- DCO mode via I2C or SPI with 0.005 ppb resolution
- Programmable output delay control
- Repeatable input to output delays for each power up of chip
    - Zero delay buffer mode
    - Output wake up sync with an independent clock
- Chip status monitoring indicators: Lock Loss, Clock Loss, Frequency Drift
- Industry standard 64-pin 9 x 9 mm package

2.9. What is the availability of Cascade products?

All five Cascade devices – SiT95141, SiT95143, SiT95145, SiT95147, SiT95148 – are sampling now. Volume production is slated for Q4 2020.

2.10. What applications do Cascade products target?

The Cascade clock-system-on-a-chip platform is ideal for:

- 5G remote radio units (RRU), active antenna units (AAU)
- 5G small cells
- Microwave backhaul
- DU (distributed unit)
- CU (centralized unit)
- Base stations
- Fronthaul switches and routers
- Carrier grade Ethernet routers and switches
- Optical transport network (OTN) clocking for framers, mappers and processors
- PON OLT
- Cable modem termination systems (CMTS), remote PHY
- Multiaccess edge computing (MEC) servers
- Datacenter switches or top-of-the-rack (ToR) switches
- Satellite communication systems
- Broadcasting systems
- Test and measurement instrumentation

2.11. What customer problems are solved by Cascade in these applications?

Traditional clock ICs need quartz resonators as an input clock reference. This dependency causes many system reliability, design, and performance issues:

- Prone to field failures as quartz is 10 times lower in reliability compared to semiconductor devices
- System performance degradation due to quartz susceptibility to EMI, vibration, board bending and activity dips (frequency jumps)
- Multiple design and test cycles to ensure proper quartz oscillator circuit. Load capacitance mismatch can cause inaccuracy in the output frequencies of the clock IC
- Additional BOM and space due to external quartz and load capacitors

The Cascade clock-system-on-a-chip products eliminates all the above quartz issues by integrating SiTime's proven MEMS resonator technology within the clock IC.

2.12. Does the Cascade platform achieve any industry firsts?

Cascade clock-system-on-a-chip devices are the first to offer the following:

- Network synchronizer with integrated MEMS, eliminating quartz reference
- Jitter cleaner with integrated MEMS, eliminating quartz reference
- Clock generator/frequency synthesizer with integrated MEMS, eliminating quartz reference

2.13. What customer feedback has SiTime received on Cascade?

Customers have provided the following comments:

- "My design is dense and tight on space. Cascade does not require an external reference and helps save space."
- "It usually requires multiple PCB spins to get a resonator circuit to work properly. With Cascade, I don't have to worry about that, and my development time is much shorter now."
- "Using an external resonator can affect jitter which is important to my design. With Cascade, that is not an issue since a MEMS resonator is already integrated in the clock IC."
- "Reliability is a huge concern for my application, where we see MEMS having a clear advantage over quartz solutions."

2.14. What is the difference between Cascade and traditional clock devices?

Traditional clock ICs need quartz resonators (crystal) to create an input clock reference for the PLL(s). Designing a PCB with an external quartz component exposes sensitive analog nodes that provide a path for EMI and board noise to couple into the oscillation circuit. Proper PCB design needs to minimize such coupling. An external crystal must also be designed with a load capacitor that is chosen to match the characteristics of that specific crystal, which varies from model to model even within the same manufacturer. Load capacitor matching requires careful design to provide accurate, stable, and reliable operation across temperature. The crystal and load capacitor also require additional board area, which can increase cost in space-constrained designs. Load capacitors are historically prone to supply-chain management issues. Finally, crystal performance (phase noise) degrades when subjected to mechanical shock or vibration, such as from fans, or environmental stressors when deployed outdoors.

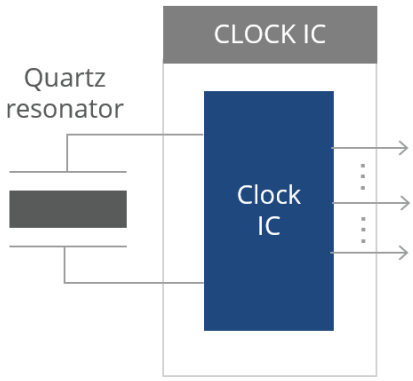

Figure 5: Traditional Clock Require External Quartz

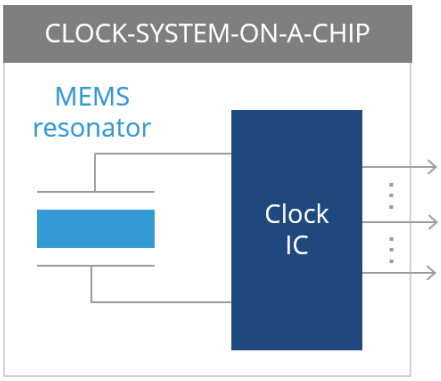

Figure 6: MEMS Clock with Integrated MEMS Resonator

The Cascade clock-system-on-a-chip integrates a MEMS resonator and eliminates all quartz-related issues. This MEMS integration increases reliability and simplifies the overall design effort by reducing component count, circuit complexity, exposure to system noise, board real estate, and time to market.

2.15. Can traditional clock vendors integrate resonators to achieve the same level of integration as Cascade?

Integrating a quartz resonator with a clock device in the same package does NOT resolve the fundamental issues of using quartz as a reference. These problems include being prone to field failure, susceptible to environmental stressors (shock, vibration, board bending, EMI), activity dips, frequency jumps and circuit design challenges with capacitive mismatch.

Additionally, integrating quartz into a plastic package containing a higher-power IC exposes the crystal to larger thermal gradients compared to mounting it separately on a PCB. This makes the overall solution more unreliable and prone to field failures.

3. Application Examples

3.1. 5G RRU

The Cascade clock-system-on-a-chip enables 10 times better environmental resilience and provides the flexibility to deploy a single design globally.

- 10x more vibration resistant
- Reliable startup at cold temperatures
- Eliminates quartz-related reliability field failures

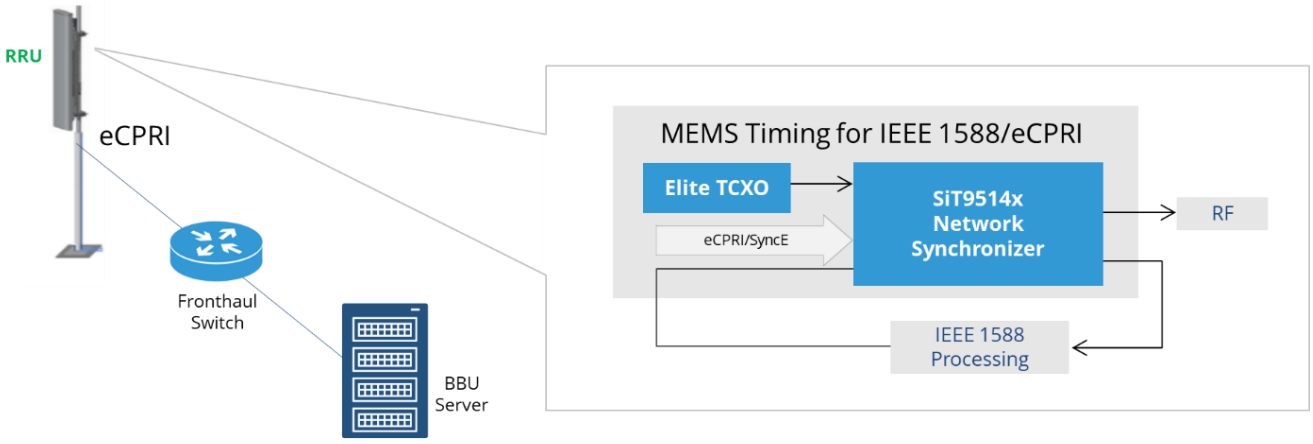

Figure 7: MEMS Solution for 5G RRU

3.2. 5G Front haul switch

The Cascade clock-system-on-a-chip enables 10 times better environmental resilience and the most robust system operation.

- Enhance robustness: flexible hitless switching and input monitoring for fail-safe
- Ensure <15 ns accuracy in real world conditions: resistant to temp change, airflow, vibration
- Minimize field failure: eliminate quartz as single points of failure

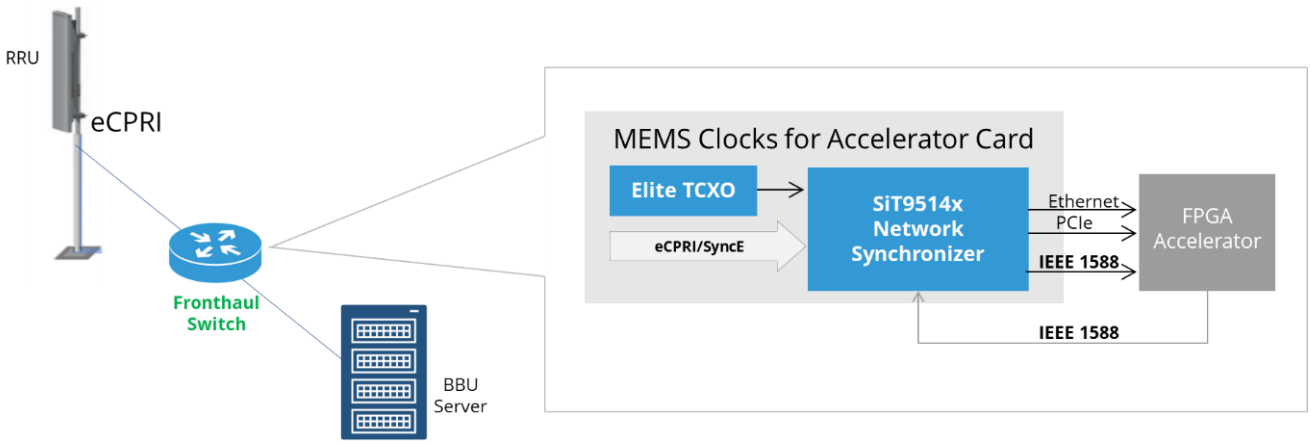

Figure 8: MEMS Solution for 5G Fronthaul Switch

3.3. Top-of-the-rack switch

The Cascade Clock-system-on-a-chip consolidates all clocks in datacenter switches

- 10x more reliable, eliminating quartz-related field failures
- 10x more resilient to supply noise, EMI, shock, and board bending
- Simplifies design, saves space, reduces BOM, speeds time to market

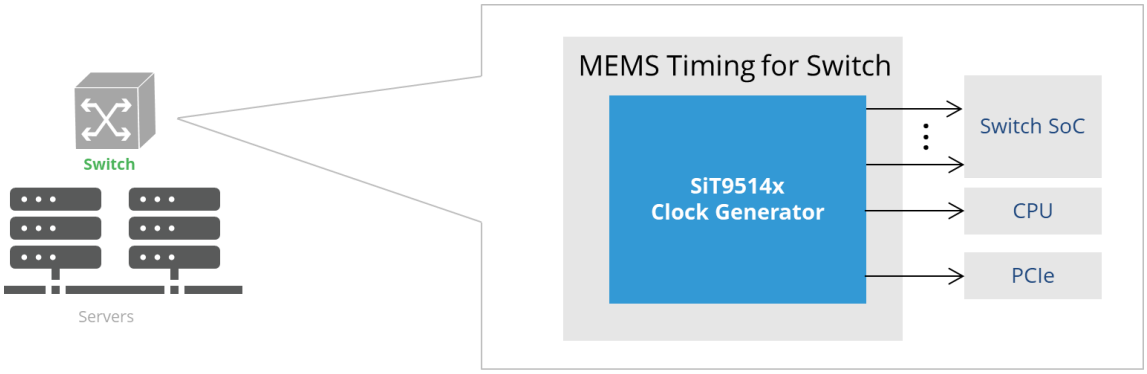

Figure 9: MEMS Solution for Datacenter Switch

4. Terminology

4.1. What is a clock?

A clock device refers to a category of timing components that typically generate and distribute multiple outputs of the same or different frequencies within a system. Some clock devices can also accept one or many input frequencies from which output frequencies are synthesized.

Other types of timing devices include oscillators and resonators, both of which can be used as reference sources for clock devices.

4.2. What are the different categories of clocks?

At the highest level, there are four categories of clock devices.

- Buffer
- Clock generator
- Jitter cleaner
- Network synchronizer

A buffer is the simplest of clock devices. It provides multiple copies of an input clock and distributes them to multiple ICs with the same frequency, across a PCB.

The other three clock types are more complex and integrate phase-locked loops (PLLs). They typically require an external oscillator or resonator as a reference to synthesize multiple output frequencies required by a system. The remainder of this document focuses on these non-buffer clock types.

4.3. What is a clock generator?

A clock generator (CG) is a PLL device that can generate multiple outputs of the same or different frequencies from an internal resonator or an input clock.

A GC is typically used to consolidate multiple oscillators and resonators on the same PCB into a single device for BOM consolidation and more integrated system clock design.

4.4. What is a jitter cleaner?

A jitter cleaner (JC), or jitter attenuator, is typically a multi-input, multi-output device. It uses a low-noise low-bandwidth PLL along with a reference oscillator or resonator to remove jitter from one or multiple input clocks to generate less jittery, cleaner output clocks of the same or different frequencies. For example, a jitter cleaner can take a noisy 1 ps rms (jittery) input and generate one or multiple clean, 0.2 ps rms jitter outputs, that have 5 times lower jitter than the input clock.

A jitter cleaner is typically used in high speed data communication systems where it accepts a recovered clock from an incoming high-speed data signal, and removes jitter on this recovered clock, so the system can use the clean recovered clock to re-time data back onto the line. This operation ensures the transmitted data is frequency synchronous to the received data and minimizes accumulation of jitter in the data signal as it propagates through the network.

In addition to removing jitter, a jitter cleaner typically includes many clock management features including:

- Input-output frequency and level translation (e.g., translating a 25-MHz LVCMOS input into a 156.25-MHz LVCPEL differential output)
- Programmable PLL loop bandwidth to support different application protocols
- Hitless switching (some jitter cleaners) between different input clocks for redundancy
- Chip operation status monitoring
- Single clock domain

A jitter cleaner is used to enable distribution of high speed, low noise clocks on a PCB or within a system.

4.5. What is a network synchronizer?

A network synchronizer is a multi-PLL, multi-clock-domain timing device designed to support synchronization applications such as synchronous Ethernet (SyncE) and IEEE 1588. The device typically features multiple inputs and outputs with the ability to route individual inputs to a group of outputs via a chosen PLL. It also enables a user to synchronize the outputs to clocks recovered from the network or another timing source such as a GNSS using SPI or I^2C. This represents the essential function of the network synchronizer – to enable the system to synchronize its timing to another timing source in the network.

In addition to the network time synchronization function, a network synchronizer typically includes many clock management features including:

- Input-output frequency and level translation (e.g., translating a 25-MHz LVCMOS input into a 156.25-MHz LVCPEL differential output)
- Jitter cleaning
- Programmable PLL loop bandwidth to support different application protocols
- Hitless switching, which is the ability to switch between different input clocks for redundancy without phase disruption at the outputs during switching
- Holdover capability when the input signals are lost, using stored data to control output phase and frequency variation
- Chip operation status monitoring
- Support for multiple clock domains
- Internal configurations to improve wander filtering (i.e. low wander mode)

A network synchronizer is used in all applications that require frequency and phase (time), such as 5G RRU, small cell, edge server, switch and router applications.

4.6. What is a clock tree?

A clock tree is a clock generation and distribution network within a system. It may comprise of all types of timing devices including oscillators, buffers, clock generators, jitter cleaners and network synchronizers.

The complexity of the clock tree depends on the number of ICs that it needs to clock, and the frequency and performance requirements of the receiving ICs.

A clock tree is used in a system to reduce the number of timing devices and also to enable some or all of the clocks within the system to be synthesized from a single reference clock source that some applications require.

Refer to section 3 for clock tree examples using SiTime MEMS timing devices.

4.7. What is frequency synchronization?

Frequency synchronization is a process by which one system or the network node adjusts its clock frequency to run at the same average frequency of a clock source in a different system. SyncE is an example of frequency synchronization where the downstream network device locks onto the clock frequency transmitted from an upstream node at the physical layer. Once locked, the downstream device has the same average frequency as its upstream device.

4.8. What is phase or time synchronization?

Time synchronization is often referred to as phase synchronization. It is a process by which one network node adjusts its notion of time to be the same as a master clock in the network. IEEE 1588 precision time protocol (PTP) is becoming the de-facto standard that facilitates the exchange and synchronization of time in 5G RAN, edge/core networks, and datacenters.

4.9. What is a clock domain?

A clock domain encompasses any signal locked to the same upstream timing reference. A clock domain is a portion of the clock tree that runs asynchronous to another part of the clock tree. Take a network synchronizer with two inputs, two PLLs, and two outputs as an example:

- A 25 MHz input from Input1 is routed to PLL1 which synthesize a 156.25 MHz from the 25 MHz input and routes it to Output1
- A 30.72 MHz input from input2 is routed to PLL2 which synthesize a 122.88 MHz frequency from the 30.72 MHz input and routes the 122.88 MHz to Output2

In this case, the network synchronizer operates two independent clock domains, one for the 25 MHz to 156 MHz clock chain, and another from the 30.72 MHz to 122.88 MHz clock chain.