MEMS Timing Solutions for 100G/200G/400G/800G Optical Modules

SiTime MEMS Timing Benefits

Complete MEMS XO portfolio

- 70 fs and 200 fs jitter grades
- 2016, 2520, 3225 packages
- LVPECL, LVDS, HCSL, Low-power HCSL, FlexSwing™

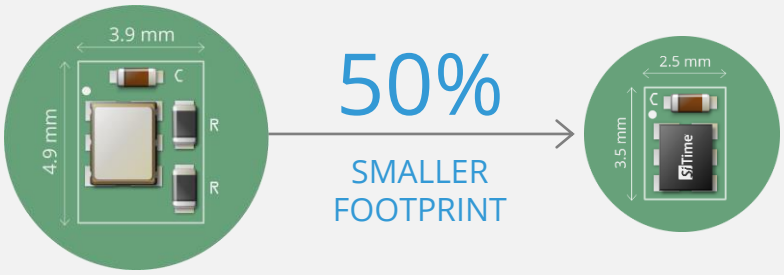
Most robust in real world conditions

- Immunity to supply noise
- 105°C, resistant to heat
- No activity or frequency jumps

Integrated MEMS, easy to use

- 50% smaller
- On-chip LDO reducing BOM
- No quartz reliability issues

Smallest package and integrated resistors – 50% less area

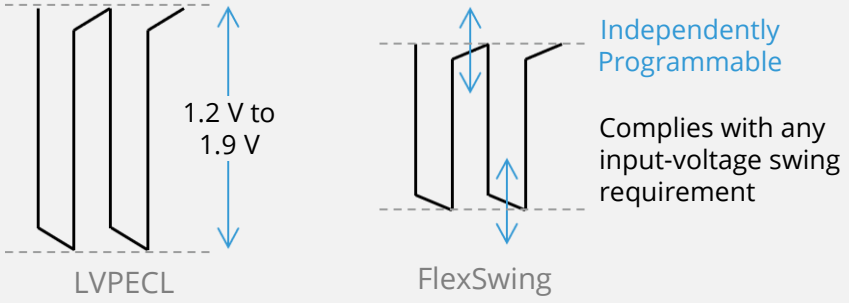


Quartz 2.5 x 2.0 mm, plus LVPECL bias resistors

SiT9501 2.0 x 1.6 mm, integrated LVPECL bias resistors

FlexSwing delivers 30% power savings vs. LVPECL, enables chipset flexibility

Differential-voltage swing diagrams

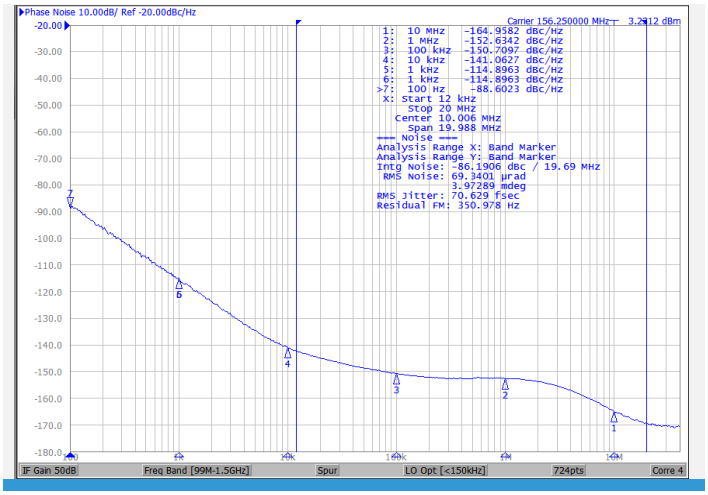


Ultra-low jitter offering down to 70 fsec

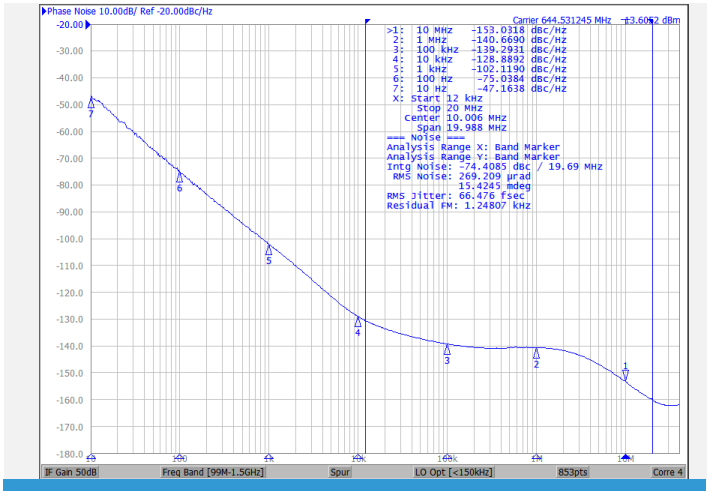
Applications	Devices	Jitter Grade	Function	Key Features
QSFP-DD, QSFP28, OSFP, QSFP	SiT9501	70 fsec	Reference clock for high-speed PHYs	14 standard frequencies, 105°C, 2016/2520/3225 pkgs
	SiT9375	200 fsec		31 standard frequencies, 105°C, 2016/2520/3225 pkgs
	SiT9365/6/7	230 fsec		1 to 725 MHz, 105°C, 3225/5032/7050 pkgs

MEMS Timing Outperforms Quartz

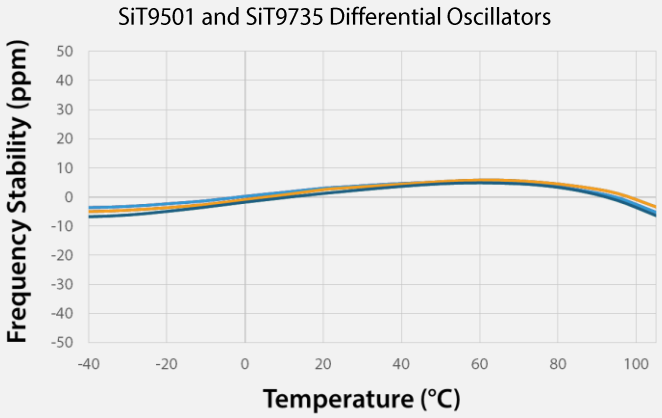
Ultra-Low Phase Noise, 156.25 MHz



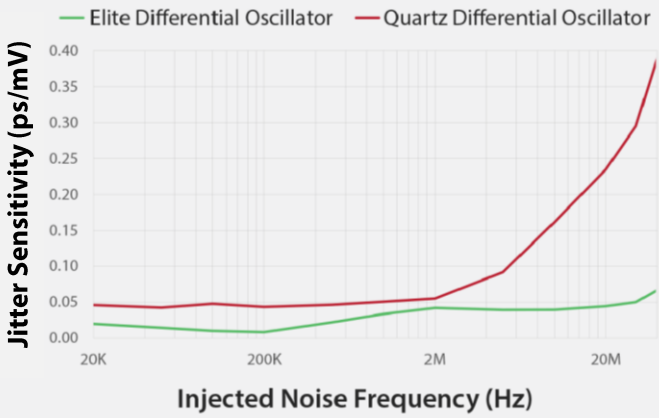
Ultra-Low Phase Noise, 644.53125 MHz



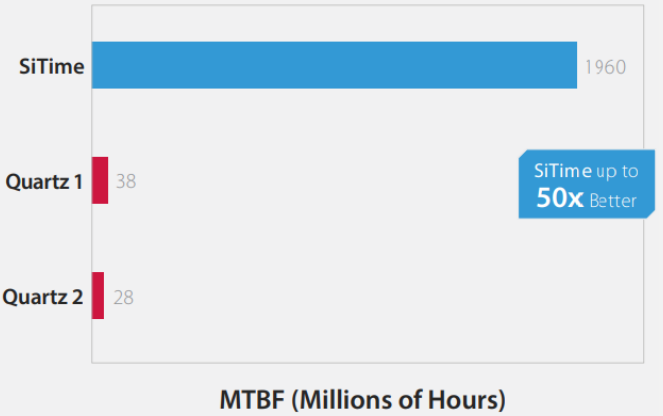
Excellent Stability



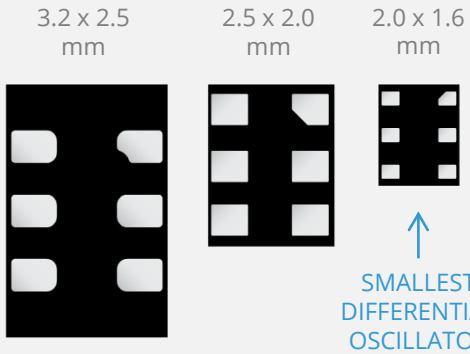
Better PSNR (Power Supply Noise Rejection)



Higher Reliability



Smallest Packages



Learn more about SiTime's Comms-Enterprise timing solutions

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