Adaptive Drift Compensation of Holdover Oscillators

Contents

Introduction

Mobile broadband and telecommunications networks rely on highly stable and accurate timing sources called Stratum clocks to meet the tight phase and synchronization requirements shown in Table 1. In a typical network deployment there is one primary reference clock source (PRS) traceable to a Stratum-1 or a cesium atomic clock. A typical network node timing clock source: Stratum-3 or -3E is derived from a more accurate upstream Stratum-2 clock. The clock at each Stratum level must meet standards-specified frequency stability and long-term aging over 20 years. Stratum-n accuracy and holdover specifications details are described in the following sections.

Table 1: Frequency and phase requirements in LT+/5G networks[1]

Application	Frequency Requirement (Network/Air*)	Phase Requirement
LTE - FDD	16ppb / 50ppb	---
LTE - TDD	16ppb / 50ppb	+/1.5uS
LTE - MBMS	16ppb / 50ppb	+/-1uS
LTE - MBSFN	16ppb / 50ppb	+/500nS
LTE - Advanced	16ppb / 50ppb	+/500nS
OTDOA for e911	---	+/100nS
5G (MIMO & Tx Diversity at each Carrier Frequency)	Not yet ratified	+/-65ns 3GPP TS 36.104 V13.1.0 section 6.5.3.1

Tighter requirements

*Network = Fronthaul/Backhaul, Air = Air interface from Antenna to UE (RF)

Each of the derived Stratum-n clocks, n = 3, 3E uses a local oven controlled oscillator (OCXO) as a back-up clock source in the event of a loss of a higher accuracy upstream Stratum-1 or -2 clock. Typically the duration of the loss of the primary clock reference (PCR) is in the range of 30 minutes to 24 hours. This state of the Stratum-3/3E clock is called the "holdover" mode.

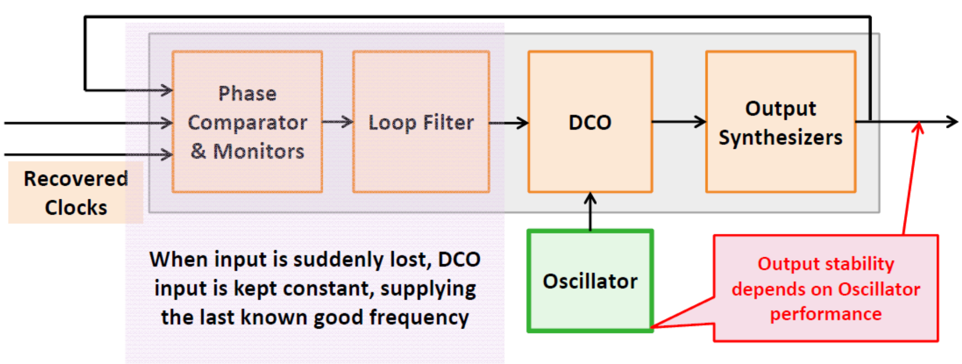

Figure 1: Conceptual block diagram of a clock showing the role of an oscillator in holdover

Since the OCXO must maintain or “hold” the timing synchronization in the event of primary clock loss, it is critical that the OCXO exhibit timing characteristics as good as that of the upstream Startum-2 clock until the link carrying the PCR is restored. The state of the Stratum clock when the OXCO “holds” the last synchronized or syntonized frequency is called the “holdover” state.

Sources of Timing Reference in the Network

All synchronized distributed clocks at each node in the wireless network are traceable to PRTC (primary reference timing clock) or PRC which is traceable to the Stratum-1 clock[2]. The various Stratum level clocks and their relationships are illustrated in Figure 2.

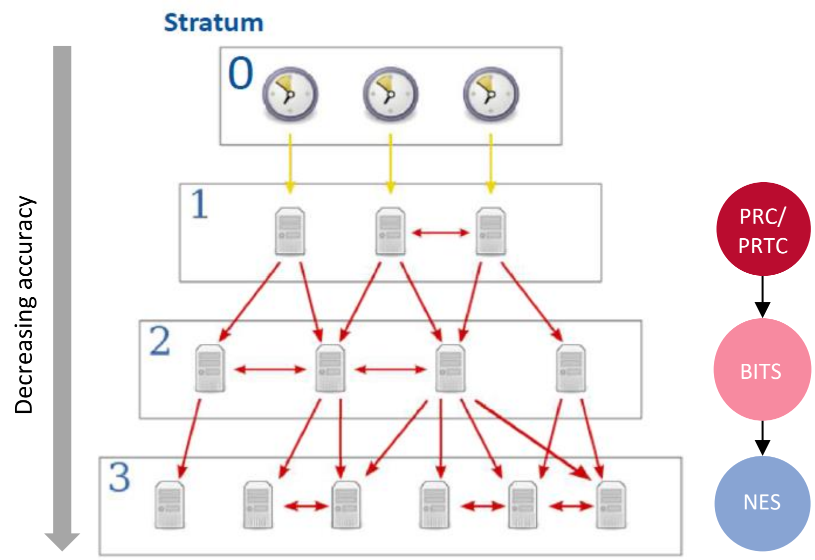

Figure 2: Synchronization hierarchy in telecommunication networks

Stratum 0: A cesium atomic based reference clock source that relays UTC (Coordinated Universal Time) and has little or no delay is known as a stratum-0 device. Stratum-0 servers cannot be used on the network; instead, they are directly connected to computers which then operate as primary time servers.

Stratum 1: The most accurate clock source in the network. Frequency accuracy is ±0.01 ppb to UTC. Also called the primary reference clock (PRC) and is used in gateways of the core network. The PRC is locked to a GPS/GNSS receiver clock which is traceable to a Stratum-0 atomic clock.

Stratum 2: Receive sync signals from the PRC and have good holdover capability. Frequency accuracy is ±16 ppb. Also called the building integrated timing source (BITS) and is used in central offices.

Stratum 3: Receive sync signals from BITS using line timing clock recovery techniques and have reasonable holdover capability. Frequency accuracy is ±4.6 ppm. Also called network element slave clock (NES) and is used in mobile switching centers. There are two variants based on frequency stability: Stratum-3 with a frequency stability of ±300 ppb and Stratum-3E with frequency stability of ±10 ppb.

Holdover Types and Contributing Factors

Holdover oscillators are characterized by two key performance parameters:

1. Frequency Holdover – max frequency deviation during the holdover period. The frequency - deviation is measured from the average frequency prior to entering the holdover state
2. Time Holdover – Time Error (TE) accumulation as referenced to the synchronizing reference (PRC) during the holdover period

The holdover performance is impacted by three contributing factors:

1. Ambient temperature variation
2. Allan variance
3. Aging

As per NIST special publication 1065[3], the time error due to the combined impact of the above contributing factors can be predicted as per the following equation:

$$\Delta T = T_0 + \frac{\Delta f}{f} \cdot t + \frac{1}{2} D \cdot t^2 + \sigma_x(t)$$

The extent of frequency drift due to ambient temperature variation is driven by the frequency vs temperature slope (ΔF/ΔT) of the oscillator. Given the ppt-level ΔF/ΔT values of precision OCXOs and minor variations in temperature (±1°C) during the holdover period, frequency drift contributions due to temperature variations have a benign impact on the overall holdover performance and may be ignored.

Allan variance (AVAR) characterizes the short term frequency stability of the device under constant environmental conditions. AVAR is a statistical metric used to quantify the low frequency noise processes intrinsic to the OCXO. Because this holdover contributing factor is a random entity and is difficult to compensate, it is outside the scope of this paper.

Aging is the long term frequency drift of holdover oscillators under constant environmental conditions and is directly influenced by the structure and construction of the OCXO. This paper discusses techniques to extend the holdover performance of off-the-shelf lower cost TCXOs or OCXOs by adaptively compensating for the long term drift of holdover oscillators.

The following sections focus on the aging profile of leading OCXOs, such as the SiTime SiT5711, and provide guidance on adaptive compensation techniques to extend the aging-related holdover performance of precision OCXOs.

Aging Profile of OCXOs

In order to adaptively compensate for daily drift, it's imperative to understand how the daily drift profile changes with time under different operating conditions. There are several factors that impact the aging profile:

1. Solder reflow shift – this effect is short term and usually takes 24 to 48 hours for the package to de-stress
2. Operating temperature impact – the daily drift is better at lower temperatures
3. Storage impact – the profile is directly related to how long the oscillator is kept in storage or is nonoperational (not powered on) and the temperature at which it was stored
4. Retrace impact – depending on how long the oscillator is powered on and duration it stays powered off, the oscillator will exhibit a different profile for each power on/off cycle

A typical aging profile of OCXOs is shown as a plot of the fractional frequency deviation over 30 days at a constant ambient temperature of 85°C as shown in Figure 3. The plot shows the frequency deviation after offset cancellation from nominal. Also, frequency is measured an hour after the device is powered on to eliminate solder shift related artifacts.

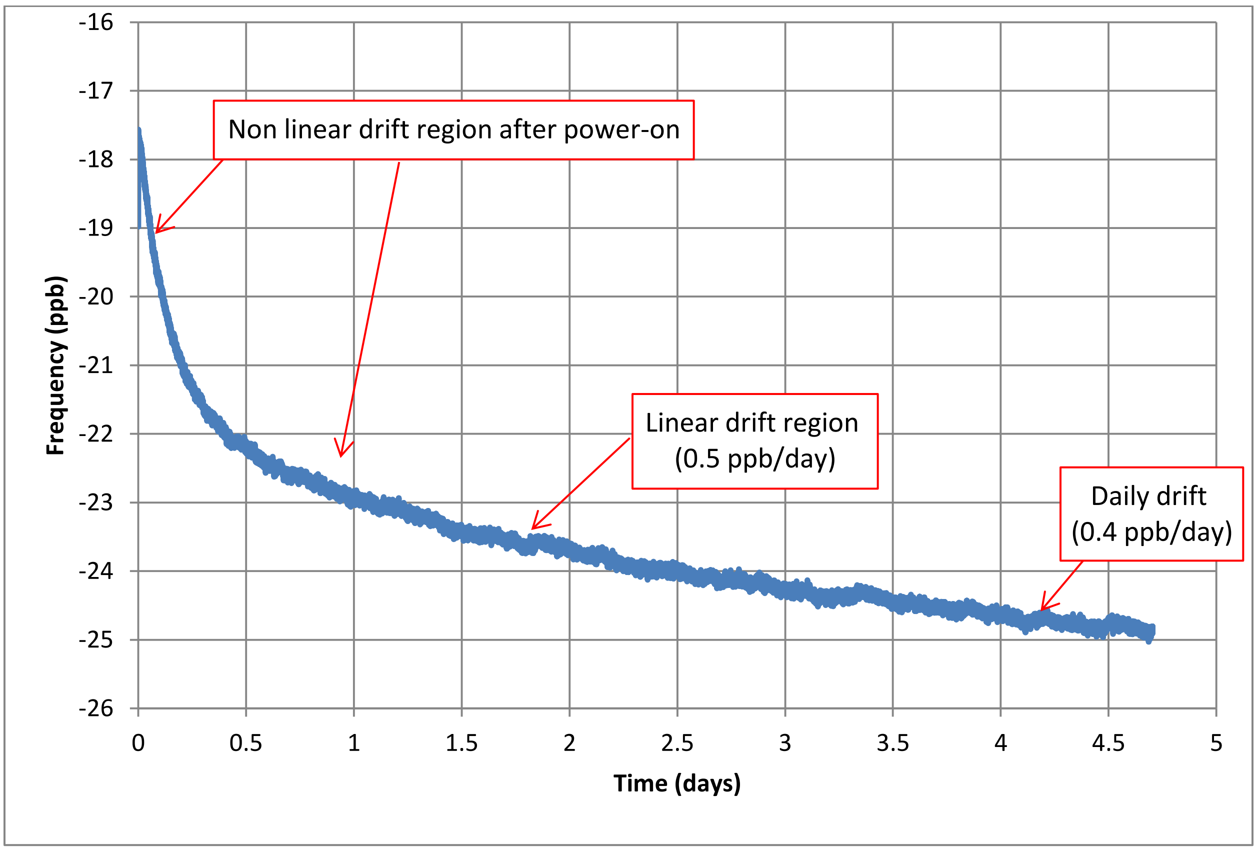

Figure 3: Aging profile showing frequency deviation vs time of a SiTime precision SiT5711 OCXO; Frequency measured an hour after power-on

As the oscillator ages or stays operational longer than few hours, the profile exhibits a linear daily drift trend. Also, as per the plot the daily drift slows down from 2 hours after power on to 5 hours. We will use this aging profile characteristic to apply our adaptive compensation methodology described in the next section.

Adaptive Compensation Methodology

The basic premise of adaptively compensating for the frequency drift is twofold:

1. Make continuous and precise frequency measurements using a system timing reference which is an order of magnitude more accurate than the OCXO. These timing references could be from the GPS/GNSS receiver or PTP time stamp over a SyncE link prior to the system entering holdover state.

2. Model the daily drift as a linear trend such that only the slope can be adaptively predicted after the clock enters the holdover state. This linear model assumption is predicated on the fact that after a few days of operation, most OCXOs exhibit a linear daily drift profile as illustrated in Figure 4.

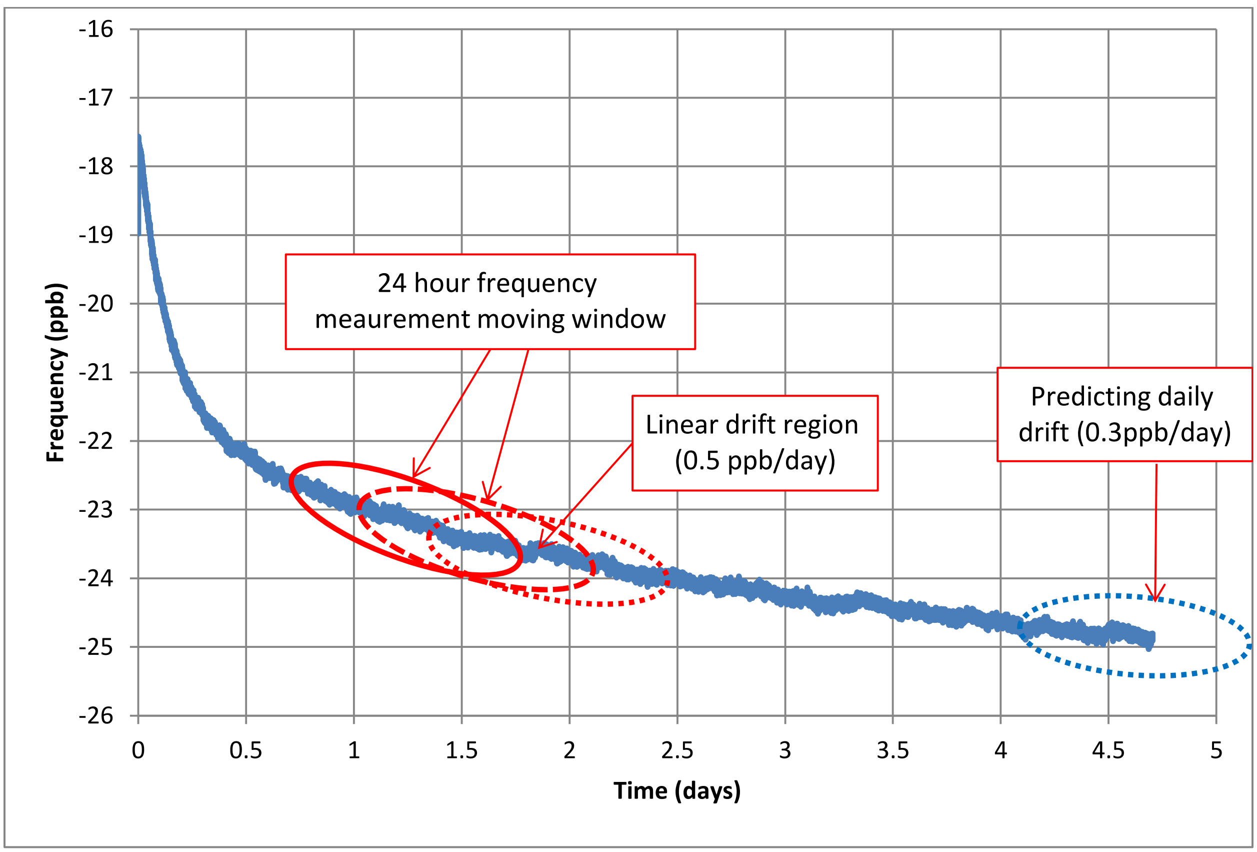

Figure 4: Aging plot of a SiTime precision SiT5711 OCXO showing the application of adaptive compensation to predict the daily rate during holdover at ~5 hours from power-on[4]

The methodology for adaptively compensating for an OCXO boils down to the following steps:

1. Based on continuous and precise measurements, determine the daily aging rate in ppb/day referencing to the nominal frequency.
2. Generate a time vector in seconds with resolution aligning with the frequency data acquired in step 1.
3. During holdover, predict the frequency change due to daily aging multiplying the aging rate form step 1 by the steps in the time vector from step 2.

A mathematical illustration of implementing the above procedure is illustrated in the plots shown in Figure 5.

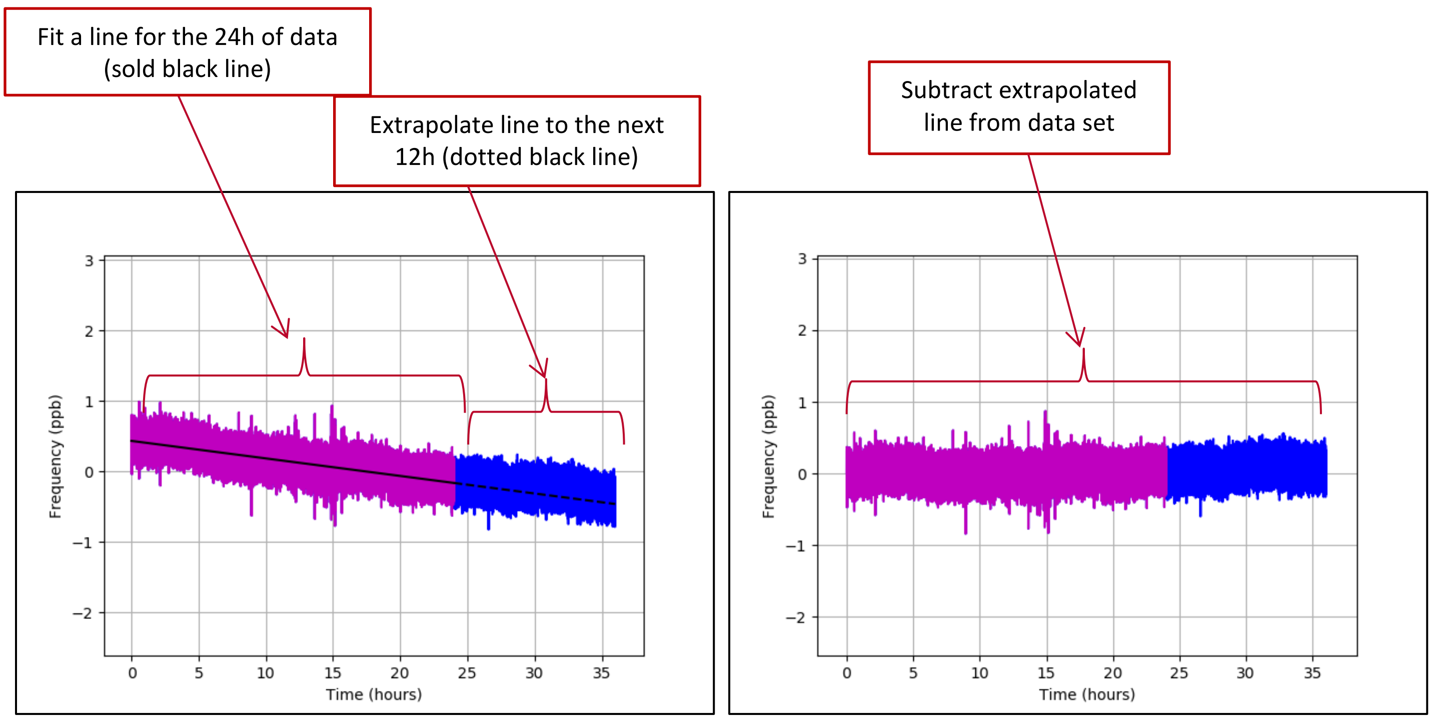

Figure 5: Illustration of aging compensation using a linear model of the daily drift

Conclusion

With the stringent time and frequency synchronization requirements in the next generation of wireless networks, it is critical that network node clock designers apply an adaptive compensation technique to predict the frequency change during holdover state to eliminate or reduce the impact of aging on the time error. The adaptive compensation methodology presented here is predicated on the availability of precision clock references in the systems which are used to make precise fractional frequency deviation measurements and a linear model of the daily aging profile of OCXOs which have been aged for at least a few hours in the system prior to entering holdover mode.

References

1. 5G Network Synchronization, Microlab, Sept 2018
2. GR-1244-CORE, Ericsson, Oct 2009
3. Handbook of Frequency Stability Analysis, NIST SP 1065, July 2008
4. SiT5711 Aging Data, SiTime Internal Characterization Data, June 2019

Table 2: Revision History

Version	Release Date	Change Summary
1.0	06/20/2019	Original doc

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