

Product Reliability Summary — SiT1408/SiT1602/SiT8008 Product Family

Purpose of Stress Testing
This report documents production qualification of the SiT1602 product family. Qualification testing was done on SiT1602 product and by similarity the results of this qualification qualify the SiT1408, SiT1409, SiT1602, SiT1603, SiT1604, SiT5008, SiT8008, SiT8009, SiT9201, SiT2001, and SiT2002 product die for full production release.

Early Life Results (EFR) JEDEC STD-22 A108
Condition: Dynamic, 125°C, Vcc (max), 168 hours
Quantity Stressed: 325 **Quantity Passed:** 325 **Failure Rate:** 0

High Temperature Operating Life (HTOL) JEDEC STD-22 A108
Condition: Dynamic, 125°C, Vcc (max), 1000 hours
Quantity Stressed: 722 **Quantity Passed:** 722 **Quantity Failed:** 0
Semiconductor FIT Calculation: 0.65 FIT^{Note 1}
Confidence Level: 90% **Ea (activation energy in eV):** 0.7 **Derating:** 25°C

Extended Operating Life Test (HTOL) JEDEC STD-22 A108
Condition: Dynamic, 125°C, Vcc (max), 5000 hours
Quantity Stressed: 77 **Quantity Passed:** 77 **Quantity Failed:** 0

ESD
Human Body Model (HBM) JESD22-A114
Condition: one +ve and -ve pulse, all pin combinations **ESD level:** 2000 V
Quantity Stressed: 3 **Quantity Passed:** 3 **Failure Rate:** 0
Machine Model (MM) JEDEC STD-EIA/JESD-22 A115
Condition: one +ve and -ve pulse, all pin combinations **ESD level:** 200 V
Quantity Stressed: 3 **Quantity Passed:** 3 **Failure Rate:** 0
Charged Device Model (CDM) JEDC STD-JESD-22 C101
Condition: one +ve and -ve pulse, all pins **ESD level:** 750 V
Quantity Stressed: 3 **Quantity Passed:** 3 **Failure Rate:** 0

Latch Up JEDEC STD-JESD78
Condition: 100 mA @ 125°C, Vcc (max) and voltage overstress
Quantity Stressed: 6 **Quantity Passed:** 6 **Failure Rate:** 0

NVM Data Retention <small>Note 2</small>			
Condition:	NVM High Temp Storage (NVM HTS), 150°C, 1000 hours		
Quantity Stressed:	93	Quantity Passed:	93
		Quantity Failed:	0
Programing:	Checkerboard pattern, Specific Custom Pattern		
Condition:	NVM Operating Life (NVM HTOL), Dynamic, 125°C, Vcc (max), 1000 hours		
Quantity Stressed:	95	Quantity Passed:	95
		Quantity Failed:	0
Programing:	Checkerboard pattern		

Mechanical Shock (MS) MIL-STD-883 Method 2002			
Condition:	Peak acceleration 10 kg		
Quantity Stressed:	39	Quantity Passed:	39
		Failure Rate:	0

Variable Frequency Vibration (VfV) MIL-STD-883 Method 2007			
Condition:	Peak acceleration 70 g		
Quantity Stressed:	39	Quantity Passed:	39
		Failure Rate:	0

Vibration Fatigue (VF) MIL-STD-883 Method 2005 <small>Note 3</small>			
Condition:	Peak acceleration 20 g, 30 hours		
Quantity Stressed:	39	Quantity Passed:	39
		Failure Rate:	0

Constant Acceleration (CA) MIL-STD-883 Method 2001			
Condition:	Y1 plane, 30 kg		
Quantity Stressed:	39	Quantity Passed:	39
		Failure Rate:	0

Product Information					
Wafer Fabrication					
Factory:	CMOS:	TSMC, Taiwan	Process:	1P5M CMOS-8"	Design Rule: 0.18 um
Factory:	MEMS:	BOSCH, Germany	Process :	PFD1_A	Design Rule: 0.25 um
Notes:					
<ol style="list-style-type: none"> 1. The oscillator family failure rate of 0.65 FIT, calculated based on large HTOL sample size, applies due to process technology and design rule similarity. 2. NVM data retention testing was done on SiT8208 product as test vehicle; however, because of structural and process similarities between SiT8208 and SiT14xx/SiT16xx/SiT8008/SiT89xx/SiT200x base products, data sharing is used. 3. Data share with SiT8208 product is done because of structural and process similarity between SiT8208 and SiT14xx/SiT16xx/SiT8008/SiT89xx/SiT200x base products. 					

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