Precision Timing Solutions

For FPGA Designers

Precision Timing for FPGAs

FPGAs have progressed well beyond the original core fabric composed of logic and flops, surrounded by general-purposed I/O. The fabric has been upgraded with embedded memory, DSP blocks, AI processors, all connected by a network on chip. In addition to an upgraded fabric, FPGAs now feature multi-core processors.

The I/O ring has also been upgraded with a range of hard IP blocks and high-speed SerDes to support several interfaces such as Gigabit Ethernet, PCIe, DRR memory, etc. Today's modern FPGA has become a programmable SoC with complex clocking requirements.

Key Considerations

- Number and frequency of clocks
- Range of clocking solutions
- Accuracy and robustness
- Board space

FPGAs Represent a Complex Clocking Environment

As the functionality of FPGAs has increased, the complexity of clocking needs has grown. As a result, FPGA vendors have added several built-in PLLs and clock management functions. This increase in functionality is mirrored by an increase in needed clock sources:

- Multiple reference clocks for the embedded PLLs
- Per I/O bank reference clocks
- Clocks for user logic
- Various supporting clock sources for features such as real-time clocks, configuration controllers, etc.

For SRAM-based FPGAs, additional external logic may be required to control the configuration. Often a small CPU plus flash memory is used, requiring its own clock source.

These FPGAs and the supporting configuration logic do not exist on a board in isolation. For example, higher-end CPUs can be found in conjunction to the FPGA, with the FPGA acting as a hardware accelerator to the CPU. Often other devices such as transceivers, DRAM, and other ASSPs can be found on the board. All these devices have their own clocking requirements, collectively creating a complex clocking environment. Designers need a supplier who can deliver a range of clocking solutions from oscillators to clock management devices.

FPGAs are Ubiquitous

FPGAs are a niche product used everywhere, from set top boxes to GPS-guided munitions, from the ocean floor to space — anywhere a custom solution is needed. But a custom ASIC would be cost prohibitive (from an NRE perspective), or not be able to meet time-to-market needs. Consequently, FPGA designers need a supplier whose product line supports a range of environments from the benign conditions of an office, to harsh environments with wide temperature ranges, high vibration and pressure.

Why SiTime Timing Solutions

More robust in harsh environments
- 4x better vibration resistance — 0.1 ppb/g typical
- 20x better shock survivability

Better stability over a wide temperature range
- Up to -55 to +125°C operation
- Airflow and thermal shock resistant — 1 ppb/°C

High reliability
- Up to 50x better quality and reliability
- Lifetime warranty

Programmability for flexible design
- Any frequency, any stability, any voltage within a wide range
- Qualify once for multiple parts

Unique features
- EMI reduction — Up to 30 dB lower
- Low power for longer battery life — 4.5 µA at 100 kHz
- Smaller size — 1.5 mm x 0.8 mm packages

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Featured products – please refer to SiTime.com or contact us for more options.

Type	Product	Frequency	Key Features	Key Values
Clock Generator	SiT95141 SiT95143	1 to 220 MHz	• up to 4 inputs, 11 outputs • Up to 2 GHz clock output frequencies • 120 fs(1) integrated phase jitter • Programmable PLL loop bandwidth, 1 mHz to 4 kHz • Digital frequency control • -40°C to 85°C • 9.0 x 9.0 mm package	• Multiple clock domains, multiple clock outputs enables complex clock architectures • 10x more resistant to vibration and board bending
Jitter Attenuator	SiT95145			
Network Synchronizer	SiT95147 SiT95148			
Differential Oscillator	SiT9375	25 to 644.5 MHz 70 fs IPJ[1]	• ±20 ppm to ±50 ppm frequency stability • LVPECL, LVDS, HCSL • 1.8 V to 3.3 V • -40°C to 105°C • 2.0 x 1.6 mm, 2.5 x 2.0 mm, 3.2 x 2.5 mm packages	• Meets demanding jitter requirements • Small PCB footprint, easier layout • Easy design due to flexibility • Better MEMS reliability
	SiT9501	25 to 644.5 MHz 150 fs IPJ[1]		
Super-TCXO	SiT5501[2]	1 to 60 MHz	• ±10 ppb stability • ±0.5 ppb/°C • 2E-11 ADEV • -40°C to 105°C • 7.0 x 5.0 mm package	• Ensures QoS requirements are met in telecom equipment used in hostile environments

[1] Integrated Phase Jitter, 12 kHz to 20 MHz integration range

[2] Please contact SiTime for higher frequencies.

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