

Precision Timing for FPGAs

FPGAs have evolved well beyond their original logic and flip-flop-based fabric with general-purpose I/O. Modern FPGAs integrate embedded memory, DSP blocks, AI processors, and a network-on-chip for high-speed interconnectivity. Many also feature multi-core processors, often optimized for AI/ML workloads.

The I/O ring has also advanced, incorporating hard IP blocks and high-speed SerDes to support interfaces such as Gigabit Ethernet, PCIe, and DDR memory. These additions enable increasingly complex clocking requirements in modern FPGAs.

Key Considerations

- Clock count and frequency
- Available clocking solutions
- Accuracy and robustness
- Board space constraints

FPGAs Represent a Complex Clocking Environment

Expanding FPGA functionality has introduced more complex clocking requirements. To address these demands, FPGA vendors integrate multiple PLLs and clock management features, driving demand for diverse clock sources, including:

- Reference clocks for SerDes transceivers with stringent phase noise requirements
- Timekeeping and timestamping for RTCs, IEEE 1588, and GNSS-based applications
- Multiple reference clocks for embedded PLLs
- Per I/O bank reference clocks
- Clocks for user logic
- Supporting clock sources for configuration controllers, low-speed interfaces, and other system functions

SRAM-based FPGAs often require external logic for configuration, typically using a small CPU and flash memory, each with its own clock source.

FPGAs and their configuration logic operate alongside high-performance CPUs, FPGA-based accelerators, transceivers, DRAM, and other ASSPs—each with distinct clocking needs. This creates a complex timing environment, requiring a supplier that provides a full range of clocking solutions, from oscillators to advanced clock management devices.

FPGAs are Ubiquitous

FPGAs are used in diverse applications, from set-top boxes and GPS-guided munitions to the ocean floor and space. They provide customizable solutions where integrating a custom ASIC is impractical due to high NRE costs or tight time-to-market constraints. To ensure safe, reliable operation, FPGA designers rely on suppliers with product lines that support a broad environmental spectrum—from stable enterprise conditions to deployments exposed to wide temperature variations, high vibration, and intense pressure.

Why SiTime Timing Solutions

Superior performance in harsh environments

- 4x greater vibration resistance (0.1 ppb/g typical)
- 20x higher shock survivability

Enhanced stability across a wide temperature range

- Operational from -55 to +125°C
- Resistant to airflow and thermal shock (1 ppb/°C)

Exceptional reliability

- Up to 50x better quality and reliability
- Lifetime warranty

Programmability for flexible design

- Broad configurability — Any frequency, stability, or voltage within a wide range
- Simplified qualification — Qualify once for multiple parts

Unique features

- EMI reduction — Up to 30 dB lower
- Low power consumption — 4.5 μ A at 100 kHz for extended battery life
- Compact footprint — 1.5 mm x 0.8 mm packages

Clocking Decision Tree for FPGA-Based Devices

Designers must follow a logical process with selected clocking devices to support these advanced programmable SoCs.

Design Requirement	SiTime Solution
Environmental	
What is the temperature range of the target application?	SiTime oscillators are available in a variety of temperature ranges, including –55°C to +125°C.
Does the application require high vibration tolerance?	All SiTime products withstand high levels of shock and vibration. Endura™ products are screened for extreme environmental conditions.
Timekeeping	
Do embedded processors require an RTC?	SiTime offers a range of 32 kHz XO and TCXO products based on required timekeeping accuracy.
Does the application require timestamping or clock synchronization (e.g., GNSS, IEEE 1588)?	SiTime offers programmable MHz XOs, TCXOs, and OCXOs, ideal for applications needing precise timestamping or long-term hold-over without a reference clock.
High-Speed Communication	
What standards are required?	SiTime offers clocking solutions for high-speed SerDes applications. Contact SiTime support for help selecting the right device to meet reference frequency and phase noise requirements.
How many transceivers are required, and what types?	
What reference clock(s) and phase noise requirements apply?	
Application Logic Clocking	
What clocks are needed for external memory and lower-speed interfaces?	Application clock stability and jitter requirements vary widely. SiTime offers the industry's broadest portfolio of XOs, TCXOs, OCXOs, and clock generators to meet diverse needs. The SiT8008 programmable MHz XO is a widely used solution, with additional options available for specialized applications.
What clocking requirements apply to application logic?	
System and Support Clocks	
What clocks are required for device configuration?	SiTime offers system and support clocks designed to meet specific frequency and performance requirements. The SiT8008 is a good starting point, with additional options available— contact SiTime for expert guidance.

Featured products – please refer to [SiTime.com](https://www.sitime.com) or [contact us](#) for more options.

Type	Product	Frequency	Key Features	Key Values
Clock Generator	SiT95141 SiT91211 SiT91213	1 to 220 MHz	<ul style="list-style-type: none"> Up to 4 inputs, 11 outputs Up to 2 GHz clock output frequencies Integrated phase jitter as good as 70 fs (typ.) Programmable PLL loop bandwidth, 1 mHz to 4 kHz Digital frequency control -40°C to 85°C 4 x 4 mm, 9.0 x 9.0 mm packages 	<ul style="list-style-type: none"> Highest level of clock tree integration with integrated MEMS resonator, eliminating the need for quartz crystal reference required by traditional clocks Multiple clock domains, multiple clock outputs enables complex clock architectures 10x more resistant to vibration and board bending
Jitter Attenuator	SiT95145			
Network Synchronizer	SiT95147 SiT95148			
Differential Oscillator	SiT9375	25 to 644.5 MHz 70 fs IPJ ^[1]	<ul style="list-style-type: none"> ±20 ppm to ±50 ppm frequency stability LVPECL, LVDS, HCSL 1.8 V to 3.3 V -40°C to 105°C 2.0 x 1.6 mm, 2.5 x 2.0 mm, 3.2 x 2.5 mm packages 	<ul style="list-style-type: none"> Meets demanding jitter requirements Small PCB footprint, easier layout Easy design due to flexibility Better MEMS reliability
	SiT9501	25 to 644.5 MHz 150 fs IPJ ^[1]		
Super-TCXO	SiT5501 ^[2] SiT5503	1 to 60 MHz	<ul style="list-style-type: none"> ±5, ±10 ppb stability ±0.3, ±0.5 ppb/°C frequency slope 1.5e-11 ADEV, 2e-11 ADEV Up to -40°C to 105°C 7.0 x 5.0 mm package 	<ul style="list-style-type: none"> Ensures QoS requirements are met in telecom equipment used in hostile environments
Single-Ended Oscillators	SiT8008 SiT8009	1 to 137 MHz	<ul style="list-style-type: none"> 1.3 ps RMS phase jitter Field Programmable 	<ul style="list-style-type: none"> Enables higher reliability and tighter frequency stability over quartz

¹ Integrated Phase Jitter, 12 kHz to 20 MHz integration range ² Please [contact SiTime](#) for higher frequencies.



[Learn more](#) about timing solutions from SiTime



[SiTimeDirect Store](#)



[Contact Us](#)



[sitime.com](https://www.sitime.com)