

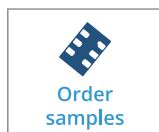
Description

The SiT9397 is an AEC-Q100 qualified, ultra-low jitter differential oscillator engineered for automotive applications. It delivers the most stable timing under environmental stressors such as shock, vibration, high heat, rapid thermal transients and power supply noise.

The SiT9397 can be factory programmed for specific combinations of frequency, stability, output signaling, voltage, and output enable functionality. Programmability enables automotive system designers to qualify the device once and use it for different applications. It also eliminates the long lead times and customization costs associated with quartz devices where each combination is custom built.

In addition to standard differential signal types, this device comes with a unique FlexSwing™ output-driver that performs like LVPECL but provides independent control of voltage swing and DC offset. It is designed to interface with chipsets having non-standard input voltage requirements and eliminate all external source-bias resistors. It also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for an external dedicated LDO.

Refer to [Manufacturing Notes](#) for proper reflow profile, tape and reel dimension, and other manufacturing related information.



Features

- Wide frequency range between 220 MHz and 920 MHz accurate to 6 decimal places
(For additional frequencies, refer to SiT9396 datasheet)
- 150 fs RMS typical phase jitter, 12 kHz to 20 MHz
- 12 fs/mV power supply induced jitter sensitivity with filter
- AEC-Q100 Grade 1 temperature range (-40°C to 125°C)
Grade 2 and 3 also available
- LVPECL, LVDS, HCSL, Low-power HCSL, and FlexSwing signaling options
- ±25, ±30 and ±50 ppm frequency stabilities
[Contact SiTime](#) for ±20 ppm
- Factory programmable options for low lead time
- 1.8 V, 2.5 V, 3.3 V, and wide continuous power supply voltage range options
- 2 x 1.6, 2.5 x 2, 3.2 x 2.5 mm x mm packages

Applications

- ADAS computer, ECU
- Collision detection devices
- In-vehicle 10/40/100 Gbps Ethernet
- Infotainment systems
- Lidar
- Radar

Related products for [automotive applications](#).

For aerospace and defense applications SiTime recommends using only [Endura™ SiT9357](#).

Block Diagram

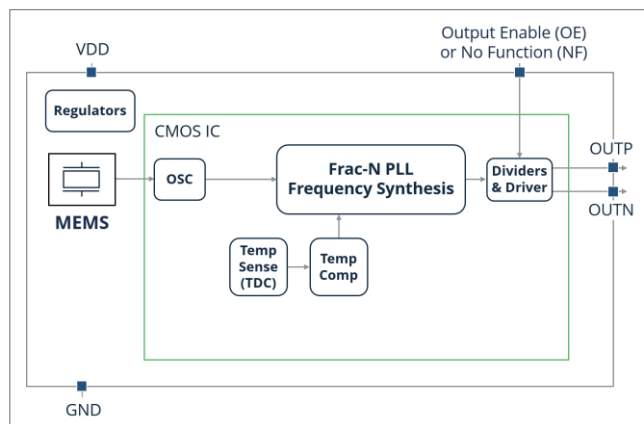


Figure 1. SiT9397 Block Diagram

Package Pinout

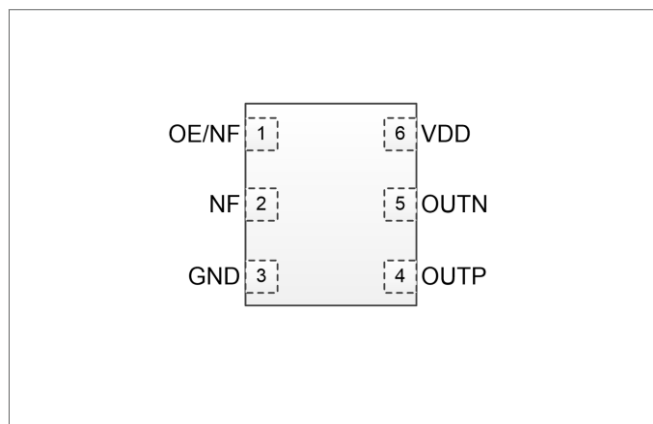
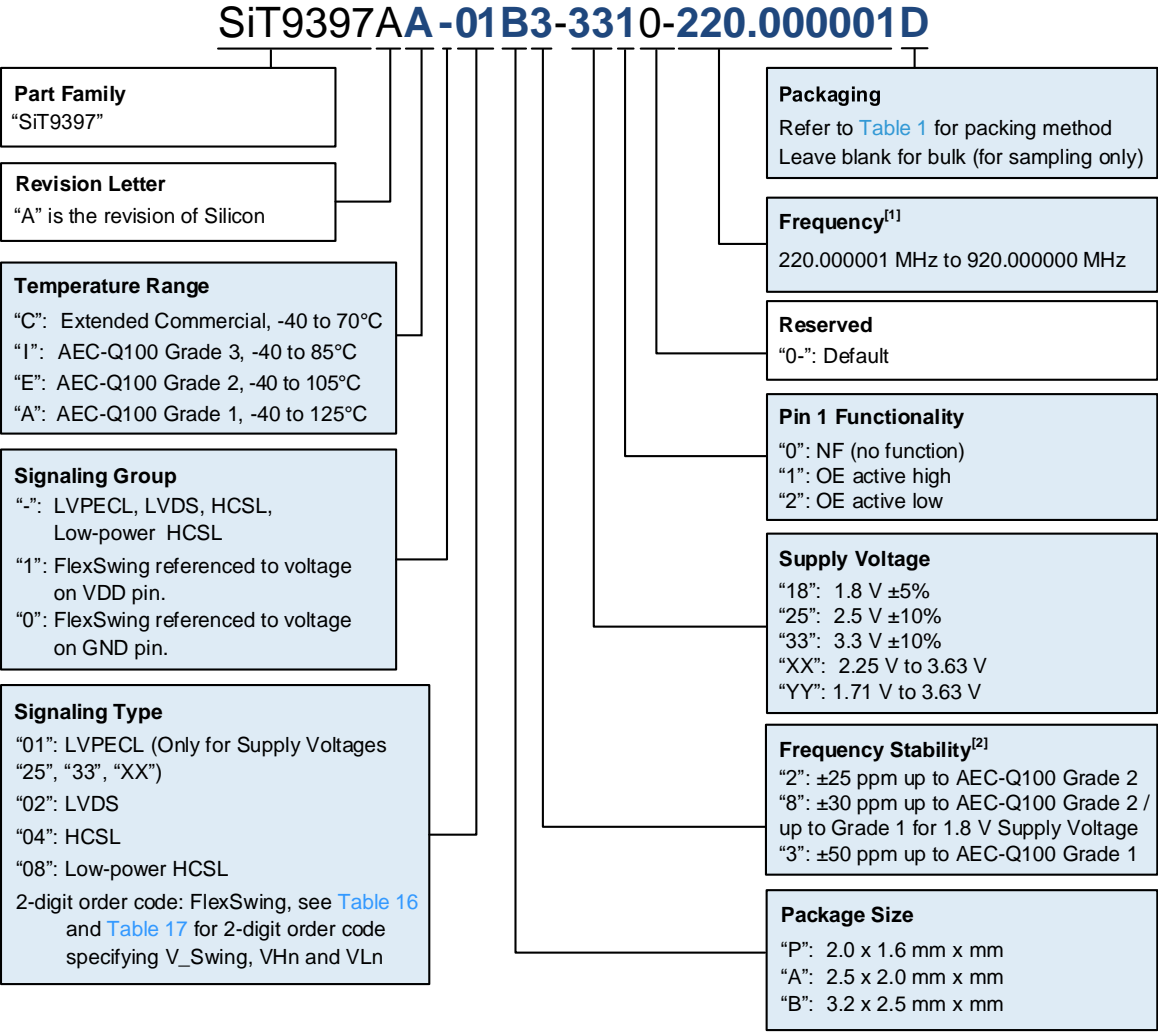


Figure 2. Pin Assignments (Top view)
(Refer to [Table 15](#) for Pin Descriptions)

Ordering Information



- Notes:**
1. Frequencies between 678.000000 MHz and 781.000000 MHz are currently not supported. HCSL Signaling up to 500MHz only. [Contact SiTime](#) for more options.
 2. [Contact SiTime](#) for ±20 ppm, and ±30 ppm over -40 to 125°C at Supply Voltage Options other than 1.8 V.

Table 1. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	8 mm T&R (250u)
2.0 x 1.6	D	E	G
2.5 x 2.0	D	E	G
3.2 x 2.5	D	E	G

Table of Contents

Description 1

Features 1

Applications 1

Block Diagram 1

Package Pinout 1

Ordering Information 2

Electrical Characteristics 4

Pin Description 14

FlexSwing Configurations 15

Test Circuit Diagrams 17

 Test Setups for LVPECL Measurements 17

 Test Setups for FlexSwing Measurements^[15] 18

 Test Setups for LVDS Measurements 19

 Test Setups for HCSL Measurements 20

 Test Setups for Low-Power HCSL Measurements 21

Waveform Diagrams 22

Termination Diagrams 25

 LVPECL and FlexSwing Termination 25

 LVDS, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V 26

 HCSL, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V 26

 Low-power HCSL, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V 26

Dimensions and Patterns — 2.0 x 1.6 mm x mm 27

Dimensions and Patterns — 2.5 x 2.0 mm x mm 28

Dimensions and Patterns — 3.2 x 2.5 mm x mm 29

Additional Information 30

Revision History 30

Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over operating temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage. See [Test Circuit Diagrams](#) for the test setups used with each signaling type.

Table 2. Electrical Characteristics – Common to All Output Signaling Types

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	220.000001	–	920.000000	MHz	Accurate to 6 decimal places. Frequencies between 678.000000 MHz and 781.000000 MHz are currently not supported. Contact SiTime for more options.
Frequency Stability						
Frequency Stability	F_stab	–	–	±25	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 2 pF ± 10%, and 10 years aging at 85°C. See Ordering Information for available frequency stability across different operating temperature ranges. Contact SiTime for ±20 ppm.
		–	–	±30	ppm	
		–	–	±50	ppm	
10 Year Aging	F_10y	–	±0.7	2.3	ppm	Ambient temperature of 85°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended commercial, ambient temperature
		-40	–	+85	°C	AEC-Q100 Grade 3
		-40	–	+105	°C	AEC-Q100 Grade 2
		-40	–	+125	°C	AEC-Q100 Grade 1
Supply Voltage						
Supply Voltage	Vdd	1.71	–	3.63	V	Voltage-supply order code “YY”
		2.25	–	3.63	V	Voltage-supply order code “XX”
		1.71	1.80	1.89	V	Voltage-supply order code “18”. Contact SiTime for 1.5 V
		2.25	2.50	2.75	V	Voltage-supply order code “25”
		2.97	3.30	3.63	V	Voltage-supply order code “33”
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Logic High function for Pin 1
Input Voltage Low	VIL	–	–	30%	Vdd	Logic High function for Pin 1
Input Pull-up/Pull-down Impedance	Z_in	–	120	–	kΩ	Pin 1 for OE function
Output Characteristics						
Duty Cycle	DC	45	–	55	%	See Figure 15 for waveform.
Startup, OE and SE Timing						
Startup Time	T_start	–	1.2	2	ms	Measured from the time Vdd reaches its rated minimum value
Output Enable Time 1	T_oe	–	–	100+3 clock cycles	ns	For all signaling types except Low-Power HCSL. Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of final swing. See Figure 21 for waveform.
Output Enable Time 2	T_oe	–	–	500+3 clock cycles	ns	For Low-Power HCSL signaling type. Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of final swing. See Figure 21 for waveform.
Output Disable Time	T_od	–	–	100+3 clock cycles	ns	Measured from the time OE pin toggles to disable logic level to the last clock edge. See Figure 22 for waveform.
Jitter and Phase Noise, measured at f = 622.08 MHz						
RMS Phase Jitter (random)	T_phj	–	150	200	fs	12 kHz to 20 MHz offset frequency integration bandwidth. Contact SiTime for <100 fs rms jitter
Spurious Phase Noise	PN_spur	–	-88	–	dBc	12 kHz to 20 MHz offset frequency range
RMS Period Jitter ^[3]	T_jitt_per	–	0.62	0.72	ps	Measured based on 10K cycles
Peak Cycle-to-cycle Jitter ^[3]	T_jitt_cc	–	3.5	4.4	ps	Measured based on 1K cycles

Note:

3. Measured according to JESD65B using Keysight DSAX91604A Oscilloscope.

Table 3. Electrical Characteristics – LVPECL | Supply voltage (“order code”): 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”). All typical specifications are measured at nominal supply voltage of 2.5 V and nominal frequency of 622.08 MHz unless otherwise stated. See [Figure 4](#) and [Figure 5](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	46	56.5	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination 1	Idd_oe_wt1	–	58	72	mA	Including load termination current as shown in Figure 27 for Vdd=3.3 V $\pm 10\%$, Vdd=2.25 V to 3.63 V and R3=50 Ohms.
		–	58	66.5	mA	Including load termination current as shown in Figure 27 for Vdd=2.5 V $\pm 10\%$ and R3=50 Ohms.
Current Consumption, Output Enabled with Termination 2	Idd_oe_wt2	–	71	76.5	mA	Including load termination current. See Figure 28 for termination.
Current Consumption Output Disabled with Termination 1	Idd_od_wt1	–	59	74.5	mA	Including load termination current as shown in Figure 27 for Vdd=3.3 V $\pm 10\%$, Vdd=2.25 V to 3.63 V and R3=50 Ohms. Driver output is at logic-high voltage levels.
		–	59	67.5	mA	Including load termination current as shown in Figure 27 for Vdd=2.5 V $\pm 10\%$ and R3=50 Ohms. Driver output is at logic-high voltage levels.
Current Consumption, Output Disabled with Termination 2	Idd_od_wt2	–	74	80.5	mA	Including load termination current. See Figure 28 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	Vdd-1.15	Vdd-0.95	Vdd-0.77	V	See Figure 14 for waveform.
Output Low Voltage	VOL	Vdd-1.92	Vdd-1.7	Vdd-1.57	V	See Figure 14 for waveform.
Output Differential Voltage Swing	V_Swing	1.35	1.5	1.7	V	See Figure 15 for waveform.
Rise/Fall Time	Tr, Tf	–	120	170	ps	20% to 80%. See Figure 15 for waveform.
Differential Asymmetry, peak-peak	V_da	–	65	–	mV	See Figure 17 for waveform.
Differential Skew, peak	V_ds	–	± 30	–	ps	See Figure 18 for waveform.
Overshoot Voltage, peak	V_ov	–	8	–	%	Measured as percent of V_Swing. See Figure 19 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	13	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	4.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 4 .
Power Supply-Induced Phase Noise	PSPN	–	-64	–	dBc	50 mV peak-peak ripple on VDD.
		–	-73.5	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 4 .

Table 4. Electrical Characteristics – FlexSwing | Supply voltage (“order code”) referred to VDD, only: 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”). All typical specifications are measured at nominal frequency of 622.08 MHz unless otherwise stated. See [Figure 6](#) and [Figure 7](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	49.5	62.5	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	58.5	74	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 27 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V, and R3=100 Ohms.
		–	58.5	66.5	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 27 for Vdd=2.5 V ±10%, and R3=100 Ohms.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	57	73	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 27 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V, and R3=100 Ohms. Driver output is at logic-high voltage levels.
		–	57	66	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 27 for Vdd=2.5 V ±10%, and R3=100 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn -0.25	VHn	VHn +0.19	V	See Figure 14 for waveform; Refer to Table 16 or Table 17 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn -0.24	VLn	VLn +0.19	V	See Figure 14 for waveform; Refer to Table 16 or Table 17 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	-22%	2*(VHn-VLn)	+22%	V	See Figure 15 for waveform.
Rise/Fall Time	Tr, Tf	–	115	179	ps	20% to 80%. See Figure 15 for waveform.
Differential Asymmetry, peak-peak	V_da	–	55	–	mV	See Figure 17 for waveform.
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 18 for waveform.
Overshoot Voltage, peak	V_ov	–	8	–	%	Measured as percent of V_Swing. See Figure 19 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	17	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code “ER”.
		–	4.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code “ER”. Using RC power supply filter as shown in Figure 6 .
Power Supply-Induced Phase Noise	PSPN	–	-61.5	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code “ER”.
		–	-69	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code “ER”. Using RC power supply filter as shown in Figure 6 .

Table 5. Electrical Characteristics – FlexSwing | Supply voltage (“order code”) referred to GND, only: 1.8 V $\pm 5\%$ (“18”), 1.71 V to 3.63 V (“YY”). All typical specifications are measured at nominal frequency of 622.08 MHz unless otherwise stated. See [Figure 6](#) and [Figure 7](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	46.5	54	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	56	62	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 27 for Vdd=1.8 V ±5% and R3=100 Ohms.
		–	56	64	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 27 for Vdd=1.71 V to 3.63 V and R3=100 Ohms.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	56	61.5	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 27 for Vdd=1.8 V ±5% and R3=100 Ohms. Driver output is at logic-high voltage levels.
		–	56	63.5	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 27 for Vdd=1.71 V to 3.63 V and R3=100 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn – 0.13	VHn	VHn + 0.12	V	See Figure 14 for waveform; Refer to Table 16 or Table 17 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn – 0.13	VLn	VLn + 0.12	V	See Figure 14 for waveform; Refer to Table 16 or Table 17 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	-22%	2*(VHn-VLn)	+22%	V	See Figure 15 for waveform.
Rise/Fall Time	Tr, Tf	–	120	180	ps	20% to 80%. See Figure 15 for waveform.
Differential Asymmetry, peak-peak	V_da	–	60	–	mV	See Figure 17 for waveform.
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 18 for waveform.
Overshoot Voltage, peak	V_ov	–	8	–	%	Measured as percent of V_Swing. See Figure 19 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	15	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code “3E”.
		–	3	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code “3E”. Using RC power supply filter as shown in Figure 6 .
Power Supply-Induced Phase Noise	PSPN	–	-62.5	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code “3E”.
		–	-76.5	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code “3E”. Using RC power supply filter as shown in Figure 6 .

Table 6. Electrical Characteristics – FlexSwing | Supply voltage (“order code”) referred to GND, only: 2.5 V \pm 10% (“25”), 3.3 V \pm 10% (“33”), 2.25 V to 3.63 V (“XX”). All typical specifications are measured at nominal frequency of 622.08 MHz unless otherwise stated. See [Figure 6](#) and [Figure 7](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	47.5	54	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	57	63.5	mA	Including load termination current, for FlexSwing order code “VP”. See Figure 27 for Vdd=3.3 V \pm 10%, Vdd=2.25 V to 3.63 V, and R3=100 Ohms.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	57.5	66	mA	Including load termination current, for FlexSwing order code “VP”. See Figure 27 for Vdd=3.3 V \pm 10%, Vdd=2.25 V to 3.63 V, and R3=100 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.15	VHn	VHn + 0.1	V	See Figure 14 for waveform; Refer to Table 16 or Table 17 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn - 0.16	VLn	VLn + 0.1	V	See Figure 14 for waveform; Refer to Table 16 or Table 17 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	-21%	2*(VHn-VLn)	+21%	V	See Figure 15 for waveform.
Rise/Fall Time	Tr, Tf	–	120	170	ps	20% to 80%. See Figure 15 for waveform.
Differential Asymmetry, peak-peak	V_da	–	60	–	mV	See Figure 17 for waveform.
Differential Skew, peak	V_ds	–	\pm 40	–	ps	See Figure 18 for waveform.
Overshoot Voltage, peak	V_ov	–	8	–	%	Measured as percent of V_Swing. See Figure 19 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	17	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code “VP”
		–	3.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code “VP”. Using RC power supply filter as shown in Figure 6 .
Power Supply-Induced Phase Noise	PSPN	–	-61.5	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code “VP”.
		–	-73	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code “VP”. Using RC power supply filter as shown in Figure 6 .

Table 7. Electrical Characteristics – LVDS | Supply voltage (“order code”): 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”). All typical specifications are measured at nominal supply of 2.5 V and nominal frequency of 622.08 MHz unless otherwise stated. See [Figure 8](#) and [Figure 9](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	40.5	48	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	44.5	51.5	mA	Including load termination current. See Figure 31 for termination.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	46	52	mA	Including load termination current. See Figure 31 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Differential Output Voltage	VOD	250	345	450	mV	See Figure 16 for waveform.
Delta VOD	ΔVOD	–	–	50	mV	See Figure 16 for waveform.
Offset Voltage	VOS	1.125	1.25	1.375	V	See Figure 16 for waveform.
Delta VOS	ΔVOS	–	–	50	mV	See Figure 16 for waveform.
Rise/Fall Time	Tr, Tf	–	70	100	ps	Measured 20% to 80% using Figure 31 for termination. See Figure 15 for waveform.
Differential Asymmetry, peak-peak	V_da	–	25	–	mV	See Figure 17 for waveform.
Differential Skew, peak	V_ds	–	± 40	–	ps	See Figure 18 for waveform.
Overshoot Voltage, peak	V_ov	–	16	–	%	Measured as percent of VOD. See Figure 20 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	14	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	3.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 8 .
Power Supply-Induced Phase Noise	PSPN	–	-63	–	dBc	50 mV peak-peak ripple on VDD.
		–	-76	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 8 .

Table 8. Electrical Characteristics – LVDS | Supply voltage (“order code”): 1.8 V \pm 5% (“18”), 1.71 V to 3.63 V (“YY”). All typical specifications are measured at nominal supply of 2.5 V and nominal frequency of 622.08 MHz unless otherwise stated. See [Figure 8](#) and [Figure 9](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	I _{dd_oe_nt}	–	40.5	48	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	I _{dd_oe_wt}	–	44.5	51.5	mA	Including load termination current. See Figure 31 for termination.
Current Consumption Output Disabled with Termination	I _{dd_od_wt}	–	46	52	mA	Including load termination current. See Figure 31 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Differential Output Voltage	V _{OD}	250	345	450	mV	See Figure 16 for waveform.
Delta VOD	Δ V _{OD}	–	–	50	mV	See Figure 16 for waveform.
Offset Voltage	V _{OS}	1.125	1.25	1.375	V	See Figure 16 for waveform.
Delta VOS	Δ V _{OS}	–	–	50	mV	See Figure 16 for waveform.
Rise/Fall Time	T _r , T _f	–	70	100	ps	Measured 20% to 80% using Figure 31 for termination. See Figure 15 for waveform.
Differential Asymmetry, peak-peak	V _{da}	–	25	–	mV	See Figure 17 for waveform.
Differential Skew, peak	V _{ds}	–	\pm 40	–	ps	See Figure 18 for waveform.
Overshoot Voltage, peak	V _{ov}	–	16	–	%	Measured as percent of V _{OD} . See Figure 20 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	16	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	3.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 8 .
Power Supply-Induced Phase Noise	PSPN	–	-62	–	dBc	50 mV peak-peak ripple on VDD.
		–	-76	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 8 .

Table 9. Electrical Characteristics – HCSL | Supply voltage (“order code”): 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”), 1.8 V $\pm 5\%$ (“18”), 1.71 V to 3.63 V (“YY”). All typical specifications are measured at nominal supply of 2.5V and nominal frequency of 322.265625 MHz unless otherwise stated. See [Figure 10](#) and [Figure 11](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	38	43.5	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	52	57.5	mA	Including load termination current. See Figure 32 (a) and Figure 32 (b) for termination.
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	56.5	62.5	mA	Including load termination current. See Figure 32 (a) and Figure 32 (b) for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.52	0.7	0.85	V	See Figure 14 for waveform.
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 14 for waveform.
Output Differential Voltage Swing	V_Swing	1.0	1.25	1.5	V	See Figure 15 for waveform.
Rise/Fall Time	Tr, Tf	–	65	95	ps	See Figure 23 for waveform.
Ring-back Voltage	Rb	210	–	–	mV	See Figure 23 for waveform.
Differential Asymmetry, peak-peak	V_da	–	65	–	mV	See Figure 17 for waveform.
Differential Skew, peak	V_ds	–	± 70	–	ps	See Figure 18 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	12	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	2.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 10 .
Power Supply-Induced Phase Noise	PSPN	–	-70	–	dBc	50 mV peak-peak ripple on VDD
		–	-83.5	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 10 .

Table 10. Electrical Characteristics – Low-Power HCSL | Supply voltage (“order code”): 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”), 1.8 V $\pm 5\%$ (“18”), 1.71 V to 3.63 V (“YY”). All typical specifications are measured at nominal supply of 2.5V and nominal frequency of 350 MHz unless otherwise stated. See [Figure 12](#) and [Figure 13](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	40	45	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	41	46.5	mA	Including load termination current. See Figure 33 for termination.
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	37	42	mA	Including load termination current. See Figure 33 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.8	0.9	1.15	V	See Figure 14 for waveform.
Output Low Voltage	VOL	-0.15	0	0.1	V	See Figure 14 for waveform.
Output Differential Voltage Swing	V_Swing	1.6	2	2.25	V	See Figure 15 for waveform.
Rise/Fall Time	Tr, Tf	–	255	330	ps	Measured 20% to 80%. See Figure 15 for waveform.
Differential Asymmetry, peak-peak	V_da	–	55	–	mV	See Figure 17 for waveform.
Differential Skew, peak	V_ds	–	± 30	–	ps	See Figure 18 for waveform.
Overshoot Voltage, peak	V_ov	–	1	–	%	Measured as percent of V_Swing. See Figure 19 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	16.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	5.0	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 12 .
Power Supply-Induced Phase Noise	PSPN	–	-67	–	dBc	50 mV peak-peak ripple on VDD.
		–	-77.5	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 12 .

Table 11. Absolute Maximum Ratings

Operation outside the absolute maximum ratings may cause permanent damage to the part.
Performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Min.	Max.	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5	4.0	V
Input Voltage, Maximum	Any input pin	–	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	–	V
Storage Temperature		-65	150	°C
Maximum Junction Temperature		–	150	°C

Table 12. Thermal Considerations^[4]

Package	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	θ_{JB} (°C/W)	$\theta_{JC,Top}$ (°C/W)
3225, 6-pin	101	4.7	23	86
2520, 6-pin	111	3.7	24	116
2016, 6-pin	134	3.4	24	147

Notes:

- θ_{JA} , Ψ_{JT} , θ_{JB} and θ_{JC} are provided according to JEDEC standards 51-2A, 51-7, 51-8, and 51-12.01 with a 25°C ambient and 250 mW power consumption (typical of 1 GHz f_{out}). The conduction thermal resistances θ_{JB} and θ_{JC} are obtained with the assumption that all heat flows from the junction to a heat sink through either the solder pads (θ_{JB}) or the top of the package ($\theta_{JC,Top}$). These may be used in a two-resistor compact model. The values of θ_{JA} and Ψ_{JT} are strongly application dependent, and we report values based on the JEDEC thermal environment. θ_{JA} is the thermal resistance to ambient on a JEDEC PCB - it is a highly conservative estimate, since the JEDEC board does not have vias to PCB planes in the vicinity of the package. Ψ_{JT} can be used to estimate the junction temperature from measurements of the temperature at the top of the package if the thermal environment is similar to the JEDEC environment.

Table 13. Maximum Operating Junction Temperature^[5]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	85°C
85°C	100°C
95°C	110°C
105°C	120°C
125°C	145°C

Notes:

- Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 14. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	g
Soldering Temperature (follow standard Pb free soldering guidelines) ^[6]	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Notes:

- Please refer to [SiTime Manufacturing Notes](#).

Pin Description

Table 15. Pin Description

Pin	Map	Functionality	
1	OE/NF	Output Enable (OE)	H ^[7] : Specified frequency output L ^[8] : OUT: Logic HIGH,
		No Function (NF)	Open, 120 kΩ internal pull-down resistor to GND
2	NF	No Function	H or L or Open: No effect on output frequency or other device functions. ^[9]
3	GND	Power	Power Supply Ground
4	OUTP	Output	Oscillator output
5	OUTN	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage ^[10]

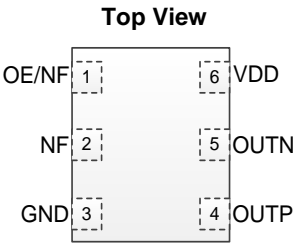


Figure 3. Pin Assignments

- Notes:
- 7. OE pin includes a 120 kΩ internal pull-up resistor to VDD when active high, and a 120 kΩ internal pull-down resistor to GND when active low. In noisy environments, the OE pin is recommended to include an external 10 kΩ resistor (Use 10kΩ pull-up if active high OE; use 10kΩ pull-down if active low OE) when the pin is not externally driven.
 - 8. Differential Logic high means OUTP=VOH, OUTN=VOL.
 - 9. Can be left open. SiTime recommends grounding it for better thermal performance.
 - 10. A capacitor of value 0.1 μF or higher between VDD and GND pins is required.

Order Code V_Swing (V)																										
			C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y			
			0.45V	0.49V	0.54V	0.59V	0.64V	0.69V	0.74V	0.79V	0.84V	0.89V	0.94V	0.99V	1.03V	1.08V	1.16V	1.23V	1.3V	1.38V	1.45V	1.53V	1.6V			
VHn	A	VLn + V_Swing / 2																		AV	AW	AX	AY			
																				1.94	1.86	1.69	1.61			
	B		Supply Voltage		Available Colors																	BV	BW	BX	BY	
			1.8V±5%		Orange	Green																	1.86	1.77	1.61	1.52
	C		1.71V to 3.63V		Green																CU	CV	CW	CX	CY	
			2.5V±10%		Orange	Green		Blue	Purple										1.94	1.77	1.69	1.52	1.44			
	D		3.3V±10%		Green				Blue	Red									DT	DU	DV	DW	DX	DY		
			2.25V to 3.63V		Green				Blue										1.94	1.86	1.69	1.61	1.44	1.35		
	E		Note 12		Gray																ET	EU	EV	EW	EX	EY
																				1.86	1.77	1.61	1.52	1.35	1.27	
	F																		FS	FT	FU	FV	FW	FX	FY	
																			1.94	1.77	1.69	1.52	1.44	1.27	1.18	
	G															1.94			GS	GT	GU	GV	GW	GX	GY	
																	1.94		1.86	1.69	1.61	1.44	1.35	1.18	1.10	
	H															1.94	1.86		HS	HT	HU	HV	HW	HX	HY	
																		1.77	1.61	1.52	1.35	1.27	1.10	1.01	1.01	
	J														1.94	1.86	1.77		JS	JT	JU	JV	JW	JX	JY	
																1.94	1.86	1.77		1.69	1.52	1.44	1.27	1.18	1.01	0.93
	K															1.94	1.86	1.77		KS	KT	KU	KV	KW	KX	KY
																				1.61	1.44	1.35	1.18	1.10	0.93	0.85
	L												1.94	1.86	1.77	1.69	1.61		LS	LT	LU	LV	LW	LX	LY	
																		1.52	1.35	1.27	1.10	1.01	0.85	0.76	0.68	
	M												1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.27	1.18	1.01	0.93	0.76	0.68	
																		MR	MS	MT	MU	MV	MW	MX	MY	
N											1.94	1.86	1.77	1.69	1.61	NQ	NR	NS	NT	NU	NV	NW	NX	NY		
																1.52	1.44	1.35	1.18	1.10	0.93	0.85	0.68	0.59		
P																PP	PQ	PR	PS	PT	PU	PV	PW	PX	PY	
																	1.44	1.35	1.27	1.10	1.01	0.85	0.76	0.59	0.51	
Q																QN	QP	QQ	QR	QS	QT	QU	QV	QW	QX	

Rev 1.05

Test Circuit Diagrams

A 1.5 pF capacitive load is used at each differential output. Because of the additive input capacitance of the active probe used with the oscilloscope, the output characteristics for all signal types are measured with a total of 2 pF capacitive load.

Test Setups for LVPECL Measurements

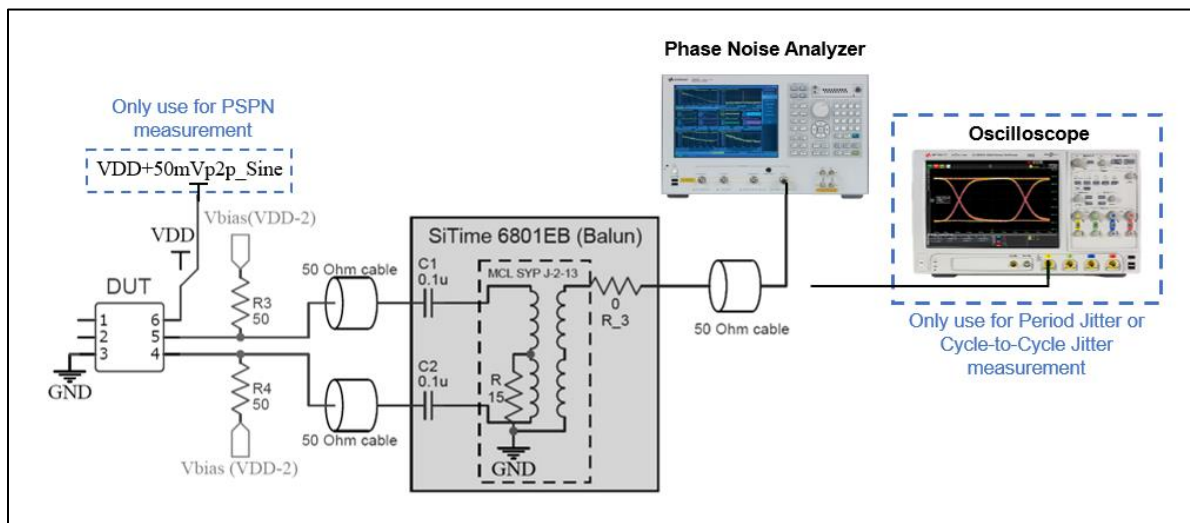


Figure 4. Test setup to measure LVPECL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) without filter added^[13]

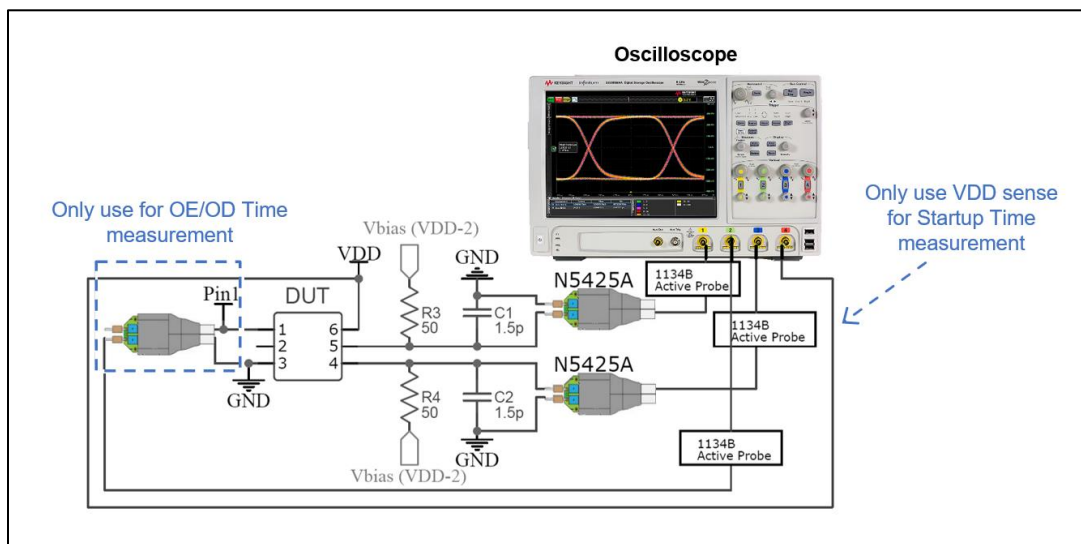


Figure 5. Test setup to measure LVPECL Output Waveform Characteristics, Current Consumption (with Termination 2)^[14], Output Enable/Disable Time, and Startup Time

Notes:

13. See Figure 6 for the test setup to measure LVPECL Power Supply-Induced Phase Noise (PSPN) with filter added.
14. See Figure 7 for the test setup to measure LVPECL Current Consumption with Termination 1 or without Termination.

Test Circuit Diagrams (continued)

Test Setups for LVDS Measurements

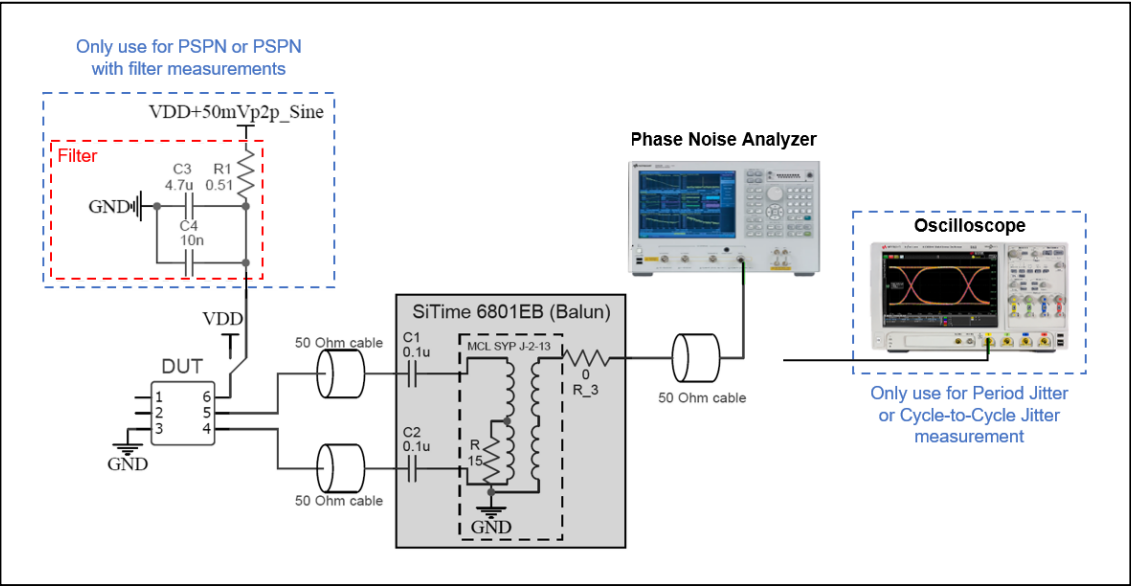


Figure 8. Test setup to measure LVDS Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added

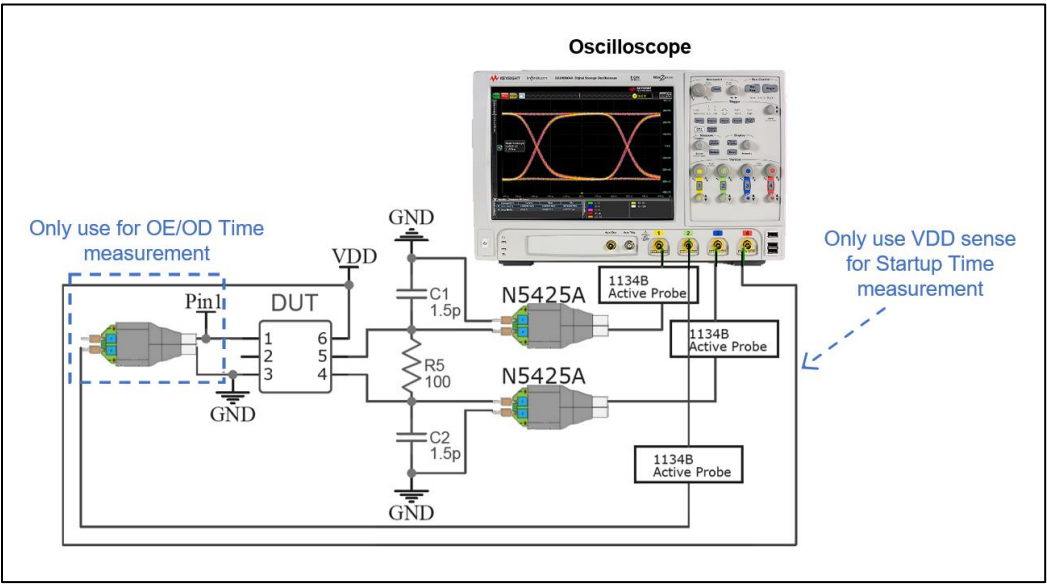


Figure 9. Test setup to measure LVDS Output Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time

Test Circuit Diagrams (continued)

Test Setups for Low-Power HCSL Measurements

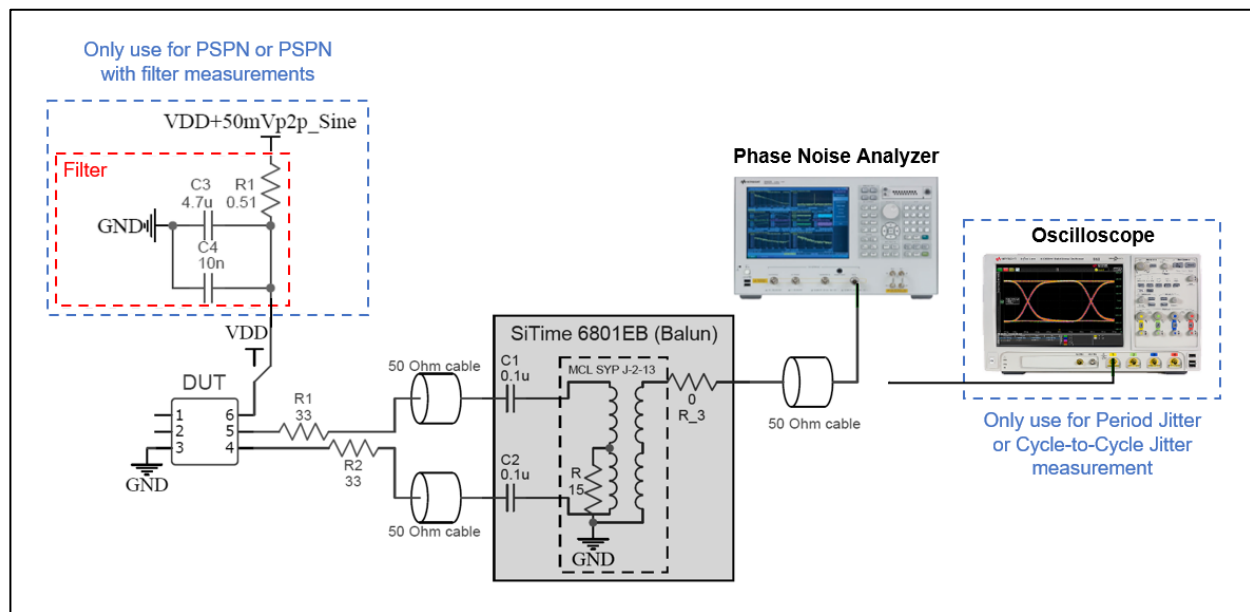


Figure 12. Test setup to measure Low-Power HCSL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and PowerSupply-Induced Phase Noise (PSPN) with and without filter added

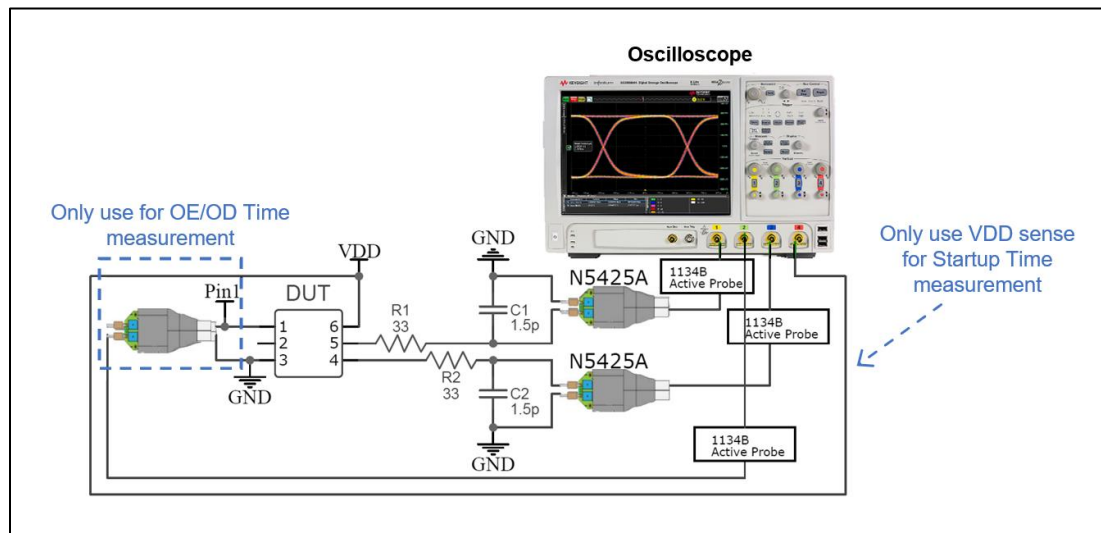


Figure 13. Test setup to measure Low-Power HCSL Output Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time

Waveform Diagrams

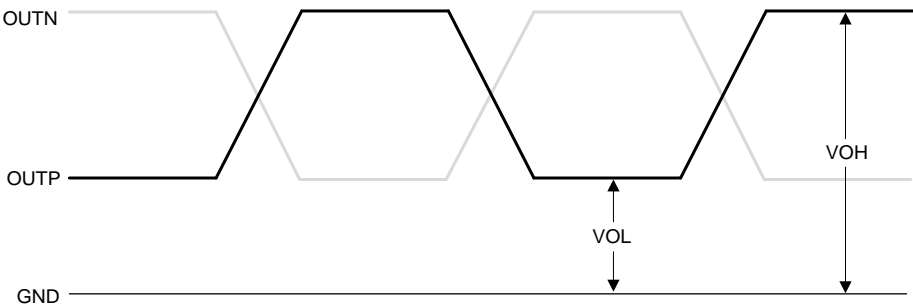


Figure 14. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels per Differential Pin

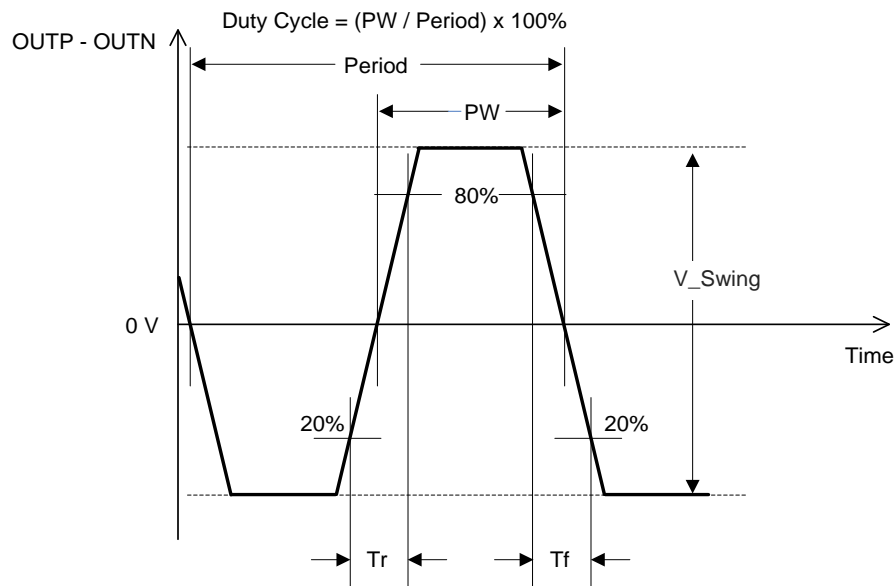


Figure 15. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels Across Differential Pair

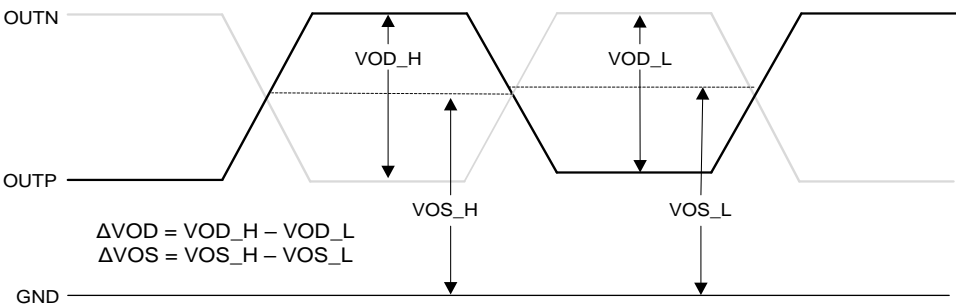


Figure 16. LVDS Voltage Levels per Differential Pin

Waveform Diagrams (continued)

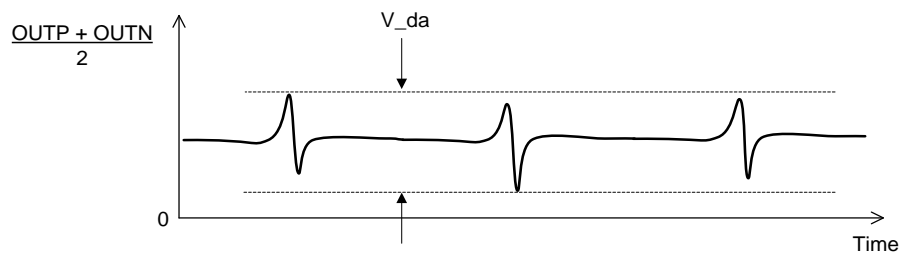


Figure 17. Differential Asymmetry (V_{da})

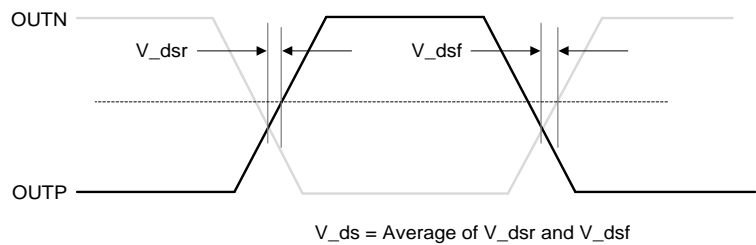


Figure 18. Differential Skew (V_{ds}) is measured as the Time between the Average Voltage Level and Crossing Voltage

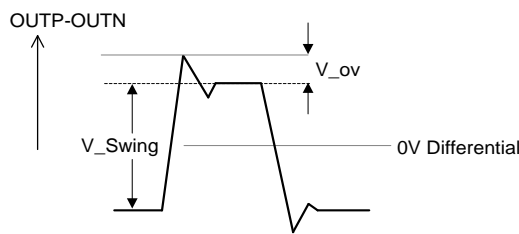


Figure 19. Overshoot Voltage (V_{ov}) for LVPECL, FlexSwing, HCSL, Low-power HCSL

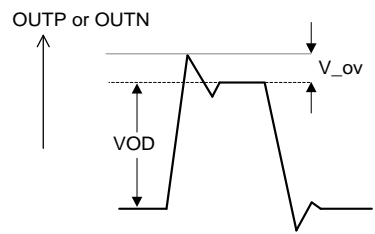


Figure 20. Overshoot Voltage (V_{ov}) for LVDS Output

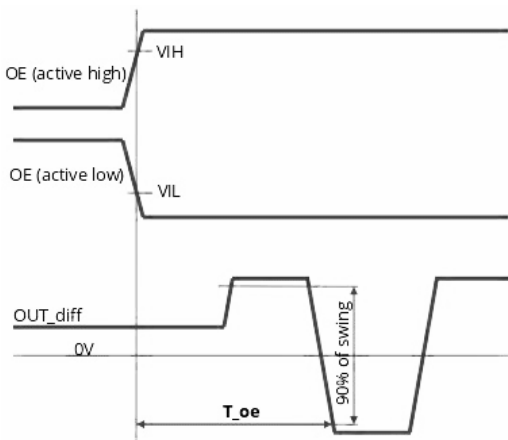


Figure 21. OE Pin Enable Timing (T_{oe})

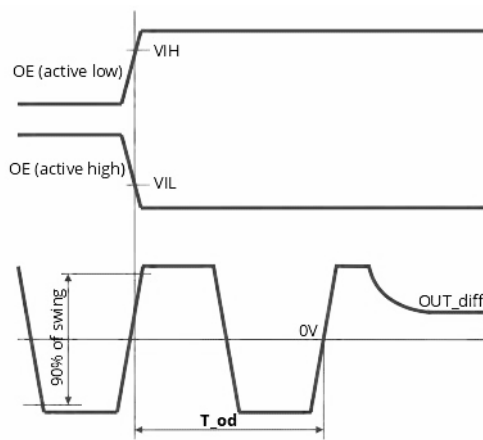


Figure 22. OE Pin Disable Timing (T_{od})

Waveform Diagrams (continued)

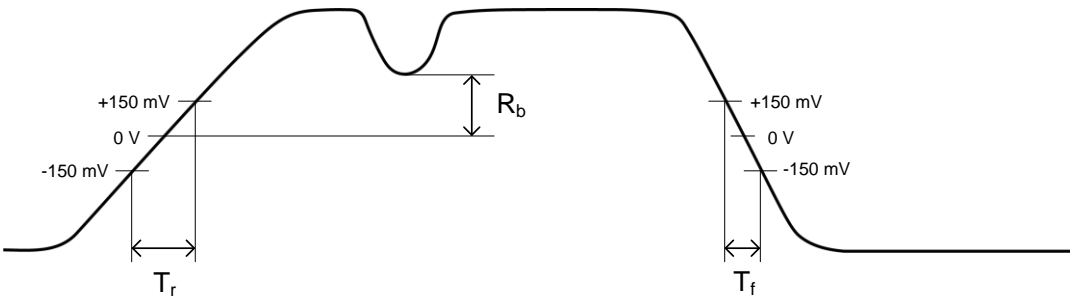


Figure 23. Ring Back Voltage Test Condition

Termination Diagrams

LVPECL and FlexSwing Termination

The SiT9397 FlexSwing output drivers support low power without sacrificing signal integrity via simple terminations as shown in [Figure 25](#) and [Figure 27](#), compared to traditional LVPECL drivers. The FlexSwing and LVPECL outputs are

voltage-mode drivers. Use the table and figures below to select a termination circuit for the desired supply voltage. The table also provides LVPECL current consumption (I_{load}) into the load termination.

Table 18. Termination Options for LVPECL and FlexSwing Signaling

Signaling	Supply Voltage Order Codes	Termination Options					
		Figure 24	Figure 25	Figure 26	Figure 27	Figure 28	Figure 29
LVPECL referenced to Vdd	"25", "33", "XX"	OK to use $I_{load} = 40\text{ mA}$ with $100\text{ }\Omega$ near-end bias resistor	Do Not Use	OK to use $I_{load} = 28\text{ mA}$	OK to use	OK to use $I_{load} = 28\text{ mA}$	Do Not Use
FlexSwing referenced to Vdd			OK to use (See Figure 25 for frequency ranges and voltage swings)	OK to use ^[19]	OK to use	OK to use	Do Not Use
FlexSwing referenced to Gnd	"25", "33", "XX", "YY"	OK to use ^[18]		Do Not Use	OK to use	Do Not Use	Do Not Use
	"18"			Do Not Use	OK to use	Do Not Use	OK to use

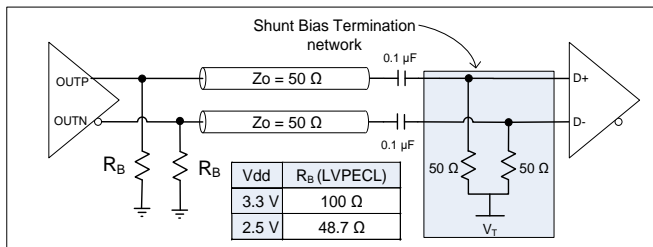


Figure 24. Recommended LVPECL and FlexSwing^[18] Termination when AC-coupled

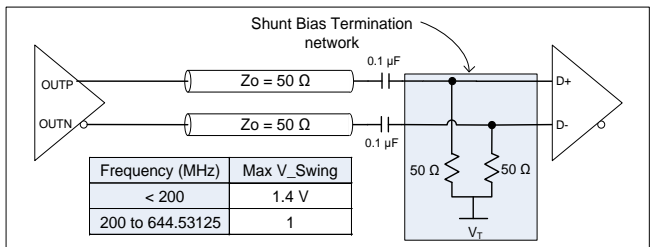


Figure 25. Recommended FlexSwing Termination when AC-coupled

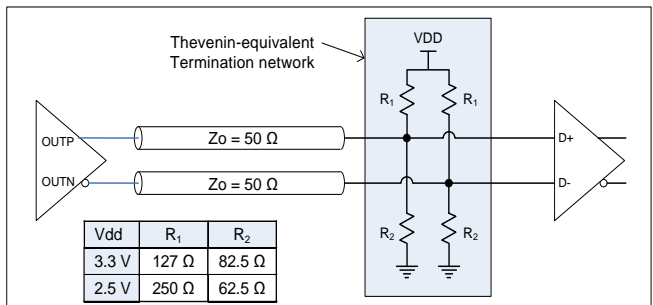


Figure 26. LVPECL and FlexSwing DC-coupled Load Termination with Thevenin Equivalent Network^[19]

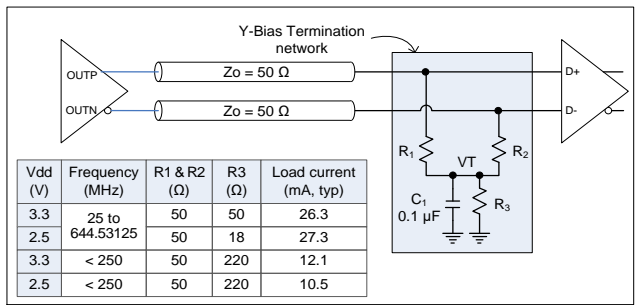


Figure 27. LVPECL and FlexSwing with DC-coupled Parallel Shunt Load Termination

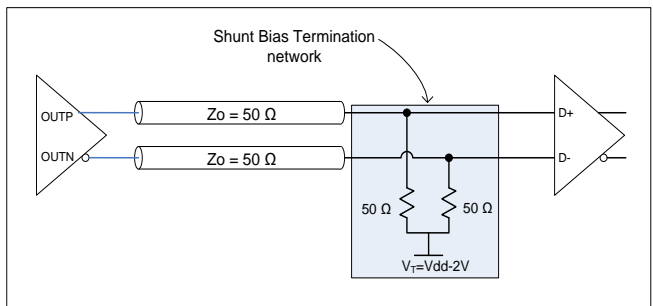


Figure 28. LVPECL and FlexSwing with Y-Bias Termination

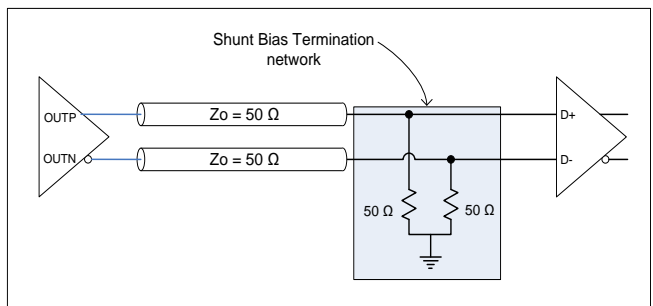


Figure 29. FlexSwing Termination – Only for use with Supply Voltage Order Code “18”

Termination Diagrams (continued)

LVDS, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

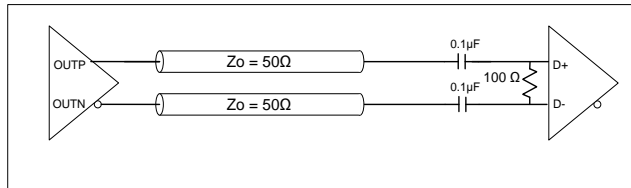


Figure 30. LVDS AC Termination

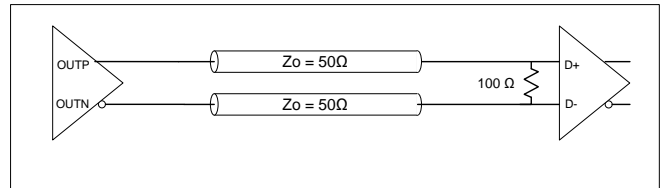


Figure 31. LVDS DC Termination at the Load

HCSL, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

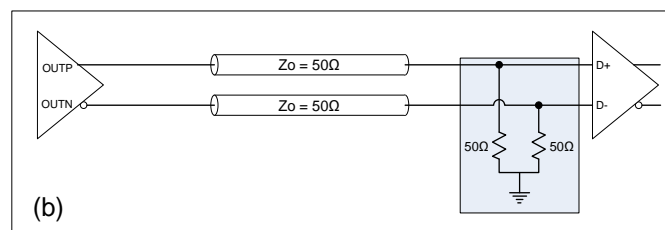
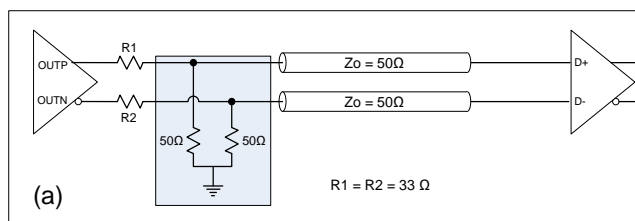


Figure 32. (a) HCSL Source Termination and (b) HCSL Load Termination

Low-power HCSL, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

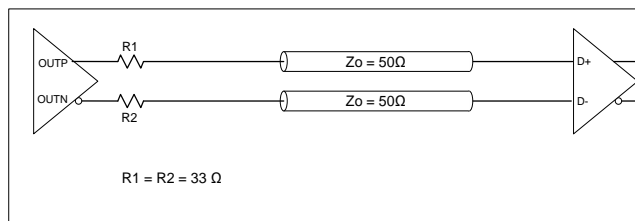
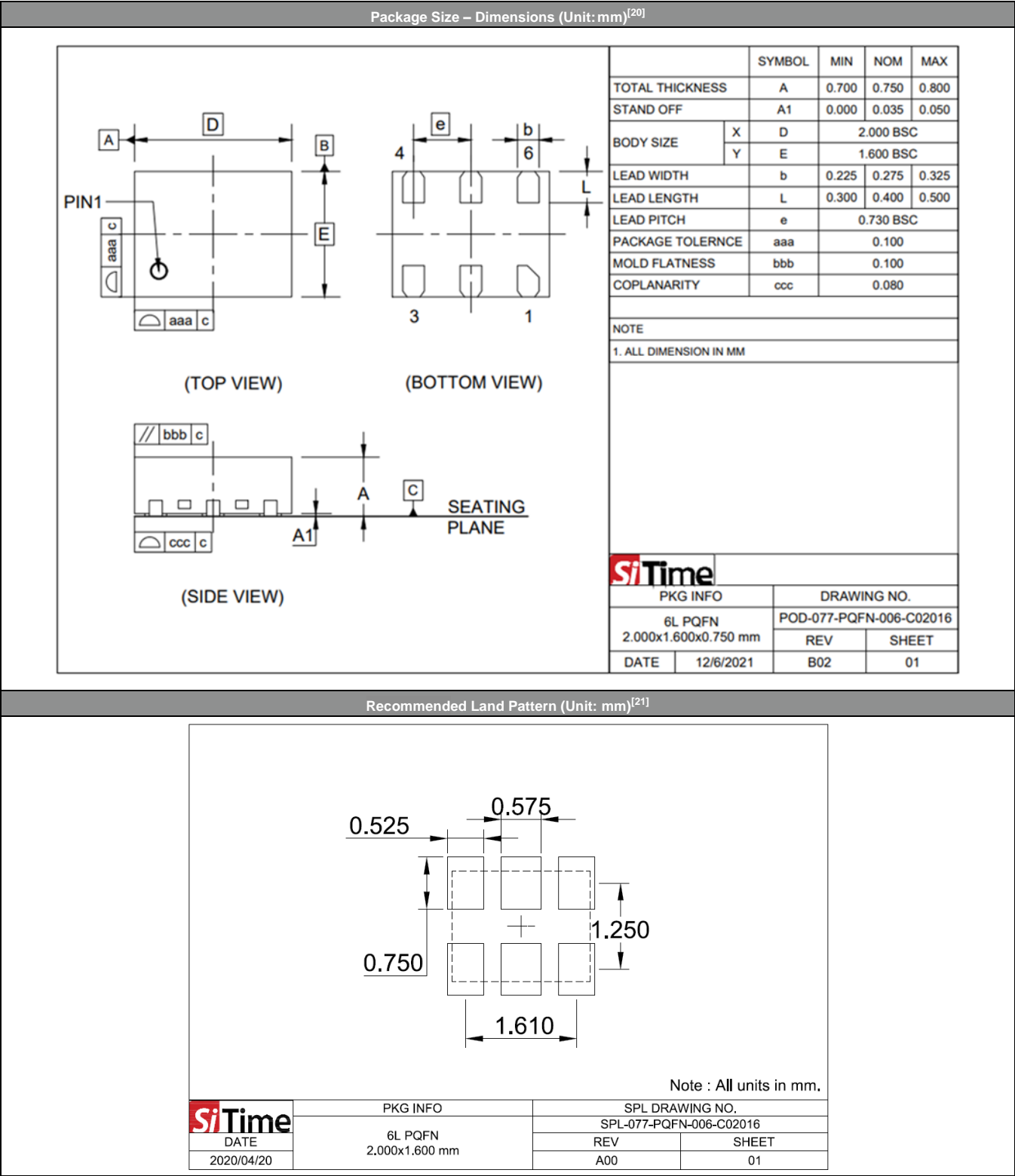


Figure 33. Low-power HCSL Termination

Notes:

18. [Contact SiTime](#) for optimum R_B values for FlexSwing options.
19. [Contact SiTime](#) for optimum R_1 and R_2 values for FlexSwing options.

Dimensions and Patterns — 2.0 x 1.6 mm x mm

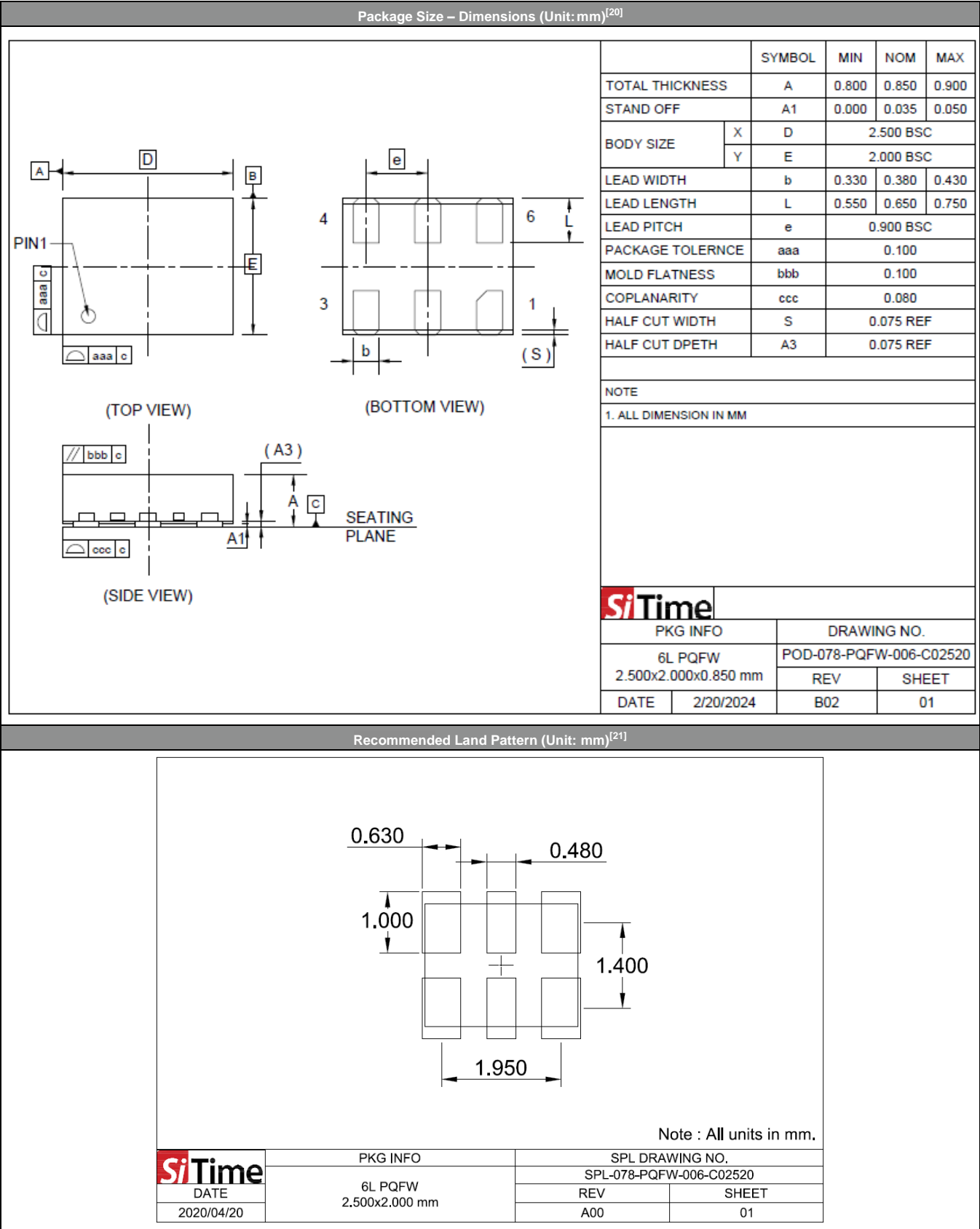


Notes:

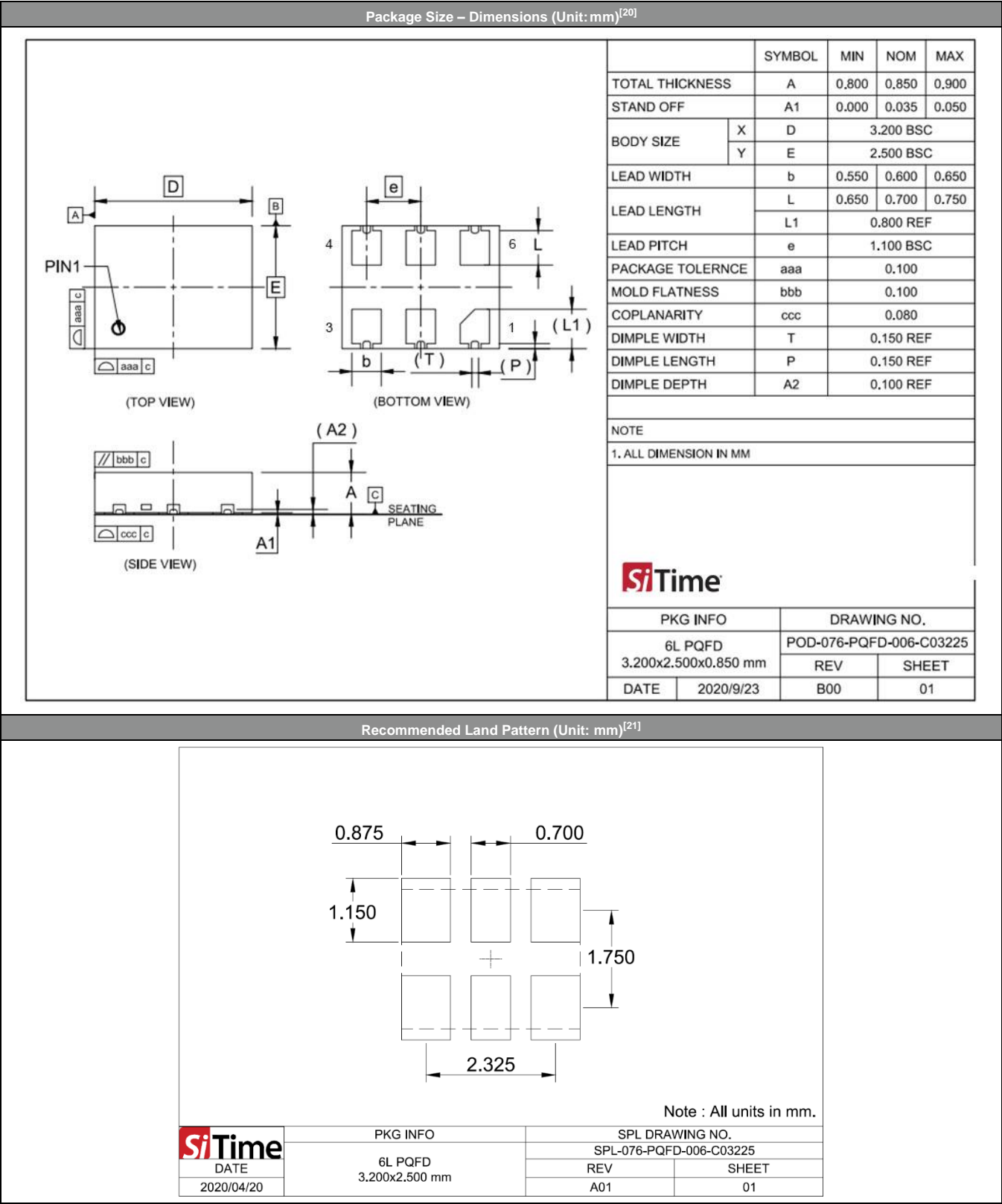
20. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.

21. A capacitor of value 0.1 μ F or higher between VDD and GND is required. An additional 10 μ F capacitor between VDD and GND is required for the best phase jitter performance.

Dimensions and Patterns — 2.5 x 2.0 mm x mm



Dimensions and Patterns — 3.2 x 2.5 mm x mm



Additional Information

Table 19. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the Commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes
Evaluation Boards	SiT6760EB	https://www.sitime.com/support/development-tools/evaluation-boards

Revision History

Table 20. Revision History

Revision	Release Date	Change Summary
0.1	10-May-2022	Advanced datasheet
0.65	12-Aug-2022	Preliminary datasheet Added Test Diagrams section Updated Electrical Characteristics tables and descriptions Updated frequency range
0.66	23-Sep-2022	Formatting Updates
0.67	1-Jan-2023	Updated company disclaimer, links, references and icons
0.7	30-Aug-2023	Updated 2520 package Dimensions drawing Updated Maximum Junction Temperature in Table 11 and Table 13
0.71	6-Nov-2023	Updated 3225 package Dimensions drawing
0.8	8-Dec-2023	Updated Electrical Characteristics
0.9	8-Jan-2024	Added Figure 23
1.0	20-Jan-2024	Final characterization data, Removed Preliminary Label
1.01	25-Jan-2024	Removed Additional Package info, Edited Ordering Information LPHCSL description
1.02	26-Jan-2024	Corrected PSJS text in features, typographical errors
1.03	20-Feb-2024	Corrected Package Dimensions Table for 2520 package
1.04	8-Apr-2024	Updated Ordering Information
1.05	31-Jan-2025	Updated HCSL specifications

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