

Description

The SiT9375 is a differential MEMS oscillator that is engineered for low-jitter applications requiring standard frequencies from 25 MHz to 644.53125 MHz.

A unique FlexSwing output-driver performs like LVPECL but provides independent control of voltage swing and DC offset to simplify interfacing with chipsets having non-standard input voltage requirements and eliminate all external source-bias resistors. The device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for an external dedicated LDO.

The SiT9375 can be factory programmed for specific combinations of frequency, stability, voltage, output signaling, and pin 1 functionality. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each combination is custom built.

The wide frequency range and programmability makes this device ideal for communications, enterprise, and industrial applications that require a variety of frequencies and operate in noisy environments.

Refer to [Manufacturing Notes](#) for proper reflow profile, tape and reel dimension, and other manufacturing related information.

Features

- Standard frequencies from 25 MHz to 644.53125 MHz
- 200 fs RMS typical phase jitter, 12 kHz to 20 MHz
- Excellent power-supply noise rejection
- LVPECL, LVDS, HCSL, Low-power HCSL, and FlexSwing signaling options
- ± 20 , ± 25 , ± 30 , and ± 50 ppm frequency stabilities
- Wide temperature support up to -40°C to 105°C
- Factory programmable options for low lead time
- 1.8 V, 2.5 V, 3.3 V, and wide continuous range power supply voltage
- 2 x 1.6, 2.5 x 2, 3.2 x 2.5 mm x mm package ([Contact SiTime](#) for 7 x 5, and 5 x 3.2 mm x mm packages)

Applications

- 100G/200G/400G network equipment
- Optical modules
- Coherent optics
- Network switches, routers
- Industrial networking equipment
- Server and storage systems
- Industrial networks
- Test and measurement
- Broadcast video

Block Diagram

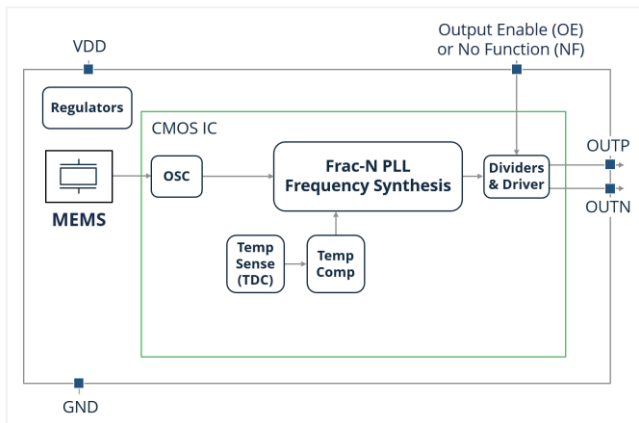


Figure 1. SiT9375 Block Diagram

Package Pinout

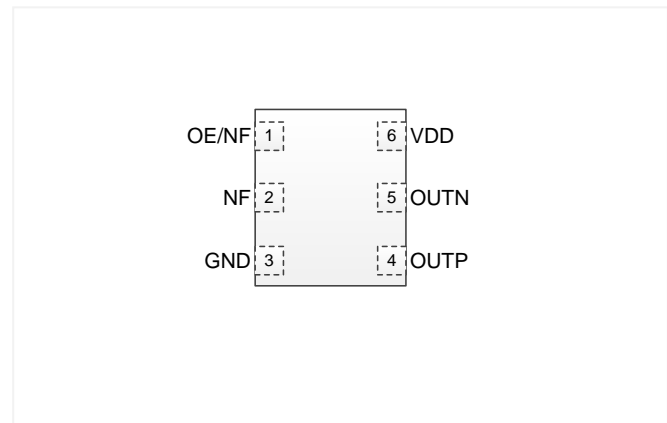


Figure 2. Pin Assignments (Top view)
(Refer to [Table 17](#) for Pin Descriptions)

Ordering Information

SiT9375AC-01B2-3310-125.000000T

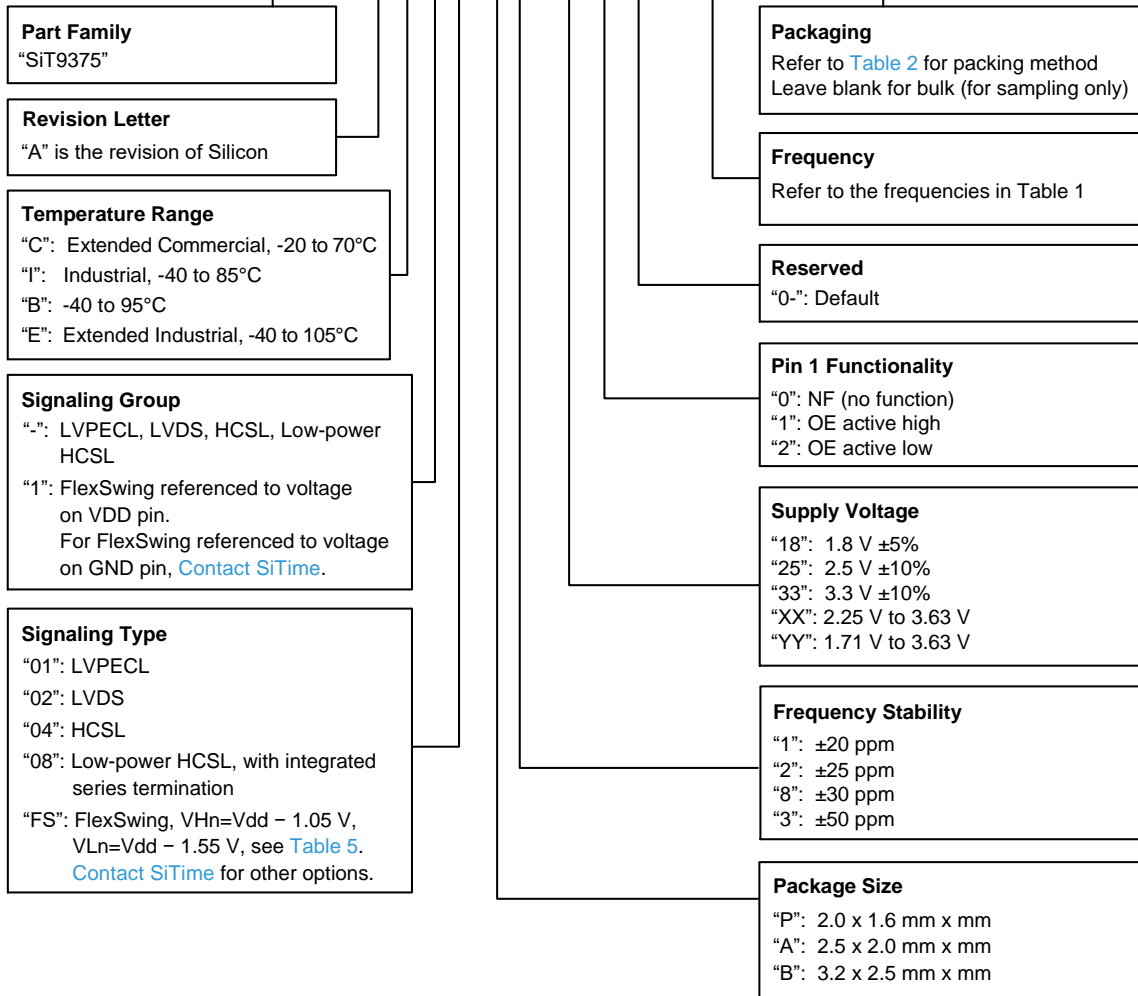


Table 1. Supported Frequencies

25.000000 MHz	30.720000 MHz	50.000000 MHz	53.125000 MHz	61.440000 MHz	62.500000 MHz	74.250000 MHz	75.000000 MHz
98.304000 MHz	100.000000 MHz	106.250000 MHz	122.880000 MHz	125.000000 MHz	133.333333 MHz	148.500000 MHz	150.000000 MHz
153.600000 MHz	155.520000 MHz	156.250000 MHz	159.375000 MHz	160.000000 MHz	161.132813 MHz	166.666666 MHz	200.000000 MHz
212.500000 MHz	250.000000 MHz	300.000000 MHz	312.500000 MHz	322.265625 MHz	625.000000 MHz	644.531250 MHz	

Table 2. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)
2.0 x 1.6	D	E
2.5 x 2.0	D	E
3.2 x 2.5	D	E

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 HCSL, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V 18

 Low-power HCSL, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V 18

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Dimensions and Patterns — 2.5 x 2.0 mm x mm 20

Dimensions and Patterns — 3.2 x 2.0 mm x mm 21

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Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over operating temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Table 3. Electrical Characteristics – Common to All Output Signaling Types

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	Standard frequencies			MHz	Refer to frequencies listed in Ordering Information section.
Frequency Stability						
Frequency Stability	F_stab	–	–	±20	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 15 pF ± 10%, and 10 years aging at 25°C
		–	–	±25	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 15 pF ± 10%, and first year aging at 25°C
		–	–	±30	ppm	
		–	–	±50	ppm	
10 Year Aging	F_10y	–	±1	–	ppm	Ambient temperature of 25°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended commercial, ambient temperature
		-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+95	°C	Ambient temperature
		-40	–	+105	°C	Extended industrial, ambient temperature
Supply Voltage						
Supply Voltage	Vdd	1.71	–	3.63	V	Voltage-supply order code "YY"
		2.25	–	3.63	V	Voltage-supply order code "XX"
		1.71	1.80	1.89	V	Voltage-supply order code "18". Contact SiTime for 1.5 V
		2.25	2.50	2.75	V	Voltage-supply order code "25"
		2.97	3.30	3.63	V	Voltage-supply order code "33"
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pins 1 and 2 for OE and SE, respectively
Input Voltage Low	VIL	–	–	30%	Vdd	Pins 1 and 2 for OE and SE, respectively
Input Pull-up Impedance	Z_in	–	100	–	kΩ	Pins 1 and 2 for OE and SE, respectively
Output Characteristics						
Duty Cycle	DC	45	–	55	%	See Figure 5 and Figure 7
Startup, OE and SE Timing						
Startup Time	T_start	–	1	5	ms	Measured from the time Vdd reaches its rated minimum value
Output Enable Time	T_oe	–	–	100+3 clock cycles	ns	Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of swing. See Figure 12
Output Disable Time	T_od	–	–	100+3 clock cycles	ns	Measured from the time OE pin toggles to disable logic level to the last clock edge. See Figure 13
Jitter and Phase Noise						
RMS Phase Jitter (random)	T_phj	–	200	–	fs	12 kHz to 20 MHz offset frequency integration bandwidth, 156.25 MHz
Spurious Phase Noise	PN_spur_a	–	-110	–	dBc	12 kHz to 20 MHz offset frequency range, 156.25 MHz
	PN_spur_b	–	-80	–	dBc	12 kHz to 20 MHz offset frequency range, 155.52 MHz
RMS Period Jitter^[1]	T_jitt_per	–	1	–	ps	156.25 MHz
Peak Cycle-to-cycle Jitter^[1]	T_jitt_cc	–	6	–	ps	156.25 MHz

Note:

1. Measured according to JESD65B.

Table 4. Electrical Characteristics – LVPECL | Supply voltages: 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	I _{dd_oe_nt}	–	43	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination 1	I _{dd_oe_wt1}	–	52	–	mA	Including load termination current. See Figure 15 for termination
Current Consumption, Output Enabled with Termination 2	I _{dd_oe_wt2}	–	71	–	mA	Including load termination current. See Figure 18 for termination
Current Consumption, Output Disabled without Termination	I _{dd_od_nt}	–	58	–	mA	Excluding load termination current
Current Consumption Output Disabled with Termination 1	I _{dd_od_wt1}	–	58	–	mA	Including load termination current. See Figure 15 for termination
Current Consumption, Output Disabled with Termination 2	I _{dd_od_wt2}	–	86	–	mA	Including load termination current. See Figure 18 for termination
OE Leakage Current	I _{leak}	–	37	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 13 . Use AC termination to reduce I _{leak} to 0 mA.
Output Characteristics						
Output High Voltage	VOH	V _{dd} -1.025	V _{dd} -0.95	V _{dd} -0.88	V	See Figure 4
Output Low Voltage	VOL	V _{dd} -1.81	V _{dd} -1.7	V _{dd} -1.62	V	See Figure 4
Output Differential Voltage Swing	V _{Swing}	1.2	1.5	1.9	V	See Figure 5
Rise/Fall Time	T _r , T _f	–	170	–	ps	20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V _{da}	–	100	–	mV	See Figure 8
Differential Skew, peak	V _{ds}	–	\pm 40	–	ps	See Figure 9
Overshoot Voltage, peak	V _{ov}	–	10	–	%	Measured as percent of V _{Swing} ; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 5. Electrical Characteristics – FlexSwing | Supply voltage: 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	I _{dd_oe_nt}	–	43	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	I _{dd_oe_wt}	–	52	–	mA	Including load termination current. See Figure 15 for termination
Current Consumption, Output Disabled without Termination	I _{dd_od_nt}	–	58	–	mA	Excluding load termination current
Current Consumption Output Disabled with Termination	I _{dd_od_wt}	–	58	–	mA	Including load termination current. See Figure 15 for termination
OE Leakage Current	I _{leak}	–	37	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 13 . Use AC termination to reduce I _{leak} to 0 mA.
Output Characteristics						
Output High Voltage	VOH	V _{Hn} - 0.1	V _{Hn}	V _{Hn} + 0.1	V	See Figure 4 , Refer to Table 18 or Table 19 order codes for nominal VOH (i.e. V _{Hn}) values.
Output Low Voltage	VOL	V _{Ln} - 0.1	V _{Ln}	V _{Ln} + 0.1	V	See Figure 4 , Refer to Table 18 or Table 19 order codes for nominal VOL (i.e. V _{Ln}) values
Output Differential Voltage Swing	V _{Swing}	VOH - VOL			V	See Figure 5
Rise/Fall Time	T _r , T _f	–	170	–	ps	20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V _{da}	–	100	–	mV	See Figure 8
Differential Skew, peak	V _{ds}	–	\pm 40	–	ps	See Figure 9
Overshoot Voltage, peak	V _{ov}	–	10	–	%	Measured as percent of V _{Swing} ; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 6. Electrical Characteristics – FlexSwing | Supply voltage referred to GND, only: 1.8 V \pm 5%, 1.71 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	I _{dd_oe_nt}	–	43	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	I _{dd_oe_wt}	–	52	–	mA	Including load termination current. See Figure 15 for termination
Current Consumption, Output Disabled without Termination	I _{dd_od_nt}	–	58	–	mA	Excluding load termination current
Current Consumption Output Disabled with Termination	I _{dd_od_wt}	–	58	–	mA	Including load termination current. See Figure 15 for termination
OE Leakage Current	I _{leak}	–	37	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 13 . Use AC termination to reduce I _{leak} to 0 mA.
Output Characteristics						
Output High Voltage	VOH	V _{Hn} - 0.1	V _{Hn}	V _{Hn} + 0.1	V	See Figure 4 , Refer to Table 18 or Table 19 order codes for nominal VOH (i.e. V _{Hn}) values
Output Low Voltage	VOL	V _{Ln} - 0.1	V _{Ln}	V _{Ln} + 0.1	V	See Figure 4 , Refer to Table 18 or Table 19 order codes for nominal VOL (i.e. V _{Ln}) values
Output Differential Voltage Swing	V _{Swing}	VOH - VOL			V	See Figure 5
Rise/Fall Time	T _r , T _f	–	170	–	ps	20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V _{da}	–	100	–	mV	See Figure 8
Differential Skew, peak	V _{ds}	–	\pm 40	–	ps	See Figure 9
Overshoot Voltage, peak	V _{ov}	–	10	–	%	Measured as percent of V _{Swing} ; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 7. Electrical Characteristics – LVDS | Supply voltage: 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	I _{dd_oe_nt}	–	45	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	I _{dd_oe_wt}	–	49	–	mA	Including load termination current. See Figure 21 for termination
Current Consumption, Output Disabled without Termination	I _{dd_od_nt}	–	54	–	mA	Excluding load termination current
Current Consumption Output Disabled with Termination	I _{dd_od_wt}	–	57	–	mA	Including load termination current. See Figure 21 for termination
OE Leakage Current	I _{leak}	–	12.5	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 13 . Use AC termination to reduce I _{leak} to 0 mA.
Output Characteristics						
Differential Output Voltage	VOD	250	350	450	mV	See Figure 6
Delta VOD	ΔVOD	–	–	50	mV	See Figure 6
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 6
Delta VOS	ΔVOS	–	–	50	mV	See Figure 6
Rise/Fall Time	T _r , T _f	–	290	–	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%. See Figure 7
Differential Asymmetry, peak-peak	V _{da}	–	50	–	mV	See Figure 8
Differential Skew, peak	V _{ds}	–	±40	–	ps	See Figure 9
Overshoot Voltage, peak	V _{ov}	–	10	–	%	Measured as percent of VOD; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 8. Electrical Characteristics – LVDS | Supply voltage: 1.8 V ±5%, 1.71 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	I _{dd_oe_nt}	–	45	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	I _{dd_oe_wt}	–	49	–	mA	Including load termination current. See Figure 21 for termination
Current Consumption, Output Disabled without Termination	I _{dd_od_nt}	–	54	–	mA	Excluding load termination current
Current Consumption Output Disabled with Termination	I _{dd_od_wt}	–	57	–	mA	Including load termination current. See Figure 21 for termination
OE Leakage Current	I _{leak}	–	12.5	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 13 . Use AC termination to reduce I _{leak} to 0 mA.
Output Characteristics						
Differential Output Voltage	VOD	250	350	450	mV	See Figure 6
Delta VOD	ΔVOD	–	–	50	mV	See Figure 6
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 6
Delta VOS	ΔVOS	–	–	50	mV	See Figure 6
Rise/Fall Time	T _r , T _f	–	290	–	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%. See Figure 7
Differential Asymmetry, peak-peak	V _{da}	–	50	–	mV	See Figure 8
Differential Skew, peak	V _{ds}	–	±40	–	ps	See Figure 9
Overshoot Voltage, peak	V _{ov}	–	10	–	%	Measured as percent of VOD; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 9. Electrical Characteristics – HCSL | Supply voltage: 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	I _{dd_oe_nt}	–	41	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	I _{dd_oe_wt}	–	56	–	mA	Including load termination current. See Figure 22 (a) and Figure 22 (b) for termination.
Current Consumption, Output Disabled without Termination	I _{dd_od_nt}	–	49	–	mA	Excluding load termination current
Current Consumption, Output Disabled with Termination	I _{dd_od_wt}	–	64	–	mA	Including load termination current. See Figure 22 (a) and Figure 22 (b) for termination.
OE Leakage Current	I _{leak}	–	24	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 13
Output Characteristics						
Output High Voltage	VOH	0.60	0.7	0.95	V	See Figure 4
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 4
Output Differential Voltage Swing	V _{Swing}	1	1.4	1.6	V	See Figure 5
Rise/Fall Time	T _r , T _f	–	400	–	ps	Measured 20% to 80% using Figure 22 (b) for termination. See Figure 5
Differential Asymmetry, peak-peak	V _{da}	–	100	–	mV	See Figure 8
Differential Skew, peak	V _{ds}	–	±40	–	ps	See Figure 9
Overshoot Voltage, peak	V _{ov}	–	10	–	%	Measured as percent of V _{Swing} ; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 10. Electrical Characteristics – HCSL | Supply voltage: 1.8 V ±5%, 1.71 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	I _{dd_oe_nt}	–	41	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	I _{dd_oe_wt}	–	56	–	mA	Including load termination current. See Figure 22 (a) and Figure 22 (b) for termination.
Current Consumption, Output Disabled without Termination	I _{dd_od_nt}	–	49	–	mA	Excluding load termination current
Current Consumption, Output Disabled with Termination	I _{dd_od_wt}	–	64	–	mA	Including load termination current. See Figure 22 (a) and Figure 22 (b) for termination.
OE Leakage Current	I _{leak}	–	24	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 13
Output Characteristics						
Output High Voltage	VOH	0.60	0.7	0.95	V	See Figure 4
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 4
Output Differential Voltage Swing	V _{Swing}	1	1.4	1.6	V	See Figure 5
Rise/Fall Time	T _r , T _f	–	400	–	ps	Measured 20% to 80% using Figure 22 (b) for termination. See Figure 5
Differential Asymmetry, peak-peak	V _{da}	–	100	–	mV	See Figure 8
Differential Skew, peak	V _{ds}	–	±40	–	ps	See Figure 9
Overshoot Voltage, peak	V _{ov}	–	10	–	%	Measured as percent of V _{Swing} ; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 11. Electrical Characteristics – Low Power HCSL | Supply voltage: 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	I _{dd_oe_nt}	–	44	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	I _{dd_oe_wt}	–	46	–	mA	Including load termination current for 5pF loading at 156.25 MHz. See Figure 23 for termination
Current Consumption, Output Disabled without Termination	I _{dd_od_nt}	–	48	–	mA	Excluding load termination current
Current Consumption, Output Disabled with Termination	I _{dd_od_wt}	–	48	–	mA	Including load termination current for 5pF loading at 156.25 MHz. See Figure 23 for termination
OE Leakage Current	I _{leak}	–	9	–	mA	OE = disable logic, AC termination, OUP _T and OUP _{TN} held at constant voltage, see Figure 13
Output Characteristics						
Output High Voltage	VOH	0.8	0.9	1.15	V	See Figure 4
Output Low Voltage	VOL	-0.3	0	0.1	V	See Figure 4
Output Differential Voltage Swing	V _{Swing}	1.55	1.65	1.9	V	See Figure 5
Rise/Fall Time	T _r , T _f	–	520	–	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V _{da}	–	550	–	mV	See Figure 8
Differential Skew, peak	V _{ds}	–	\pm 30	–	ps	See Figure 9
Overshoot Voltage, peak	V _{ov}	–	10	–	%	Measured as percent of V _{Swing} ; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 12. Electrical Characteristics – Low Power HCSL | Supply voltage: 1.8 V \pm 5%, 1.71 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	I _{dd_oe_nt}	–	44	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	I _{dd_oe_wt}	–	46	–	mA	Including load termination current for 5 pF loading at 156.25 MHz. See Figure 23 for termination
Current Consumption, Output Disabled without Termination	I _{dd_od_nt}	–	48	–	mA	Excluding load termination current
Current Consumption, Output Disabled with Termination	I _{dd_od_wt}	–	48	–	mA	Including load termination current for 5 pF loading at 156.25 MHz. See Figure 23 for termination
OE Leakage Current	I _{leak}	–	9	–	mA	OE = disable logic, AC termination, OUP _T and OUP _{TN} held at constant voltage, see Figure 13
Output Characteristics						
Output High Voltage	VOH	0.8	0.9	1.15	V	See Figure 4
Output Low Voltage	VOL	-0.3	0	0.1	V	See Figure 4
Output Differential Voltage Swing	V _{Swing}	1.55	1.65	1.9	V	See Figure 5
Rise/Fall Time	T _r , T _f	–	520	–	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V _{da}	–	550	–	mV	See Figure 8
Differential Skew, peak	V _{ds}	–	\pm 30	–	ps	See Figure 9
Overshoot Voltage, peak	V _{ov}	–	10	–	%	Measured as percent of V _{Swing} ; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Note:

- Terminology chosen for clarity; referred to historically as power-supply noise rejection (PSNR).

Table 13. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Min.	Max.	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5	4.0	V
Input Voltage, Maximum	Any input pin	–	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	–	V
Storage Temperature		-65	150	°C
Maximum Junction Temperature		–	130	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		–	260	°C

Table 14. Thermal Considerations^[3]

Package	θ_{JA} , 4 Layer Board (°C/W)	θ_{JC} , Bottom (°C/W)
3225, 6-pin	TBD	TBD

Notes:

3. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 15. Maximum Operating Junction Temperature^[4]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	TBD
85°C	TBD
95°C	TBD
105°C	TBD

Notes:

4. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 16. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	g
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Pin Description

Table 17. Pin Description

Pin	Map	Functionality	
1	OE/NF	Output Enable (OE)	H ^[5] Specified frequency output L: OUTP (OUTN) held at logic high (low)
		No Function (NF)	H or L or Open: No effect on output frequency or other device functions.
2	NF	No Function	H or L or Open: No effect on output frequency or other device functions
3	GND	Power	VDD Power Supply Ground
4	OUTP	Output	Oscillator output
5	OUTN	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage ^[6]

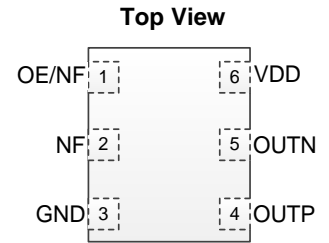


Figure 3. Pin Assignments

Notes:

- 5. OE pin includes a 120 kΩ internal pull-up resistor to VDD when active high, and a 120 kΩ internal pull-down resistor to GND when active low. In noisy environments, OE pin that is active high or active low are recommended to include an external pull-up or pull-down resistor, respectively, of 10 kΩ when the pin is not externally driven.
- 6. A capacitor of value 0.1 μF or higher between VDD and GND pins is required.

FlexSwing Configurations

A FlexSwing output-driver performs like LVPECL but provides independent control of voltage swing and DC offset voltage levels. This simplifies interfacing with chipsets having non-standard input voltage requirements

and can eliminate all external source-bias resistors. FlexSwing supports power supply voltages from 1.71 V to 3.63 V, and the programmable VOH and VOL levels may be referenced to the voltage on either VDD or GND pins.

Table 18. FlexSwing 2-digit Order Codes specifying VHn and VLn referenced to voltage on VDD pin

Order Code V_Swing (V)		VLn																														
		A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X									
		Vdd-2.35V	Vdd-2.30V	Vdd-2.25V	Vdd-2.20V	Vdd-2.15V	Vdd-2.10V	Vdd-2.05V	Vdd-2.00V	Vdd-1.95V	Vdd-1.90V	Vdd-1.85V	Vdd-1.80V	Vdd-1.75V	Vdd-1.70V	Vdd-1.65V	Vdd-1.60V	Vdd-1.55V	Vdd-1.50V	Vdd-1.45V	Vdd-1.40V	Vdd-1.35V	Vdd-1.30V									
VHn	A Vdd-0.80V	Supply Voltage				Available Colors																										
	B Vdd-0.85V	1.8V±5%				Not Supported																										
	C Vdd-0.90V	1.71V to 3.63V				Not Supported																										
	D Vdd-0.95V	2.5V±10%				Blue																										
		3.3V±10%				Blue Red																										
	E Vdd-1.00V	2.25V to 3.63V				Blue																										
																EK	EL	EM	EN	EP	EQ	ER	ES	ET	EU	EV	EW	EX				
	F Vdd-1.05V															FJ	FK	FL	FM	FN	FP	FQ	FR	FS	FT	FU	FV	FW	FX			
	G Vdd-1.10V															GH	GJ	GK	GL	GM	GN	GP	GQ	GR	GS	GT	GU	GV	GW	GX		
	H Vdd-1.15V															HG	HH	HJ	HK	HL	HM	HN	HP	HQ	HR	HS	HT	HU	HV	HW	HX	
	J Vdd-1.20V															JF	JG	JH	JJ	JK	JL	JM	JN	JP	JQ	JR	JS	JT	JU	JV	JW	JX
	K Vdd-1.25V															KE	KF	KG	KH	KJ	KK	KL	KM	KN	KP	KQ	KR	KS	KT	KU	KV	KW
	L Vdd-1.30V															LD	LE	LF	LG	LH	LJ	LK	LL	LM	LN	LP	LQ	LR	LS	LT	LU	LV
	M Vdd-1.35V															MC	MD	ME	MF	MG	MH	MJ	MK	ML	MM	MN	MP	MQ	MR	MS	MT	MU
	N Vdd-1.40V															NB	NC	ND	NE	NF	NG	NH	NJ	NK	NL	NM	NN	NP	NQ	NR	NS	NT
	P Vdd-1.45V	PA	PB	PC	PD	PE	PF	PG	PH	PJ	PK	PL	PM	PN	PP	PQ	PR	PS														
	Q Vdd-1.50V	QA	QB	QC	QD	QE	QF	QG	QH	QJ	QK	QL	QM	QN	QP	QR																
	R Vdd-1.55V	RA	RB	RC	RD	RE	RF	RG	RH	RJ	RK	RL	RM	RN	RP	RQ																
	S Vdd-1.60V	SA	SB	SC	SD	SE	SF	SG	SH	SJ	SK	SL	SM	SN	SP																	
T Vdd-1.65V	TA	TB	TC	TD	TE	TF	TG	TH	TJ	TK	TL	TM	TN																			
U Vdd-1.70V	UA	UB	UC	UD	UE	UF	UG	UH	UJ	UK	UL	UM																				
V Vdd-1.75V	VA	VB	VC	VD	VE	VF	VG	VH	VJ	VK	VL																					
W Vdd-1.80V	WA	WB	WC	WD	WE	WF	WG	WH	WJ	WK																						

The above table identifies supported combinations of nominal VOH (i.e. VHn) and nominal VOL (i.e. VLn) in colored boxes. The two-character code in each box corresponds to the VHn and VLn codes specified in the 2nd column and 2nd row in the table, respectively. The number in each box indicates the nominal differential swing (i.e. VHn – VLn).

(2.25 V to 3.63 V). Alternatively, an order code of “GS” corresponds to a VHn code “G” (i.e. Vdd-1.10 V) and a VLn order code “S” (e.g. Vdd-1.55 V) corresponding to a V_Swing of 0.9 V peak-peak, which may be used for a supply voltage of 3.3 V ±10%.

For example, order code “FS” selects VHn code “F” (i.e. Vdd-1.05 V) and VLn code “S” (i.e. Vdd-1.55 V) corresponding to a V_Swing of 1 V peak-peak, which may be used for supply voltages of 2.5 V ±10%, 3.3 V ±10% or

Waveform Diagrams

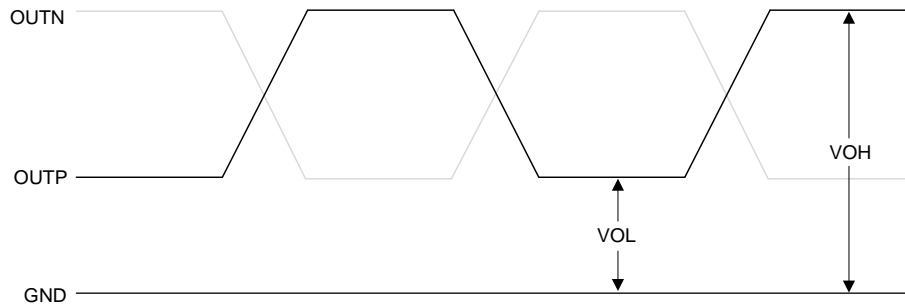


Figure 4. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels per Differential Pin

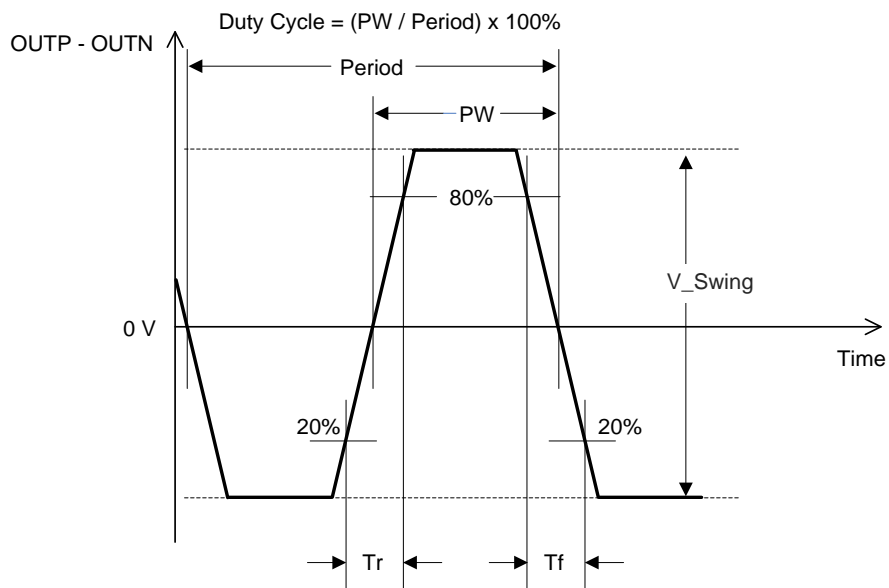


Figure 5. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels Across Differential Pair

Waveform Diagrams (continued)

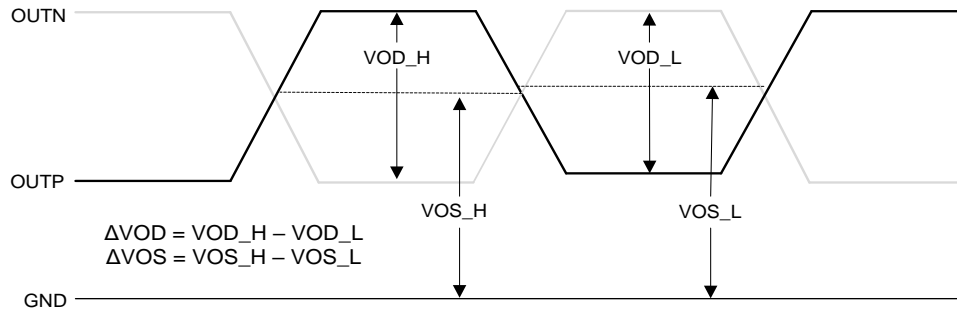


Figure 6. LVDS Voltage Levels per Differential Pin

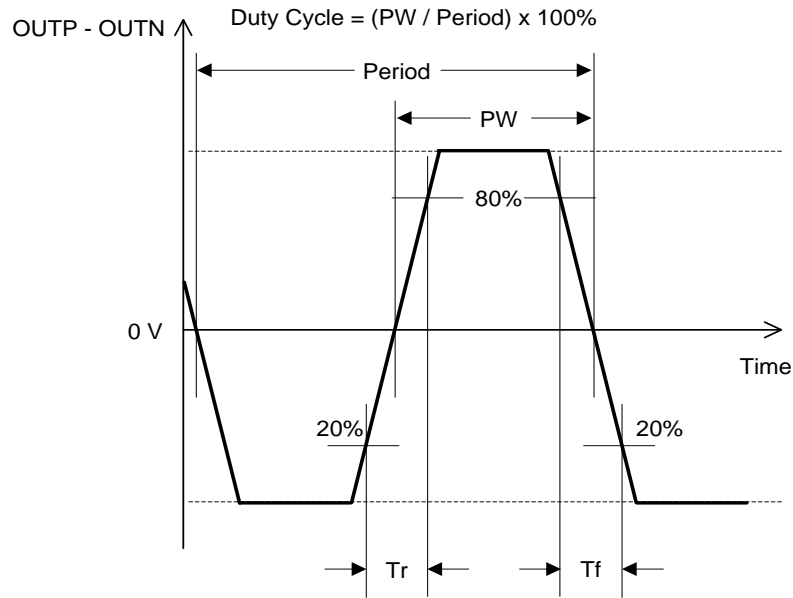


Figure 7. LVDS Differential Waveform

Waveform Diagrams (continued)

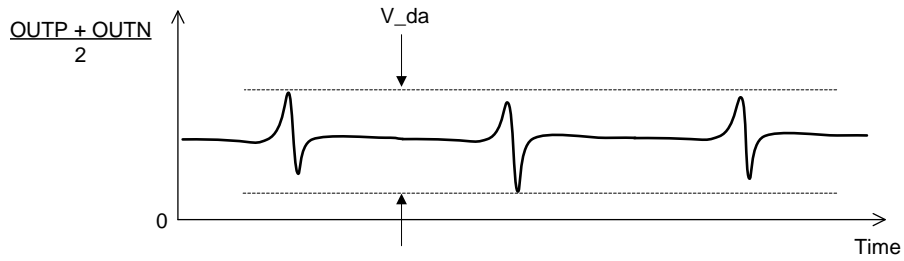


Figure 8. Differential Asymmetry (V_{da})

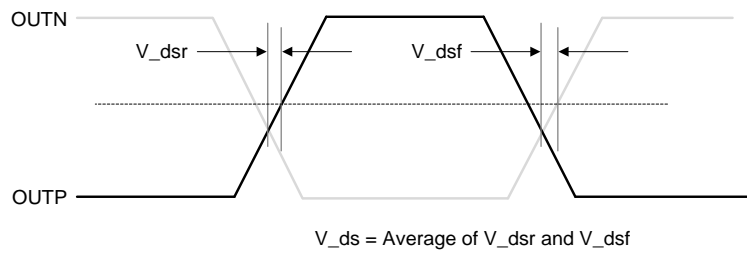


Figure 9. Differential Skew (V_{ds}) is measured as the Time between the Average Voltage Level and Crossing Voltage

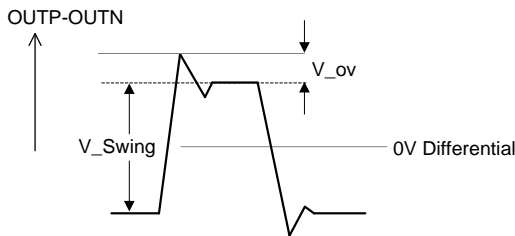


Figure 10. Overshoot Voltage (V_{ov}) for LVPECL, FlexSwing, HCSL, Low-power HCSL

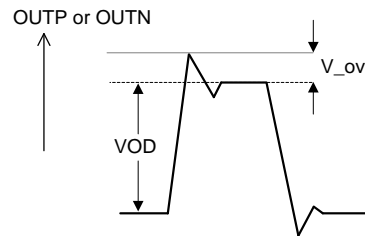


Figure 11. Overshoot Voltage (V_{ov}) for LVDS Output

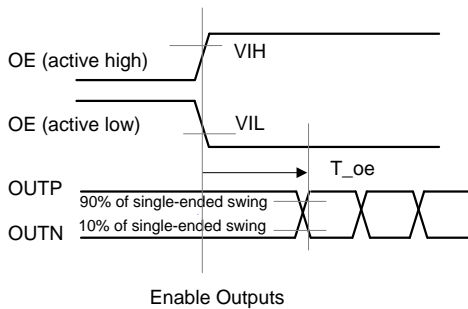


Figure 12. OE Pin Enable Timing (T_{oe})

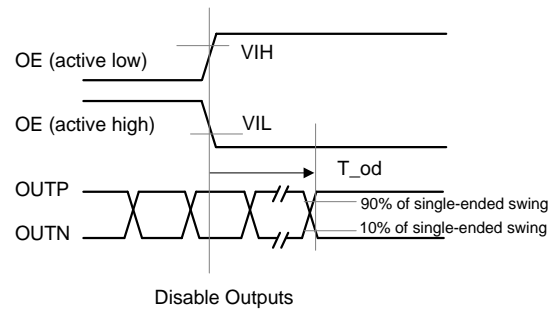


Figure 13. OE Pin Disable Timing (T_{od})

Termination Diagrams

LVPECL and FlexSwing Termination

The SiT9375 output drivers include special features for supporting low-load current without sacrificing signal integrity via simple terminations as shown in Figure 15 and Figure 17. This allows very low power consumption compared to traditional LVPECL drivers. The FlexSwing

and LVPECL outputs are voltage-mode drivers. Use the table and figures below to select a termination circuit for the desired supply voltage. The table also provides LVPECL current consumption (I_{load}) into the load termination.

Table 20. Termination Options for LVPECL and FlexSwing Signaling

Signaling	Supply Voltage, Vdd	Termination Options					
		Figure 14	Figure 15	Figure 16	Figure 17	Figure 18	Figure 19
LVPECL referenced to Vdd	2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V	OK to use	Do Not Use	OK to use $I_{load} = 28$ mA	OK to use	OK to use $I_{load} = 28$ mA	Do Not Use
FlexSwing referenced to Vdd		OK to use ⁷	OK to use (See Figure 15 for frequency ranges and voltage swings)	OK to use ⁷	OK to use	OK to use	Do Not Use
FlexSwing referenced to Gnd	1.71 V to 3.63 V	OK to use ⁷	OK to use (See Figure 15 for frequency ranges and voltage swings)	Do Not Use	OK to use	Do Not Use	Do Not Use
	1.8 V \pm 5%			Do Not Use	OK to use	Do Not Use	OK to use

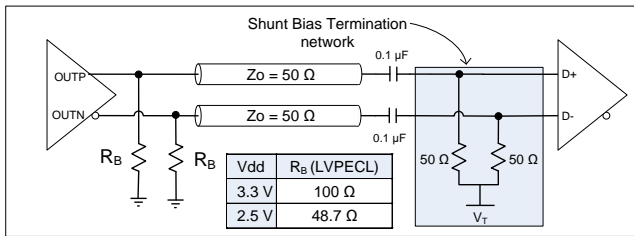


Figure 14. Recommended LVPECL and FlexSwing⁸ Termination when AC-coupled

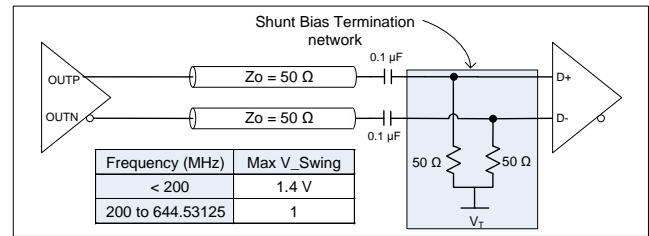


Figure 15. Recommended FlexSwing Termination when AC-coupled

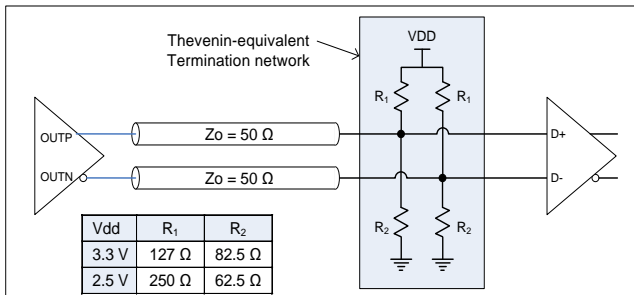


Figure 16. LVPECL and FlexSwing DC-coupled Load Termination with Thevenin Equivalent Network

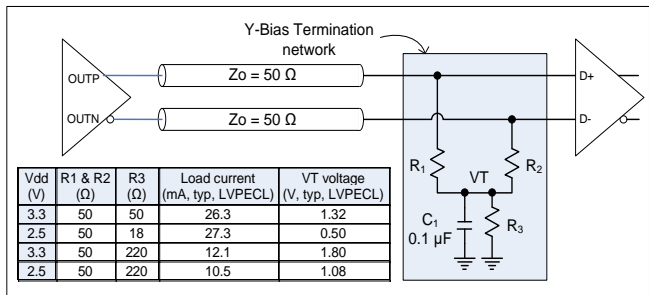


Figure 17. LVPECL and FlexSwing with DC-coupled Parallel Shunt Load Termination

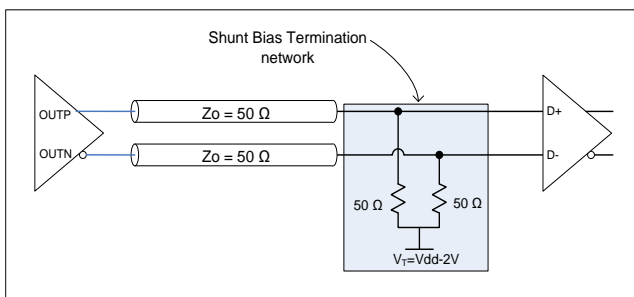


Figure 18. LVPECL and FlexSwing with Y-Bias Termination

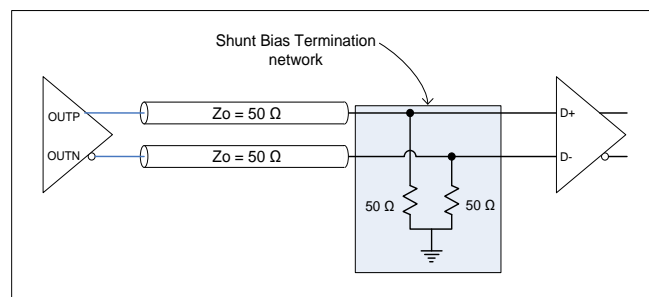


Figure 19. FlexSwing Termination - Only for use with Supply Voltage Order Code "18"

Termination Diagrams (continued)

LVDS, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

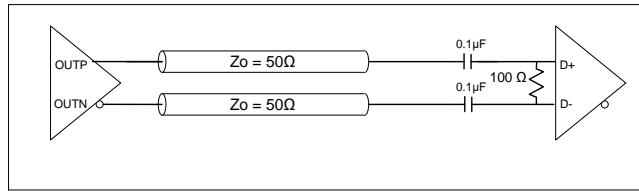


Figure 20. LVDS AC Termination

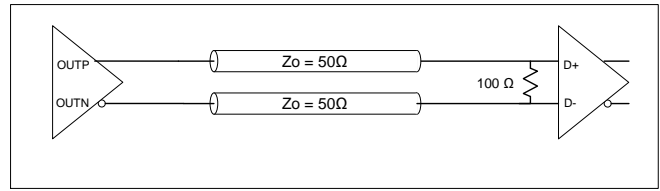


Figure 21. LVDS DC Termination at the Load

HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

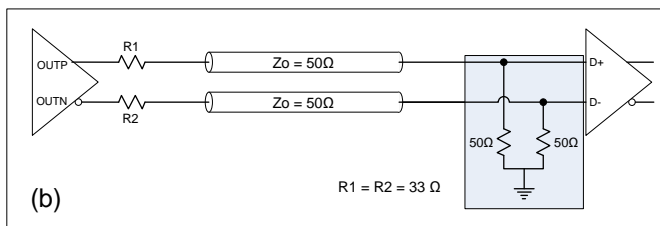
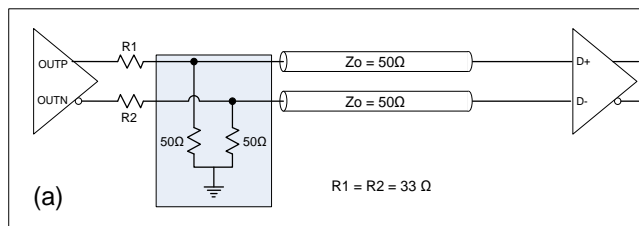


Figure 22. (a) HCSL Source Termination and (b) HCSL Load Termination

Low-power HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

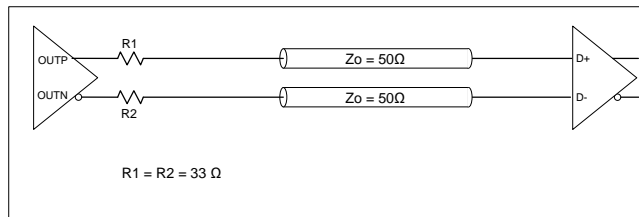


Figure 23. Low-power HCSL Termination

Notes:

- 7. Contact SiTime for optimum R1 and R2 values for FlexSwing options.
- 8. Contact SiTime for optimum Rs values for FlexSwing options.

Dimensions and Patterns — 2.0 x 1.6 mm x mm

Package Size – Dimensions (Unit: mm)^[9]

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.700	0.750	0.800
STAND OFF	A1	0.000	0.035	0.050
BODY SIZE	X	D		
	Y	E		
LEAD WIDTH	b	0.225	0.275	0.325
LEAD LENGTH	L	0.324 REF		
	L1	0.300	0.400	0.500
LEAD PITCH	e	0.730 BSC		
PACKAGE TOLERANCE	aaa	0.100		
MOLD FLATNESS	bbb	0.100		
COPLANARITY	ccc	0.080		

NOTE
1. ALL DIMENSION IN MM

SiTime	
PKG INFO	DRAWING NO.
6L PQFD 2.000x1.600X0.750 mm	POD-077-PQFN-006-C02016
DATE	REV
2020/6/1	A01
	SHEET
	01

Recommended Land Pattern (Unit: mm)^[10]

Note : All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.	
	DATE	6L PQFN 2.000x1.600 mm	SPL-077-PQFN-006-C02016
	2020/04/20	REV	SHEET
		A00	01

Notes:

9. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
10. A capacitor of value 0.1 μ F or higher between VDD and GND is required. An additional 10 μ F capacitor between VDD and GND is required for the best phase jitter performance.

Dimensions and Patterns — 2.5 x 2.0 mm x mm

Package Size – Dimensions (Unit: mm)^[9]

(TOP VIEW)

(BOTTOM VIEW)

(SIDE VIEW)

SEATING PLAN

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.800	0.850	0.900
STAND OFF	A1	0.000	0.035	0.050
BODY SIZE	X	D		
	Y	E		
LEAD WIDTH	b	0.330	0.380	0.430
LEAD LENGTH	L	0.572 REF		
	L1	0.550	0.650	0.750
LEAD PITCH	e	0.900 BSC		
PACKAGE TOLERANCE	aaa	0.100		
MOLD FLATNESS	bbb	0.100		
COPLANARITY	ccc	0.080		
HALF CUT WIDTH	R	0.075	---	---
HALF CUT DEPTH	A3	---	---	0.075
NOTE				
1. ALL DIMENSION IN MM				

PKG INFO		DRAWING NO.	
6L PQFD 2.500x2.000X0.850 mm		POD-078-PQFW-006-C02520	
DATE	2020/6/1	REV	SHEET
		A01	01

Recommended Land Pattern (Unit: mm)^[10]

Note : All units in mm.

DATE	2020/04/20
------	------------

PKG INFO		SPL DRAWING NO.	
6L PQFW 2.500x2.000 mm		SPL-078-PQFW-006-C02520	
REV	A00	SHEET	01

SPL DRAWING NO.	
SPL-078-PQFW-006-C02520	
REV	SHEET
A00	01

Dimensions and Patterns — 3.2 x 2.0 mm x mm

Package Size – Dimensions (Unit: mm)^[9]

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.800	0.850	0.900
STAND OFF	A1	0.000	0.035	0.050
BODY SIZE	X	D		
	Y	E		
LEAD WIDTH	b	0.550	0.600	0.650
LEAD LENGTH	L	0.650	0.700	0.750
	L1	0.800 REF		
LEAD PITCH	e	1.100 BSC		
PACKAGE TOLERANCE	aaa	0.100		
MOLD FLATNESS	bbb	0.100		
COPLANARITY	ccc	0.080		
DIMPLE WIDTH	T	0.150 REF		
DIMPLE LENGTH	P	0.150 REF		
DIMPLE DEPTH	A2	0.100 REF		

NOTE
1. ALL DIMENSION IN MM

SiTime	
PKG INFO	DRAWING NO.
6L PQFD 3.200x2.500X0.850 mm	POD-076-PQFD-006-C03225
DATE	REV
2020/6/1	A02
	SHEET
	01

Recommended Land Pattern (Unit: mm)^[10]

Note : All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.	
	DATE	SPL-076-PQFD-006-C03225	
2020/04/20	6L PQFD 3.200x2.500 mm	REV	SHEET
		A01	01

Additional Information

Table 21. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library?filter=531
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes
Evaluation Boards	SiT6760EB	TBD

Revision History

Table 22. Revision History

Revision	Release Date	Change Summary
0.5	05/22/2020	Advanced datasheet
0.51	06/01/2020	Formatting changes Updated package drawings
0.52	07/28/2020	Extended frequency to 644.53125 MHz
0.53	08/02/2020	Modified Termination Diagrams section

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