SiT92315
20 Output DB2000QL Equivalent with 85 Ω Terminations

Description

The SiT92315 is a HCSL-LP, 20 Output differential Fan-Out buffer that meets or exceeds all the performance requirements of the Intel DB2000QL specification. They are suitable for PCI-Express Gen 1-6 or QP/UPI applications.

SiT92315 offers three modes to control all the 20 outputs. We can control the outputs either through the SMBus interface or the Side Band Interface or Output Enable pins.

It is packaged in a compact LGA package and uses a standard pin configuration.

Nomenclature

SiT92315: 20 Output, 80 Pin, 6 mm x 6 mm

Applications

- Micro-server and Tower Server
- Rack server
- Storage area network and host bus adapter card
- Network attached storage
- SSDs

Features

- HCSL-LP outputs with Zo = 85 Ω.
- Saves power and board space - no termination resistors required.
- Supports PCIe and QPI applications.
- Spread spectrum compatible; tracks spreading input clock for low EMI.
- Additive phase jitter.
- Fclk=100 MHz (10k-20M) band ~ 42fs (Typical)
- Fclk=100 MHz after PCIE Gen5 (CC) filter ~10 fs RMS
- Fclk=100 MHz after PCIE Gen6 filter ~6 fs RMS
- Additive phase jitter after DB2000Q filter ~8 fs RMS (typical)
- Programmable output slew rate control.
- Output to Output Skew < 50 ps.
- 3.3 V core and IO supply voltages.
- Hardware-controlled low power mode (PDN)
- Current consumption : 150 mA Typical with all 20 outputs enabled at 100 MHz, driving a 10 inch T line and 2pF load on each output.

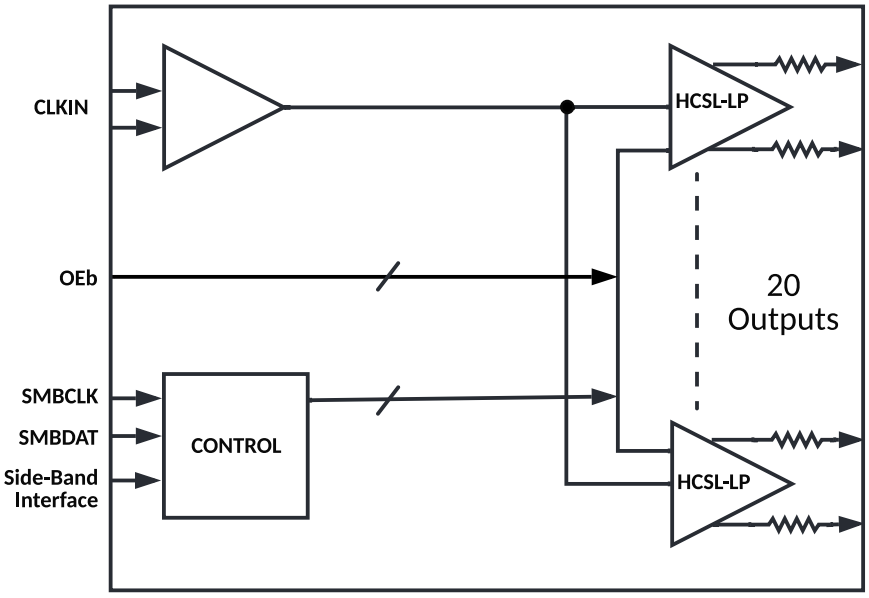

Figure 1. SiT92315 Functional Overview

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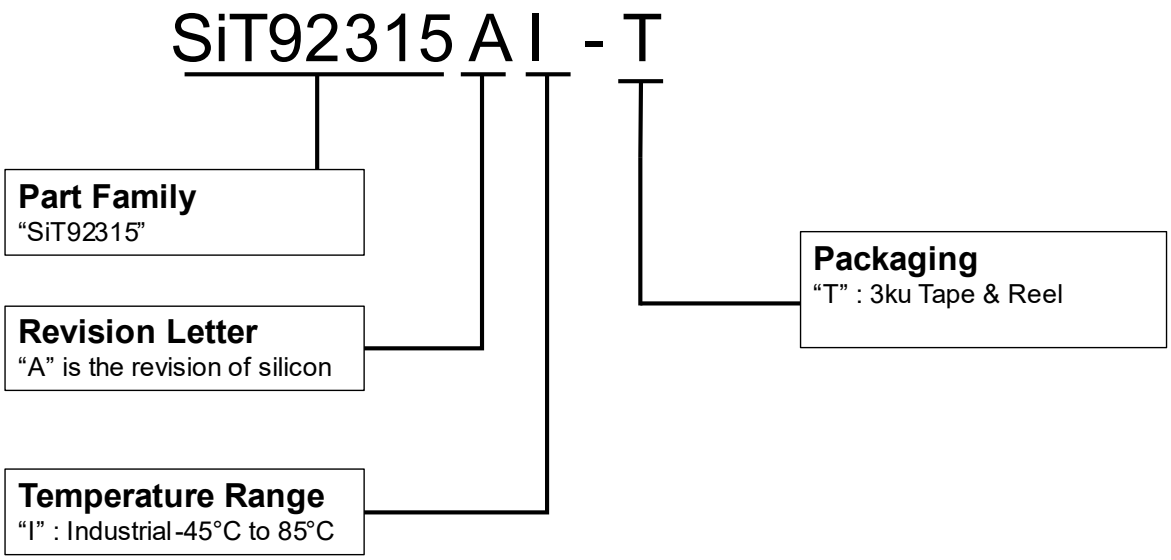
Ordering Information



Electrical Characteristics

Table 1. Absolute Maximum Ratings

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Supply Voltage	Input Supply Core Supply	VDDIN VDD			**3.63**	V
Output Bank Supply Voltage	Output Driver Supply	VDDO			**3.63**	V
Input Low Voltage		VIL	GND-0.5			V
Input High Voltage	Except for SMBus interface	VIH			VDD+0.5	V
Input High Voltage	SMBus clock and data pins	VIHSMB			3.6	V
Storage Temperature		Ts	-65		150	°C
Junction Temperature		Tj			125	°C
ESD (Human Body Model)	JESD22A-114	ESD_{HBM}			2000	V
ESD(Charge Device Model)		ESD_{CDM}			500	V
Latch Up	JEDEC JESD78D	LU			100	mA
Moisture Sensitivity Level		MSL		3		

Notes:

1. Exceeding maximum ratings may shorten the useful life of the device.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 2. Recommended Operating Conditions

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Supply Voltage		VDDIN	2.97	3.3	3.465	V
Core Supply Voltage		VDD	2.97	3.3	3.465	V
Output Supply Voltage		VDDO	2.97	3.3	3.465	V
Output Supply Voltage [bypass mode]		VDDO	0.95		1.05	V
Ambient Temperature		T_A	-40		85	°C
Junction Temperature		T_j			125	°C

Table 3 Electrical Characteristics.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Supply Current	Input Supply Current	IDD_{VDDIN}		6.6		mA
	Core Supply Current	IDD_{VDD}		20		mA
Additive Output Supply Current	All Outputs Enabled, driving a 10in T-line terminated with 2 pF cap at 100 MHz clock	IDD_{VDDO}		120		
Power Down Current	Input Supply Current	IDD_{VDDIN}		1		
	Core Supply Current	IDD_{VDD}		2		mA
	Output Driver Supply Current	IDD_{VDDO}		1		mA
Input Control Pin Characteristics						
Input High Current	VDDIN = 3.3V, VIH = VDDIN	IIH			20	µA
Input Low Current		IIL	-0.5			µA
Input high voltage – Logic inputs		VIH	0.7×VDDIN			V

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input low voltage – Logic inputs		VIL			0.3×VDDIN	V
Internal Pull-down resistance		$R_{Pulldown}$		200		K Ω
Pin Inductance[1]		L_{PIN}			7	nH
Capacitance[1,2]	Logic Inputs, except DIF_IN.	C_{IN}			4.5	pF
	DIF_IN differential clock inputs	C_{INDIF_IN}			2.7	pF
	Output pin capacitance	C_{OUT}			4.5	

Notes:

1. Guaranteed by design and characterization, not 100% tested in production.
2. DIF_IN input

Table 4 Input Clock Characteristics

Unless otherwise specified: VDD = 3.3 V ± 5%, VDDO = 3.3 V ± 5%, -40 °C ≤ TA ≤ 85 °C, CLKin driven differentially

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input frequency range		F_{CLKin}	1		400M	Hz
Peak differential input voltage swing		VID	0.1			V
Input Slew Rate - CLKin	Measured differentially	dv/dt	0.2		4	V/ns
Input Leakage Current	VIN = VDD, VIN = GND	IIN	-5		5	uA
Input Duty Cycle	Measurement from differential waveform	dtin		50		%
Input Crossover Voltage	Crossover voltage		0.1		0.9	V

Table 5 Output Clock Characteristics – HCSL-LP at 100 MHz

$T_A = T_{COM}$; Supply Voltage VDD = 3.3 V +/-5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Slew rate	Scope averaging on	T_{rf}	2		4	V/ns
Slew rate matching	Slew rate matching, Scope averaging on	ΔT_{rf}			20	%
Voltage High	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	V_{High}		750		mV
Voltage Low		V_{Low}		0		mV
Max Voltage	Measurement on single ended signal using absolute value. (Scope averaging off)	V_{max}				
Min Voltage		V_{min}				
Vswing	Scope averaging off	V_{SWING}				
Crossing Voltage (abs)	Scope averaging off	V_{cross_abs}		375		mV
Crossing Voltage (var)	Scope averaging off	Δ-Vcross				
Clock Stabilization[1,2]	From VDD power-up and after input clock stabilization or de-assertion of PDb to 1st Clock	T_{STAB}		0.11	0.5	ms
OEb Latency[1,2,3]	DIF starts after OEb assertion DIF stop after OEb de-assertion	t_{LATOEb}	2		3	Clocks

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Tdrive_PDb[1,3]	DIF output enable after CKPWRGD_PDN assertion	t_{DRVPDb}		76	300	µs
T_{FALL}[2]	Fall time of control inputs	t_F			5	ns
T_{RISE}[2]	Rise time of control inputs	t_R			5	ns
Output high voltage	Single ended, measured into DC test load	V_{OH}	225		270	mV
Output low voltage	Single ended, measured into DC test load	V_{OL}	10		120	mV
Over shoot voltage	Single ended, measured into DC test load	V_{OVS}			V_{OH}+75	mV
Under shoot voltage	Single ended, measured into DC test load	V_{UDS}			V_{OL}-75	mV
Differential Impedance[4]		Z_{DIFF}	85-5%	85	85+5%	Ω
Differential Impedance (crossing)[5]		Z_{DIFF_CROSS}	85-20%	85	85+20%	Ω

Notes :
1. Guaranteed by design and characterization, not 100% tested in production.
2. Control input must be monotonic from 20% to 80% of input swing.
3. Time from deassertion until outputs are > 200mV.
4. Measured at V_{OH}/V_{OL}
5. Measured at transition

Table 6 SMbus Electrical Parameters

$T_A = T_{AMB}$. Supply voltages are per normal conditions. See Test loads for loading conditions.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
SMBus Input Low Voltage		V_{ILSMB}			0.8	V
SMBus Input High Voltage		V_{IHSMB}	2.1		VDD_{SMB}	V
SMBus Output Low Voltage	At I_{PULLUP}	V_{OLSMB}			0.4	V
SMBus Sink Current	At V_{OL}	I_{PULLUP}	4			mA
Nominal Bus Voltage		VDD_{SMB}	2.7		3.6	V

Table 7 Skew and Differential Jitter Parameters

Parameter	Conditions	Symbol	Min	Typ	Max	Units
CLKINx, CLKOUTx[1,2,4,5,6,7]	Input-to-Output Skew in nominal value @ 25°C, 3.3V	t_{PD}	0.6	0.75	1.1	ns
CLKINx, CLKOUTx [1,2,6,7,8]	Input-to-Output Skew Variation across temperatures	T_{PD_DRIFT}			2	ps/°C
DIF[2,5,6,7]	Output-to-Output Skew across all outputs	t_{SKEW_ALL}			50	ps
Duty Cycle Distortion [3,5,6]	Measured differentially, @100MHz	t_{DCD}	-1		1	%

Notes:
1. Guaranteed by design and characterization, not 100% tested in production.
2. Differential cross-point to differential cross-point measurement.
3. The difference in Duty Cycle between the output and input clock is referred as Duty Cycle Distortion
4. Mean Value measured through scope averaging.
5. Measured from differential waveform.

6. Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
7. All input-to-output specs refer to the timing between an input edge and the specific output edge created by it.
8. This is the amount of input-to-output delay variation with respect to temperature.

Table 8 Phase Jitter Parameters-PCIe Common Clocked(CC) Architecture

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Additive Phase Jitter	PCIe Gen 1 HF [1,2,3,4]	$tjph_{PCIeG1-CC}$		0.100		ps (p-p)
	PCIe Gen 2 HF [1,2,3,4]	$tjph_{PCIeG2-CC}$		0.080		ps rms
	PCIe Gen 3[1,2,3]	$tjph_{PCIeG3-CC}$		0.023		ps rms
	PCIe Gen4[1,2,3]	$tjph_{PCIeG4-CC}$		0.023		ps rms
	PCIe Gen5[1,2,3]	$tjph_{PCIeG5-CC}$		0.009		ps rms
	PCIe Gen6[1,2,3]	$tjph_{PCIeG6-CC}$		0.006		ps rms

Notes:

1. Guaranteed by design and characterization. Applies to all differential outputs.
2. Input to SiT92315 is fed using low phase noise source SMA100B while SiT92315 is configured as 100 MHz LP-HCSL Output Driver and fed to the channels of the DSO through low noise high slew drivers to minimize the impact of DSO broadband noise.
3. Additive RMS Jitter Measurement for PCIe are made using DSO. Commercially available and popular PCIe jitter post processing tools are used to report PCIe jitter
4. Additive jitter for RMS values is calculated by solving the equation for b [$b = \sqrt{(c^2 - a^2)}$] where 'a' is the rms input jitter and "c" is the rms total jitter.

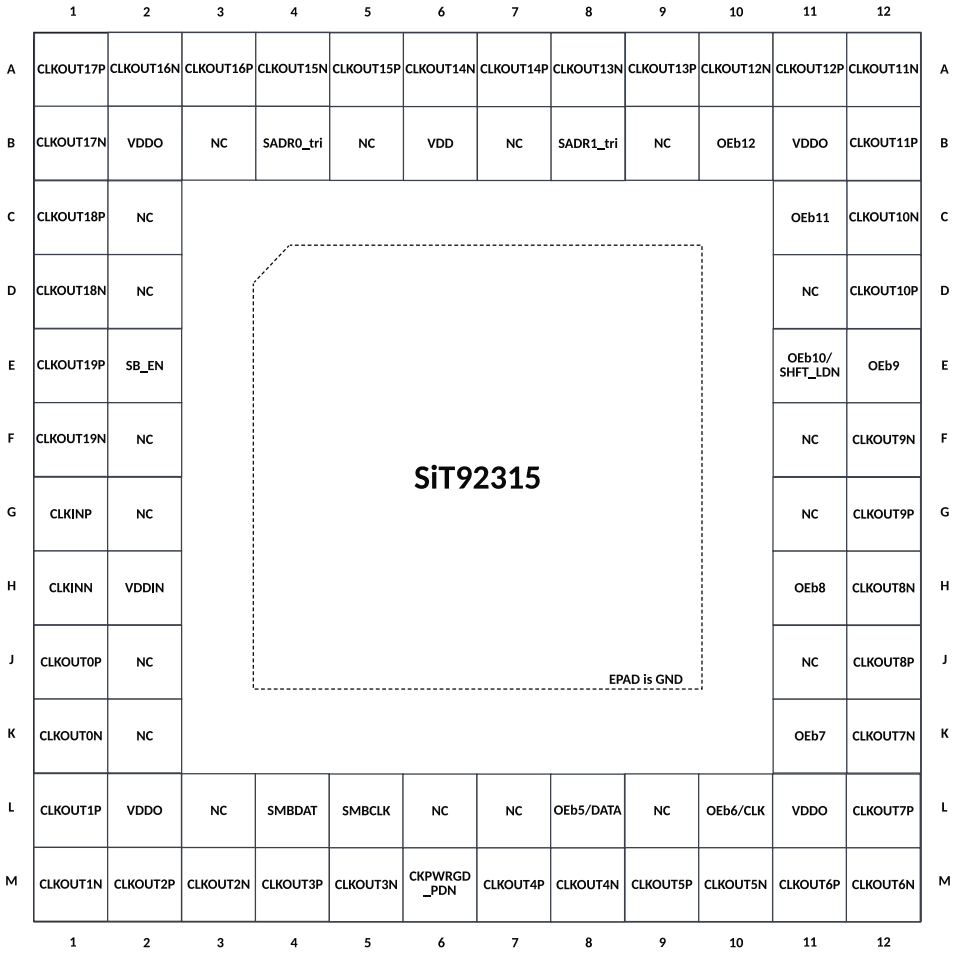


Figure 2. SiT92315 Top View

Table 9. Detailed Pin Description

Pin Name	Pin No.	I/O Type	Description
VDDO	B2, B11, L2, L11	PWR	Power Supply for the Output Drivers, nominal 3.3 V
VDD	B6	PWR	3.3 V power for the analog Core.
VDDIN	H2	PWR	3.3 V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.
SADR0_tri	B4	I, PU/PD	SMBUS address strap pin. There is a 3 level input decoding on this pad. It has a pull-up/pull-down resistors to bias to VDD/2.
SB_EN	E2	I, PD	When asserted, this pin disables the output enable pins ceding control of the output enables to the Side-Band Interface pin(E11). It has a internal pull-down resistor. 0 = OE pins and SMBus enable bits controls OE pins; Side-Band interface disabled 1 = Side-Band Interface controls OE pins; OE pins and SMBus enable bits disabled
SMBDAT	L4	I/O	Data pin of SMBUS circuitry, 3.3 V tolerant
SMBCLK	L5	I/O	Clock pin of SMBUS circuitry, 3.3 V tolerant

Pin Name	Pin No.	I/O Type	Description
SADR1_tri	B8	I, PU/PD	SMBUS address strap pin. There is a 3 level input decoding on this pad. It has a pull-up/pull-down resistors to bias to VDD/2
CLKINP	G1	I	0.75 V differential true input
CLKINN	H1	I	0.75 V differential complementary Input
CLKOUT0P	J1	O	0.75 V differential true clock output
CLKOUT0N	K1	O	0.75 V differential complementary clock output
CLKOUT1P	L1	O	0.75 V differential true clock output
CLKOUT1N	M1	O	0.75 V differential complementary clock output
CLKOUT2P	M2	O	0.75 V differential true clock output
CLKOUT2N	M3	O	0.75 V differential complementary clock output
CLKOUT3P	M4	O	0.75 V differential true clock output
CLKOUT3N	M5	O	0.75 V differential complementary clock output
CKPWRGD_PDN	M6	I, PD	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down mode, subsequent high assertions exit Power Down mode. This pin has internal pull-down resistor.
CLKOUT4P	M7	O	0.75 V differential true clock output
CLKOUT4N	M8	O	0.75 V differential complementary clock output
CLKOUT5P	M9	O	0.75 V differential true clock output
CLKOUT5N	M10	O	0.75 V differential complementary clock output
OEb5/DATA	L8	I, PD	Active low input for enabling Clock pair 5 when in OE mode and the Data pin when in Side-Band Interface mode. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT6P	M11	O	0.75 V differential true clock output
CLKOUT6N	M12	O	0.75 V differential complementary clock output
OEb6/CLK	L10	I, PD	Active low input for enabling Clock pair 6 when in OE mode and enables Clock pin when in Side-Band Interface mode. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT7P	L12	O	0.75 V differential true clock output
CLKOUT7N	K12	O	0.75 V differential complementary clock output
OEb7	K11	I, PD	Active low input for enabling Clock pair 7. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
CLKOUT8P	J12	O	0.75 V differential true clock output
CLKOUT8N	H12	O	0.75 V differential complementary clock output
OEb8	H11	I, PD	Active low input for enabling Clock pair 8. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
CLKOUT9P	G12	O	0.75 V differential true clock output
CLKOUT9N	F12	O	0.75 V differential complementary clock output
OEb9	E12	I, PD	Active low input for enabling Clock pair 9. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
CLKOUT10P	D12	O	0.75 V differential true clock output
CLKOUT10N	C12	O	0.75 V differential complementary clock output

Pin Name	Pin No.	I/O Type	Description
OEb10/SHFT_LDN	E11	I, PD	Active low input for enabling Clock pair 10 in OE mode or the SHFT_LDN pin in Side-Band Interface mode. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT11P	B12	O	0.75 V differential true clock output
CLKOUT11N	A12	O	0.75 V differential complementary clock output
OEb11	C11	I, PD	Active low input for enabling Clock pair 11. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
CLKOUT12P	A11	O	0.75 V differential true clock output
CLKOUT12N	A10	O	0.75 V differential complementary clock output
OEb12	B10	I, PD	Active low input for enabling Clock pair 12. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT13P	A9	O	0.75 V differential true clock output
CLKOUT13N	A8	O	0.75 V differential complementary clock output
CLKOUT14P	A7	O	0.75 V differential true clock output
CLKOUT14N	A6	O	0.75 V differential complementary clock output
CLKOUT15P	A5	O	0.75 V differential true clock output
CLKOUT15N	A4	O	0.75 V differential complementary clock output
CLKOUT16P	A3	O	0.75 V differential true clock output
CLKOUT16N	A2	O	0.75 V differential complementary clock output
CLKOUT17P	A1	O	0.75 V differential true clock output
CLKOUT17N	B1	O	0.75 V differential complementary clock output
CLKOUT18P	C1	O	0.75 V differential true clock output
CLKOUT18N	D1	O	0.75 V differential complementary clock output
CLKOUT19P	E1	O	0.75 V differential true clock output
CLKOUT19N	F1	O	0.75 V differential complementary clock output
NC	B3, B5, B7, B9, C2, D2, D11, F2, F11, G2, G11, J2, J11, K2, L3, L6, L7, L9,	N/A	No Connection. Recommended to be grounded.
EPAD		GND	Ground

Note:

1. PU is weak Pull Up with 120 kΩ resistor
2. PD is weak Pull Down with 120 kΩ resistor
3. PU/PD is weak Pull Up/Pull down with 120 kΩ resistor

Functional Description

Figure 3 shows a SiT92315 typical application. In this application, a clock generator provides a 100-MHz reference to the SiT92315 which then distributes that clock to PCIe endpoints. The clock generator may either be a discrete clock generator, or it may be integrated in a larger component such as a Platform Controller Hub (PCH) or application processor.

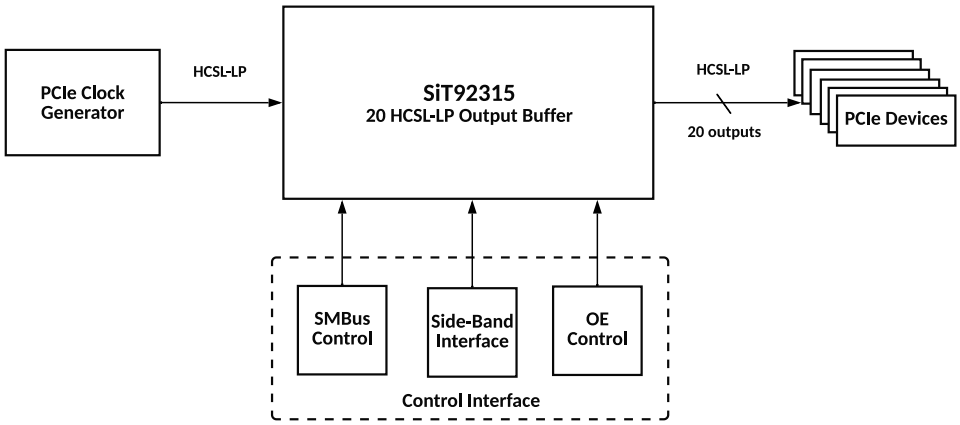


Figure 3 Typical Application Diagram

Parameter Measurement Information

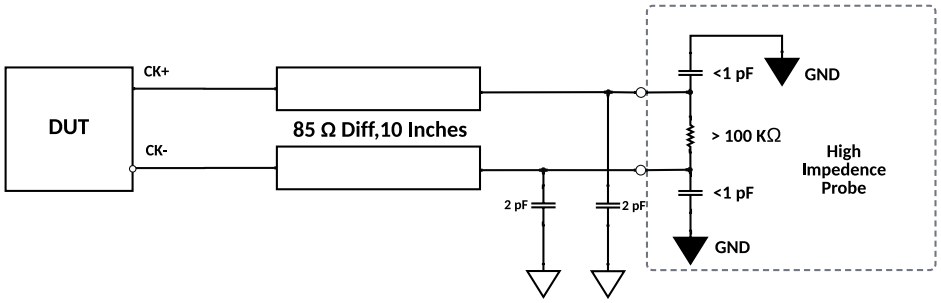


Figure 4 AC Test Mode (Referencing Intel DB2000QL document)

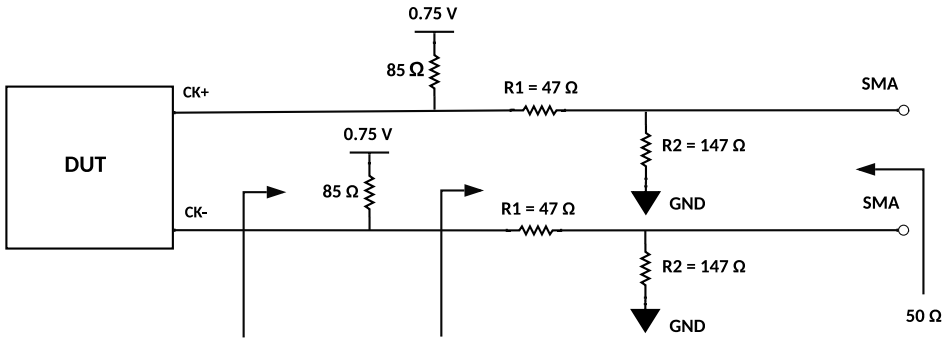


Figure 5 DC Simulation Mode (Referencing Intel DB2000QL Document)

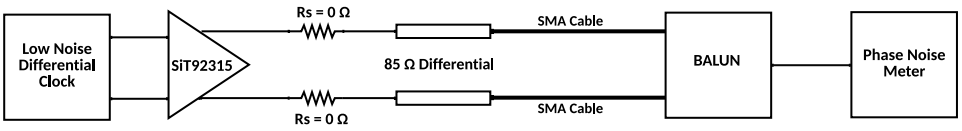


Figure 6 Phase Noise Measurement Setup

Table 10 Output Control SBEN = 0

		Traditional Interface		Side Band interface		Outputs
CKPWRGD_PDN	DIF_IN	OEx bit Byte [2:0]	OExb Pin	MASKx Byte [10:8]	Qx	DIFx
0	X	X	X	X	X	Low/Low
1	Running	0	X	X	X	Low/Low
		1	0	X	X	Running
		1	1	X	X	Low/Low
1	Stopped	1	0	X	X	Stopped
		1	1	X	X	Low/Low

Table 11 Output Control SBEN = 1

		Traditional Interface		Side Band interface		Outputs
CKPWRGD_PDN	DIF_IN	OEx bit Byte [2:0]	OExb Pin	MASKx Byte [10:8]	Qx	DIFx
0	X	X	X	X	X	Low/Low
1	Running	X	X	0	0	Low/Low
		X	X	0	1	Running
		X	X	1	X	Low/Low
1	Stopped	X	X	0	1	Stopped
		X	X	1	X	Stopped

Power Good Assertion and De-assertion

Power Good (CKPWRGD_PDN) is asserted high and de-asserted low. De-assertion of CKPWRGD_PDN (pulling the signal low) is equivalent to indicating a power down condition. CKPWRGD_PDN (assertion) is used by the DB2000QL to sample initial configurations such as SA selections.

After CKPWRGD_PDN has been asserted high for the first time, the pin becomes a PWRDNB (Power Down) pin that can be used to shut off all clocks cleanly and instruct the device to invoke power savings mode. PWRDNB is a completely asynchronous active low input.

When entering power savings mode, PWRDNb should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner. When PWRDNb is de-asserted high, all clocks will start and stop without any abnormal behavior and will meet all AC and DC parameters.

NOTE: The assertion and de-assertion of PWRDNb is asynchronous.

Warning: Disabling of the CLKIN input clock prior to the assertion of PWRDNb is an undefined mode and is not recommended. Operation in this mode may result in glitches.

Power Good De-Assertion

When PWRDNb is sampled low by two consecutive rising edges of CLKINN, all differential outputs must be held Tri-stated on the next CLKINN high to low transition.

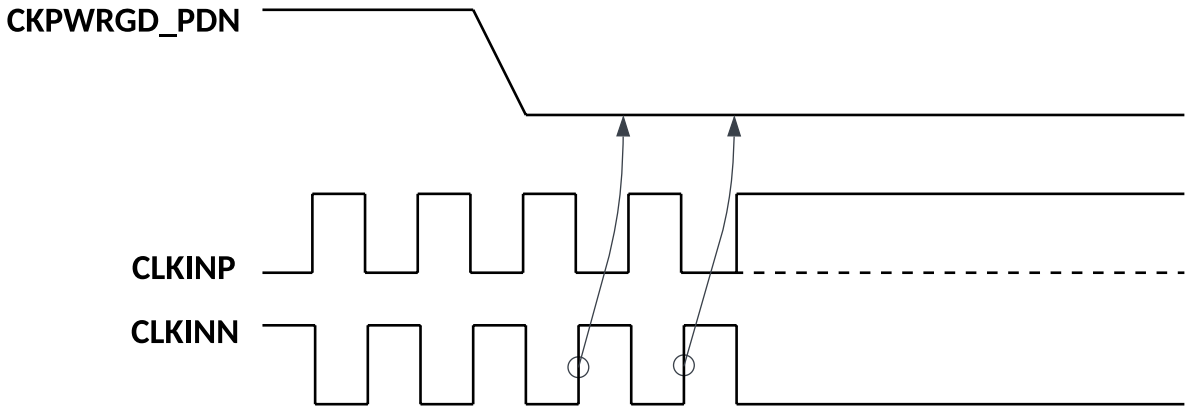


Figure 7 Power Good Assertion

Power Good Assertion

CKPWRGD_PDN must not be asserted to the clock buffer before VDD reaches VDDmin. Prior to VDD_{MIN} it is recommended to hold PWRGD low (less than 0.5V).

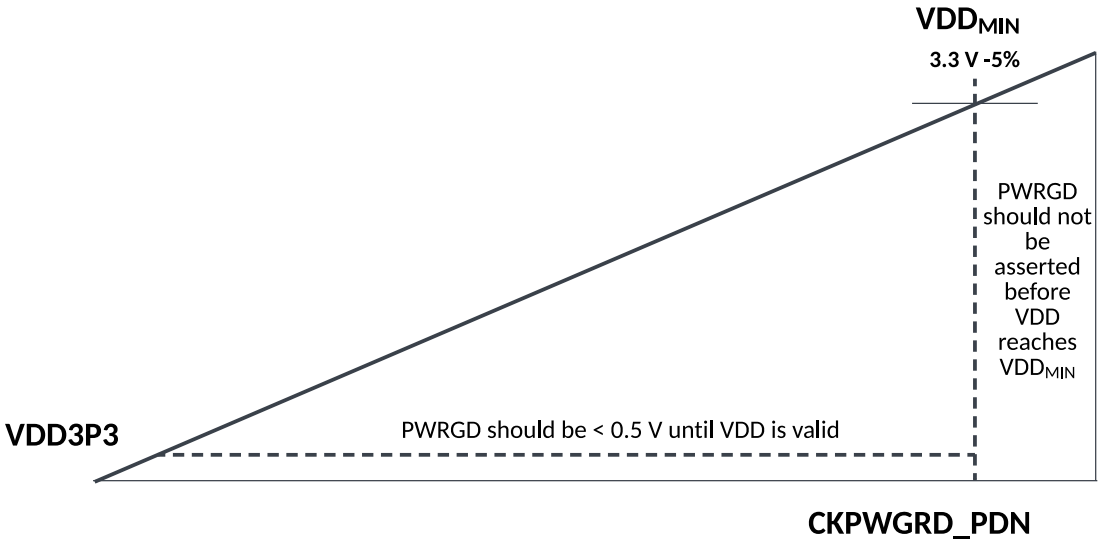


Figure 8 Power Good vs VDD3P3 relationship

The power-up latency in T_{STABLE} is to be less than 1.8 ms. This is the time from the valid CLKINx input and the assertion of the PWRGD signal until the output of the stable clocks from the buffer chip.

All differential outputs stopped in a Tri-state condition resulting from power down must be driven high in less than 300 µs of the PWRGD assertion to a voltage greater than 200 mV.

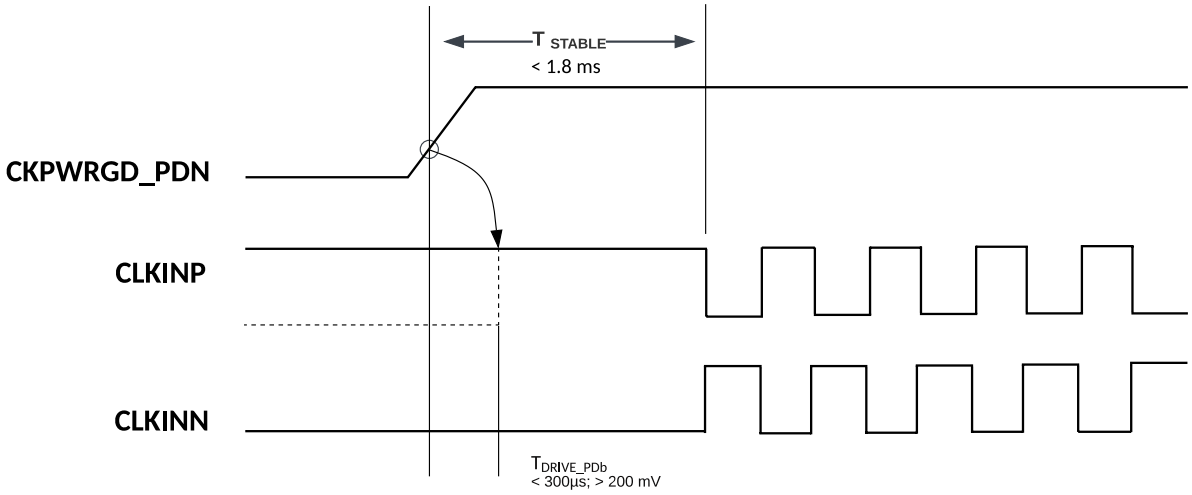


Figure 9 Power Good Assertion

SMBus Parameters

Table 12 SMBus Timing

VDD, VDD_R = 3.3 V ±5%, -40°C ≤ T_A ≤ 105°C. Typical values are at VDD = VDD_A = 3.3 V, 25°C (unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Units
SMBus operating Frequency		f_{SMB}	10		400	kHz
Bus Free time between Stop and Start		t_{BUF}				
Start Condition hold time	SMBCLK low after SMBDAT low	t_{HD_STA}				
Start Condition setup time	SMBCLK high before SMBDAT low	t_{SU_STA}				
Stop Condition setup time		t_{SU_STO}				
SMBDAT hold time		t_{HD_DAT}				
SMBDAT setup time		t_{SU_DAT}				
SMBCLK low timeout detect	Device input clock frequency	$t_{TIMEOUT}$				
SMBCLK low period		t_{LOW}				
SMBCLK high period		t_{HIGH}				
SMBCLK/SMBDAT fall time	Min V_{IH} +0.15 V to Max V_{IL} - 0.15 V	t_F				
SMBCLK/SMBDAT rise time	Max V_{IL} -0.15 V to Min V_{IH} +0.15 V	t_R				

Table 13 SMBus Address Selection

Pin (SADR1_tri, SADR0_tri)	SMBus Address
00	D8
0M	DA
01	DE
M0	C2
MM	C4
M1	C6
10	CA
1M	CC
11	CE

Output Enable Control

Traditional Method

SiT92315 with 20 outputs, has two methods for enabling and disabling outputs. The traditional method of OEb pins and SMBus output enable bits. Outputs 5 through 12 have dedicated output enable pins and each of the 20 outputs have dedicated SMBus output enable bits in Bytes[0:2] of the SMBus register set.

Side-Band Interface

The second method is a simple 3-wire serial interface referred to as the Side-Band Interface (SBI). This interface consists of DATA, CLK and SHFT_LDN pins. When the SHFT_LDN pin is high, the rising edge of CLK can shift DATA into the shift register. After shifting data, the falling edge of SHFT_LDN clocks the shift register contents to the Output register.

Both the SBI and the traditional interface feed common output enable/disable synchronization logic ensuring glitch free enable and disable of outputs, regardless of the method used. Both interfaces are not active at the same time, and the SBEN pin selects which interface is active. Tying the SBEN high enables the SBI.

Tying the SBEN pin low enables the traditional OEb pin/SMBus output enable interface. When the SBI is enabled, OEb[7, 8, 9, 11, 12] are disabled and DATA, CLK and SHFT_LDN are enabled on OE5b, OE6b and OE10b respectively. Additionally, SMBus registers for masking off the disable function of the shift register (0 value of a bit) become active. When set to a one, the mask register forces its respective output to 'enabled'. This prevents accidentally disabling critical outputs when using the SBI.

An SMBus read back bit in Byte 4 indicates which output enable control interface is enabled. When the SBI is enabled, and power has been applied, the SBI is active, even if the CKPWRGD_PDN pin indicates the part is in power down. This allows loading the shift register and transferring the contents to the output register before the assertion of CKPWRGD.

Note that the mask registers are part of the normal SMBus interface and cannot be accessed when the CKPWRGD_PDN is low. The SBI and the traditional SMBus output enable registers both default to the 'output enabled' state at power-up. The mask registers default to zero at power-up, allowing the shift register bits to disable their respective output. Refer Figure 10.

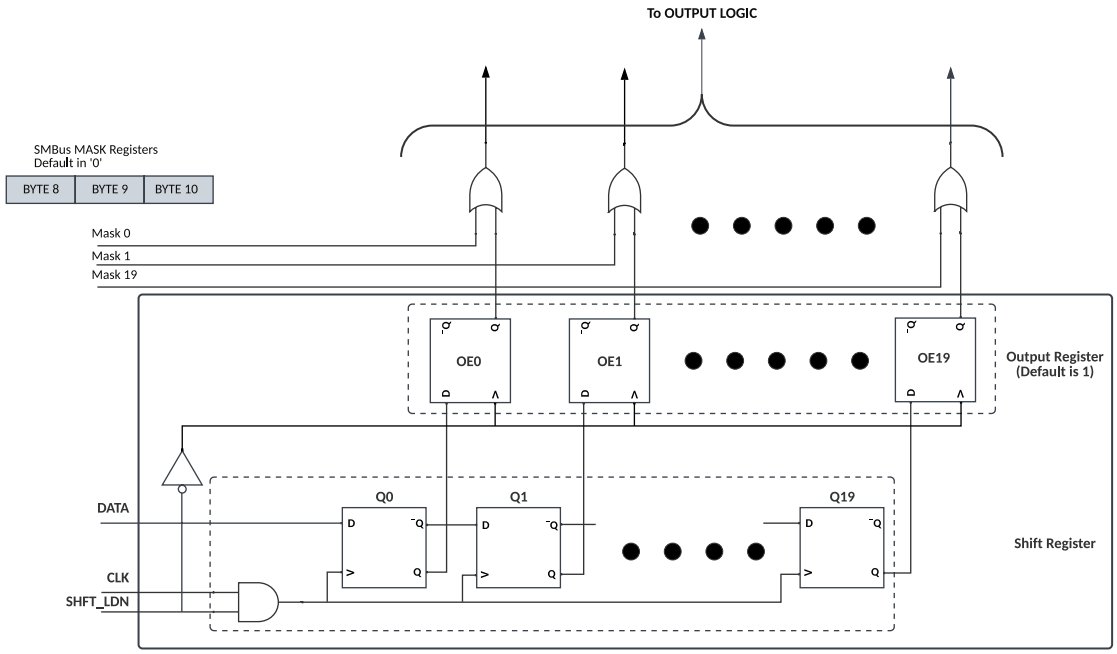


Figure 10 Side Band Interface Control Logic

Figure 11 shows the basic timing of the side-band interface. The SHFT_LDN pin goes high to enable the CLK input. Next, the rising edge of CLK clocks enable DATA into the shift register. After the 20th clock, stop the clock low and drive the SHFT_LDN pin low. The falling edge of SHFT_LDN clocks the shift register contents to the output

register, enabling or disabling the outputs. Always shift 20 bits of data into the shift register to control the outputs.

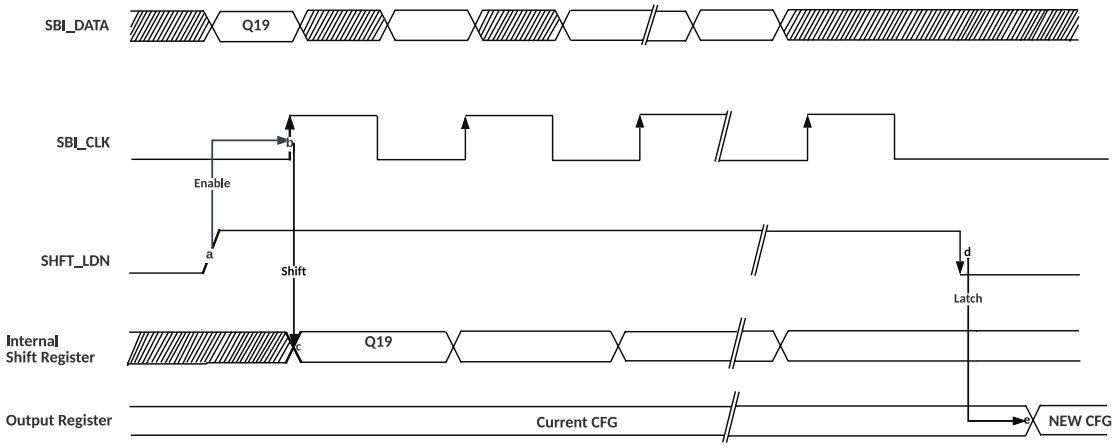


Figure 11 Side Band Interface Functional Timing

The SBI interface supports clock rates up to 25 MHz. Multiple devices may share CLK and DATA pins. Dedicating a SHFT_LDN pin to each devices allows its use as a chip-select pin. When the SHFT_LDN pin is low, the SiT92315 ignores any activity on the CLK and DATA pins.

Register Address

Table 14 Register Map SiT92315

Register Address	Bit Range	Register name	Default	Type	SiT92315 Bit Name	Description and Function
0x00	7	OE_CTRL_0	0	RO	Reserved	Reserved
	6		1	RW	DIF19_ENABLE	Output Enable 0: STOP_STATE Mode 1: OEb Pin Control
	5				DIF18_ENABLE	
	4				DIF17_ENABLE	
	3				DIF16_ENABLE	
	2:0		0	RW	SPARE	Spare
0x01	7	OE_CTRL_1	1	RW	DIF7_ENABLE	Output Enable 0: STOP_STATE Mode 1: OEb Pin Control
	6				DIF6_ENABLE	
	5				DIF5_ENABLE	
	4				DIF4_ENABLE	
	3				DIF3_ENABLE	
	2				DIF2_ENABLE	
	1				DIF1_ENABLE	
	0				DIF0_ENABLE	
0x02	7	OE_CTRL_2	1	RW	DIF15_ENABLE	Output Enable 0: STOP_STATE Mode 1: OEb Pin Control
	6				DIF14_ENABLE	
	5				DIF13_ENABLE	
	4				DIF12_ENABLE	
	3				DIF11_ENABLE	
	2				DIF10_ENABLE	
	1				DIF9_ENABLE	
	0				DIF8_ENABLE	
0x03	7	OE_PIN_READ_BACK	0	RO	RB_OE12	OEb Pin Readback Register
	6				RB_OE11	

Register Address	Bit Range	Register name	Default	Type	SiT92315 Bit Name	Description and Function
	5				RB_OE10	
	4				RB_OE9	
	3				RB_OE8	
	2				RB_OE7	
	1				RB_OE6	
	0				RB_OE5	
0x04	7:0	SBEN_PIN_READ_BACK	0	RO	Reserved	Reserved
0x05	7:4	VIN_REV_ID	0	RO	REVISION_ID	0000: revA
	3:0		0			Aura Product
0x06	7:0	DEV_ID	0	RO	DEVICE_ID	Device ID bits[7:0] map to register bits[7:0] directly.
0x07	7:5	BYTES_READ_COUNT	0	RO	Reserved	Reserved
	4:0		7	RW	BYTES_READ_COUNT_VALUE	Writing to this register configures how many bytes will be read back on a block read.
0x08	7	SBI_MASK_0	1	RW	MASK7	Side Band Mask Register (Register functional only when SBEN = 1)
	6				MASK6	
	5				MASK5	
	4				MASK4	
	3				MASK3	
	2				MASK2	
	1				MASK1	
	0				MASK0	
0x09	7	SBI_MASK_1	0	RW	MASK15	Side Band Mask Register (Register functional only when SBEN = 1)
	6				MASK14	
	5				MASK13	
	4				MASK12	

Register Address	Bit Range	Register name	Default	Type	SiT92315 Bit Name	Description and Function
	3				MASK11	
	2				MASK10	
	1				MASK9	
	0				MASK8	
0x0A	7:4	SBI_MASK_2	0	RW	SPARE	Side Band Mask Register (Register functional only when SBEN = 1)
	3				MASK19	
	2				MASK18	
	1				MASK17	
	0				MASK16	
0x14	7:5	STOP_STATE_CONFIG_REG	0	RW	OUTPUT_AMPLITUDE	AMP – Global Differential Output Control 0: 0.90 V 1: 0.85 V 2: 0.80 V 3: 0.75 V 4: 1.10 V 5: 1.05 V 6: 1.00 V 7: 0.95 V
	4:2		0	RW	SPARE	
	1:0		0	RW	STOP_STATE	00 = Low/Low 01 = HiZ/HiZ 10 = High/Low 11 = Low/High

Package Information

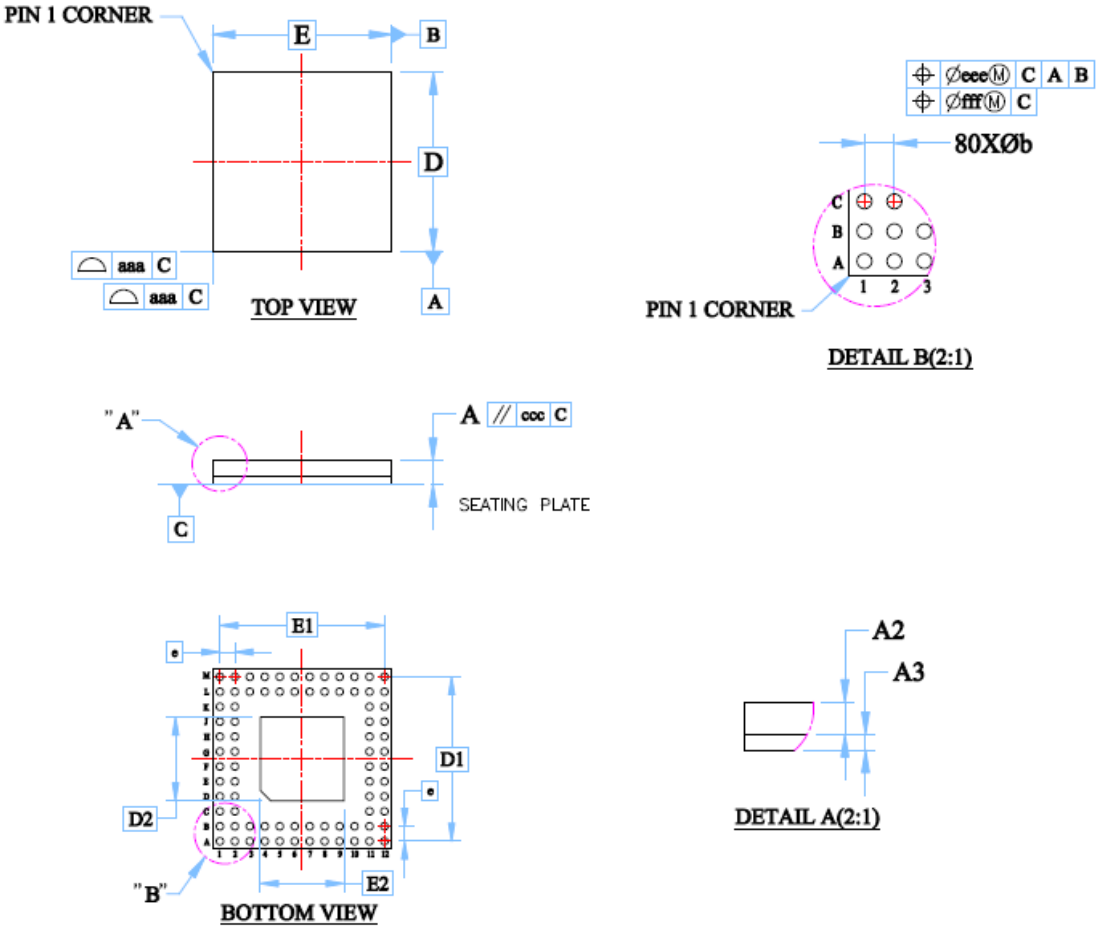


Figure 12 Package Diagram SiT92315 - 80 Pin – LGA

Description	Symbol	Millimeter		
		MIN	NOM	MAX
Total Thickness	A	0.70	0.80	0.90
Stand Off	A1	-	-	-
Mold Thickness	A2	-	0.54 BSC	-
Material Thickness	A3	0.22	0.26	0.30
Package Size	D	5.9	6.0	6.1
Package Size	E	5.9	6.0	6.1
Ball Pitch	e		0.5 BSC	
Ball Size	b	0.20	0.25	0.30
Edge Ball Center to Center	D1	-	5.5 BSC	-
	E1	-	5.5 BSC	-
Package Edge Profile	aaa		0.10	
Substrate Flatness	bbb		-	
Mold Flatness	ccc		0.10	
Ball Coplanarity	ddd		-	
Ball position Offset (Package)	eee		0.15	
Ball Position Offset (Ball)	fff		0.08	
Expose Pad	D2	2.7	2.8	2.9
	E2	2.7	2.8	2.9

Table 15. Revision History

Revisions	Release Date	Change Summary
0.5	Nov 10, 2023	Initial Release

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