SiT92114 1.8 V to 3.3 V High Performance LVCMOS Clock Buffer Output, Ultra Low Jitter Buffer

Description

The SiT92114 is a high-performance LVCMOS clock buffer family of devices. It has an additive phase jitter of 50 fs RMS.

The SiT92114 supports a synchronous glitch-free output enable (OE) function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It can operate from a 1.8 V to 3.3 V supply.

Applications

- 5G, 4G Base stations
- Telecom Equipment
- Servers

Features

- High-performance 1:4 Buffer
- LVCMOS clock buffer
- Very low pin-to-pin skew: <50 ps
- Very low additive jitter: <50 fs
- Supply voltage: 1.8 V to 3.3 V
- 3.3 V tolerant input clock
- F_{MAX} = 200 MHz
- Integrated serial termination for 50 Ω channel
- Packaged in 8 pin, 2.0 mm x 2.0 mm DFN package and 3.0 mm x 4.4 mm TSSOP package.

Order samples

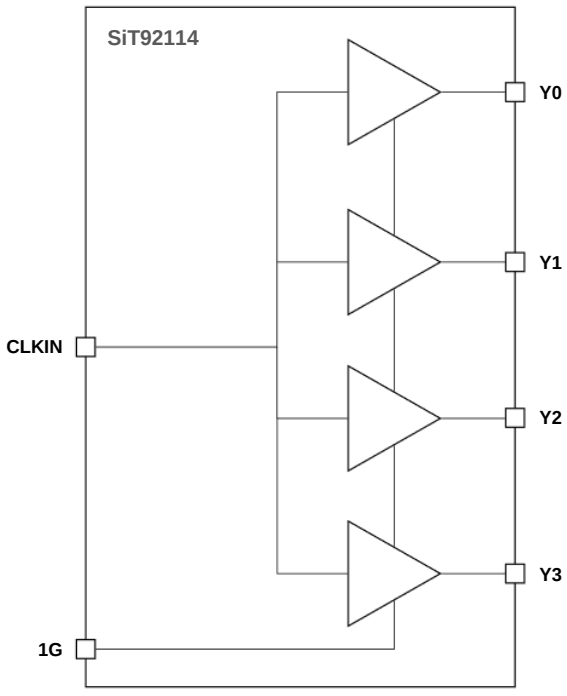

Figure 1. SiT92114 Functional Overview

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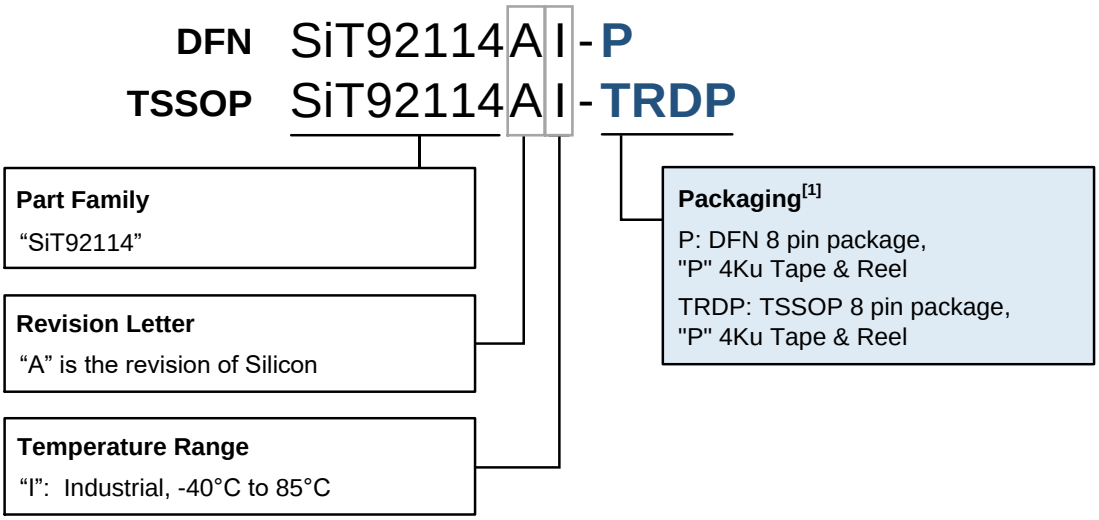
Ordering Information



Note:

1. For TSSOP package options, please contact SiTime.

Electrical Characteristics

Table 1. Absolute Maximum Ratings

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Supply Voltage, VDD			3.6		3.6	V
Output Enable and All Outputs			-0.4		VDD+0.3	V
Input voltage, CLKIN			-0.4		3.465	V
Ambient Operating Temperature,			-40		+105	°C
Storage Temperature			-65		+150	°C
Junction Temperature					+150	°C
Soldering Temperature					+260	°C
Moisture Sensitivity Level	8-DFN	MSL	3			

Notes:

1. Exceeding maximum ratings may shorten the useful life of the device.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 2. Recommended Operating Supply and Temperature

Parameter	Symbol	Min	Typ	Max	Units
Ambient Operating Temperature		-40		+105	°C
Power Supply Voltage (Measured in respect to GND)		+1.71		+3.465	V

Table 3. DC Electrical Characteristics V_{DD} = 1.8 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Voltage		V_{DD}	1.71	1.8	1.89	V
Input High Voltage, CLKIN[1]		V_{IH}	0.7×V_{DD}			V
Input Low Voltage, CLKIN[1]		V_{IL}			0.3×V_{DD}	V
Input High Voltage, 1G		V_{IH}	1.6		V_{DD}	V
Input Low Voltage, 1G		V_{IL}			0.6	V
Output High Voltage	I_{OH} = -5 mA	V_{OH}	1.4			V
Output Low Voltage	I_{OL} = 5 mA	V_{OL}			0.2	V
Nominal Output Impedance		Z_O		50		Ω
Input Capacitance	CLKIN, 1G pin	C_{IN}		5		pF
Operating Supply Current[2]	0.001 MHz, C_L = 5 pF	I_{DD}		0.7	1.7	mA
	0.008 MHz, C_L = 5 pF			0.7	1.7	
	40 MHz, C_L = 5 pF			11	13	
	100 MHz, C_L = 5 pF			25	30	
	156.25 MHz, C_L = 5 pF			37	47	
	200 MHz, C_L = 5 pF			39	57	

Notes:

1. Nominal switching threshold is VDD/2.
2. TA = -40°C to 105°C unless stated otherwise.

Table 4. DC Electrical Characteristics V_{DD} = 2.5 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Voltage		V_{DD}	2.375	2.5	2.625	V
Input High Voltage, CLKIN[1]		V_{IH}	0.7×V_{DD}			V
Input Low Voltage, CLKIN[1]		V_{IL}			0.3×V_{DD}	V
Input High Voltage, 1G		V_{IH}	1.8		V_{DD}	V
Input Low Voltage, 1G		V_{IL}			0.7	V
Output High Voltage	I_{OH} = -8 mA.	V_{OH}	1.9			V
Output Low Voltage	I_{OL} = 8 mA.	V_{OL}			0.5	V
Nominal Output Impedance		Z_O		50		Ω
Input Capacitance	CLKIN, 1G pin.	C_{IN}		5		pF
Operating Supply Current[2]	0.001 MHz, C_L = 5 pF.	I_{DD}		0.9	2	mA
	0.008 MHz, C_L = 5 pF.			0.9	2	
	40 MHz, C_L = 5 pF.			15	17.2	
	100 MHz, C_L = 5 pF.			35	42	
	156.25 MHz, C_L = 5 pF.			52	67	
	200 MHz, C_L = 5 pF.			56	80	

Notes:

1. Nominal switching threshold is VDD/2.
2. TA = -40°C to 105°C unless stated otherwise.

Table 5. DC Electrical Characteristics - V_{DD} = 3.3 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Voltage		V_{DD}	3.135	3.3	3.465	V
Input High Voltage, CLKIN[1]		V_{IH}	0.7×V_{DD}			V
Input Low Voltage, CLKIN[1]		V_{IL}			0.3×V_{DD}	V
Input High Voltage, 1G		V_{IH}	2.1		V_{DD}	V
Input Low Voltage, 1G		V_{IL}			0.8	V
Output High Voltage	I_{OH} = -12 mA	V_{OH}	2.4			V
Output Low Voltage	I_{OL} = 12 mA	V_{OL}			0.7	V
Nominal Output Impedance		Z_O		50		Ω
Input Capacitance	CLKIN, 1G pin	C_{IN}		5		pF
Operating Supply Current[2]	0.001 MHz, C_L = 5 pF	I_{DD}		1.2	2.2	mA
	0.008 MHz, C_L = 5 pF			1.2	2.2	
	40 MHz, C_L = 5 pF			19	23.3	
Operating Supply Current[2]	100 MHz, C_L = 5 pF	I_{DD}		45	54	
	156.25 MHz, C_L = 5 pF			67	87	
	200 MHz, C_L = 5 pF			75	107	

Notes:

1. Nominal switching threshold is VDD/2.
2. TA = -40 °C to +105 °C unless stated otherwise.

Table 6. AC Electrical Characteristics - V_{DD} = 1.8 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency			0		200	MHz
Input Slew rate			2			V/ns
Output Rise Time (5 pF load)[2]	0.36 V to 1.44 V, C_L = 5 pF	t_{OR}		0.65	1.2	Ns
Output Fall Time (5 pF load)[2]	1.44 V to 0.36 V, C_L = 5 pF	t_{OF}		0.65	1.2	Ns
Start-up Time	Part start-up time for valid outputs after VDD ramp-up.	$t_{START-UP}$			3	Ms
Propagation Delay[3]		t_{PD}	0.24		1.6	Ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz.	t_{JIT}			0.06	Ps
Output to Output Skew	Rising edges at VDD/2 [1]	t_{SK}		35	50	Ps
Device to Device Skew	Rising edges at VDD/2				200	Ps
Output Enable Time	C_L ≤ 5 pF Frequency = 25Mhz	t_{EN}			3	Cycles
	C_L ≤ 5 pF Frequency = 200Mhz	t_{EN}			5	Cycles
Output Disable Time	C_L ≤ 5 pF. Frequency = 25Mhz	t_{DIS}			3	Cycles
	C_L ≤ 5 pF Frequency = 200Mhz	t_{DIS}			5	Cycles
Duty Cycle		t_{DC}		50		%

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40°C to 105°C unless stated otherwise.
3. With rail to rail input clock.

Table 7. AC Electrical Characteristics - V_{DD} = 2.5 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency			0		200	MHz
Input Slew rate			2			V/ns
Output Rise Time (5 pF load)[2]	0.5 V to 2.0 V, C_L = 5 pF	t_{OR}		0.63	1.2	ns
Output Fall Time (5 pF load)[2]	2.0 V to 0.5 V, C_L = 5 pF	t_{OF}		0.63	1.2	ns
Start-up Time	Part start-up time for valid outputs after V_{DD} ramp-up.	$t_{START-UP}$			3	ms
Propagation Delay[3]		t_{PD}	0.24		1.6	ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz.	t_{JIT}			0.06	ps
Output to Output Skew	Rising edges at V_{DD}/2 [1]	t_{SK}		35	50	ps
Device to Device Skew	Rising edges at V_{DD}/2	t_{SKD}			200	ps
Output Enable Time	C_L ≤ 5 pF Frequency = 25Mhz	t_{EN}			3	cycles
	C_L ≤ 5 pF Frequency = 200Mhz	t_{EN}			5	cycles
Output Disable Time	C_L ≤ 5 pF Frequency = 25Mhz	t_{DIS}			3	cycles
	C_L ≤ 5 pF Frequency = 200Mhz	t_{DIS}			5	cycles
Duty Cycle		t_{DS}		50		%

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40°C to 105°C unless stated otherwise.
3. With rail to rail input clock.

Table 8. AC Electrical Characteristics - V_{DD} = 3.3 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency			0		200	MHz
Input Slew rate			2			V/ns
Output Rise Time (5 pF load)[2]	0.66 V to 2.64 V, CL = 5 pF	t_{OR}		0.61	1.2	ns
Output Fall Time (5 pF load)[2]	2.64 V to 0.66 V, CL = 5 pF	t_{OF}		0.61	1.2	ns
Start-up Time	Part start-up time for valid outputs after VDD ramp-up.	$t_{START-UP}$			3	ms
Propagation Delay[3]		t_{PD}	0.24		1.6	ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz	t_{JIT}			0.05	ps
Output to Output Skew	Rising edges at VDD/2[1]	t_{SK}		35	50	ps
Device to Device Skew	Rising edges at VDD/2	t_{SKD}			200	ps
Output Enable Time	C_L ≤ 5 pF Frequency = 25Mhz	t_{EN}			3	cycles
	C_L ≤ 5 pF Frequency = 200Mhz	t_{EN}			5	cycles
Output Disable Time	C_L ≤ 5 pF Frequency = 25Mhz	t_{DIS}			3	cycles
	C_L ≤ 5 pF Frequency = 200Mhz	t_{DIS}			5	cycles
Duty Cycle		t_{DC}		50		%

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40°C to 105°C unless stated otherwise.
3. With rail to rail input clock.

Table 9. ESD Ratings

Parameter	Conditions	Symbol	Min	Typ	Max	Units
ESD (Human Body Model)	AEC-Q100-002	ESD_{HBM}	-	2000	-	V
ESD(Charged Device Model)	AEC-Q100-011	ESD_{CDM}	-	500	-	V

Table 10. Thermal Characteristics

Package	ΘJA	Units
8-DFN	75	°C/W; still air

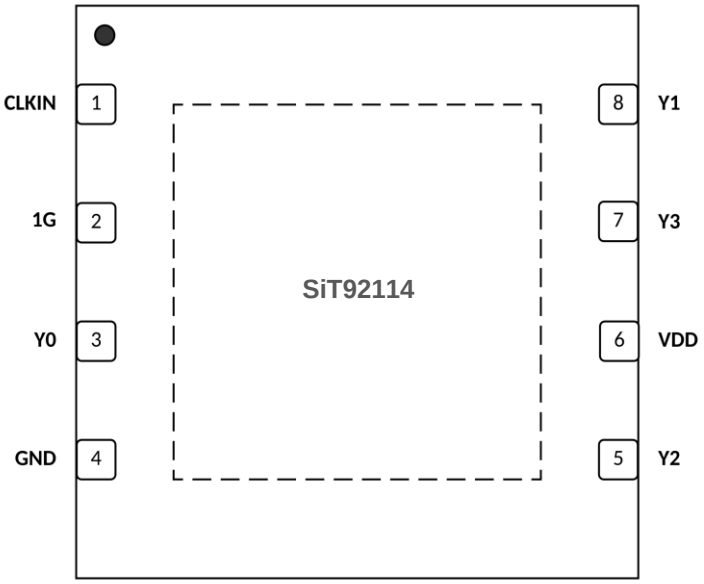


Figure 2. SiT92114 Pin Configuration

Table 11. Detailed Pin Description

Pin Name	Pin Number	Functionality SiT92114
Y0	3	LVCMOS output 0
Y1	8	LVCMOS output 1
Y2	5	LVCMOS output 2
Y3	7	LVCMOS output 3
CLKIN	1	Single Ended Input Clock
1G	2	All outputs enable/disable
VDD	6	Core Supply Voltage, VDD
GND	4	Ground

Functional Description

Output Logic Tables

Table 12. Output Logic Tables

Inputs		Output
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

Typical Application Diagram

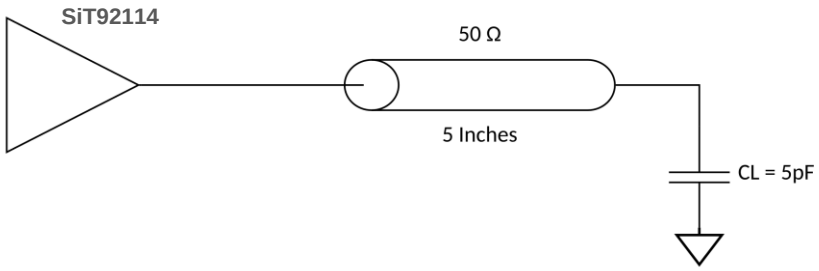


Figure 3. SiT92114 Typical Application Load

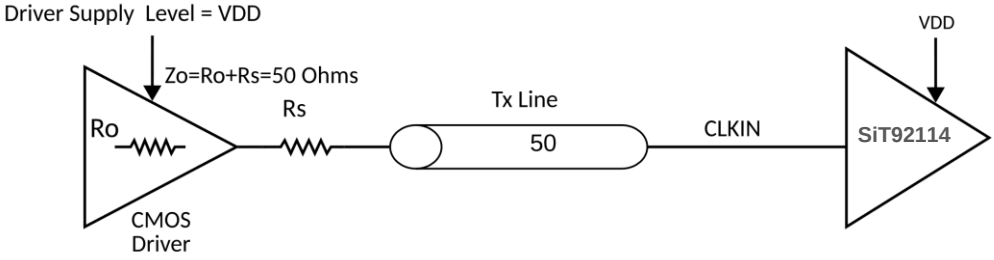


Figure 4. Recommended input clock configuration

Input Clock and Power Supply Sequencing

The clock input should be available after the SiT92114 power supply is up. An example of the power up sequence is shown in Figure 5.

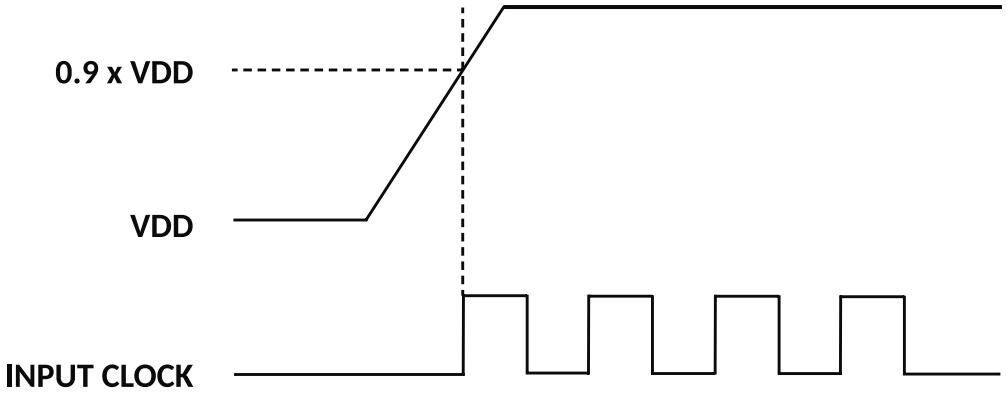
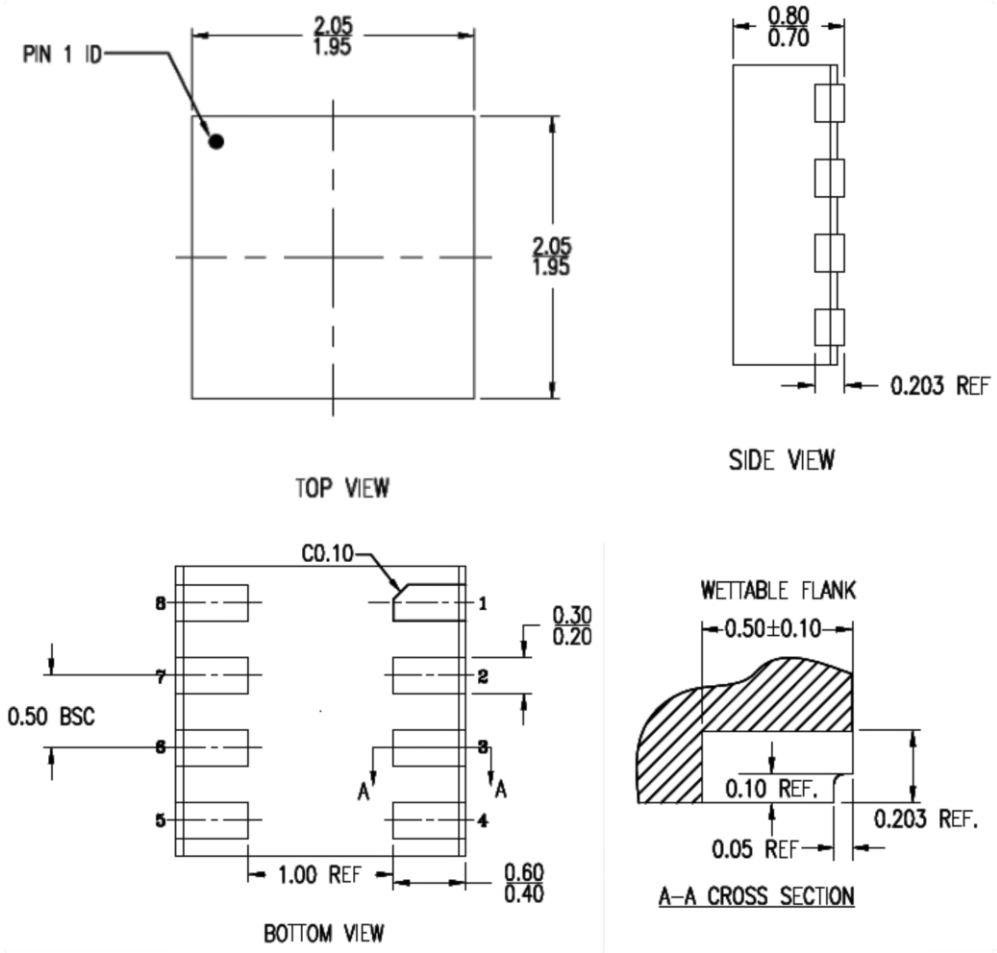


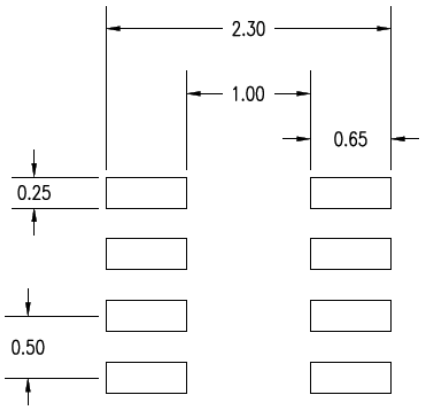
Figure 5. Input clock to VDD ramp timing requirement for SiT92114

Dimensions and Patterns – 2.0 mm x 2.0 mm DFN Package

Package Size – SiT92114 Cross Sections (Unit: mm)[1,2]



Recommended Land Pattern (Unit: mm) [2,3,4]

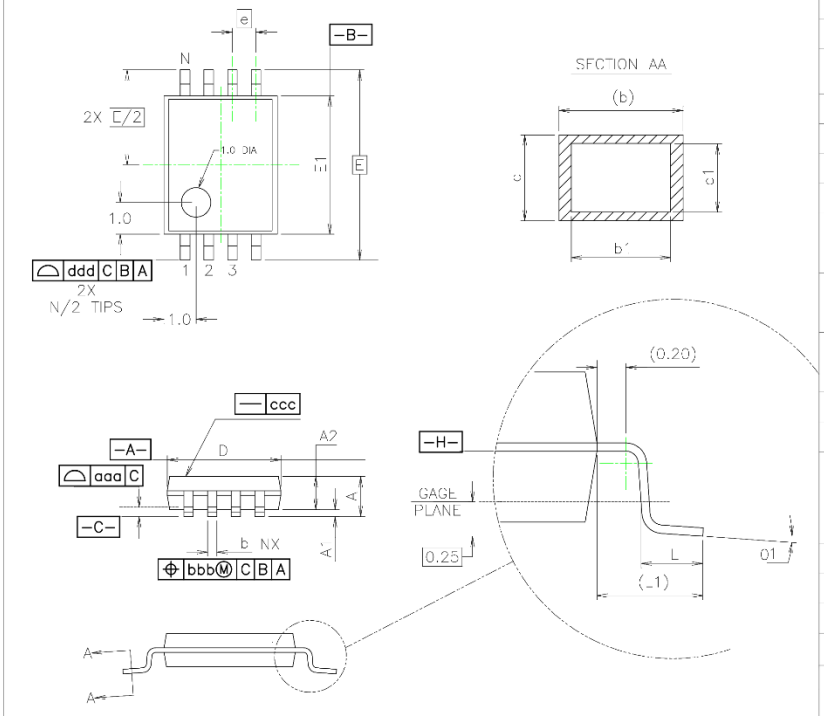


Note:

1. All Dimensions and Tolerancing Conform to ANSI Y14.5M -1982.
2. All Dimensions are in Millimeters (mm).
3. All Angles are in Degrees.
4. Land Pattern Recommendation per IPC-7351B Generic Requirement for Mount Design and Land Pattern.

Dimensions and Patterns – 3.0 mm x 4.4 mm TSSOP Package

Package Size – Dimensions (Unit: mm)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	---	---	1.10
STAND OFF	A1	0.05	---	0.15
PACKAGE THICKNESS	A2	0.85	0.90	0.95
PACKAGE LENGTH	D	2.90	3.00	3.10
LEAD SPREAD	E		6.4 BSC	
PACKAGE WIDTH	E1	4.30	4.40	4.50
FOOT LENGTH	L	0.5	0.6	0.75
FOOT ANGLE	Θ1	0°	---	8°
LEAD COUNT	N		8	
LEAD WIDTH	b	0.19	---	0.30
	b1	0.19	0.22	0.25
LEAD THICKNESS	c	0.09	---	0.20
	c1	0.09	---	0.16
LEAD LENGTH	L1		1.0 REF	
COPLANARITY	aaa		0.10	
PACKAGE TOLERANCE	bbb		0.10	
	ccc		0.05	
	ddd		0.20	
LEAD PITCH	e		0.65 BSC	

NOTE

1. ALL DIMENSION IN MM

PKG INFO		DRAWING NO.	
8TSSOP 4.40X3.00X0.90 mm		POD-101-TSSOP-008-A04430	
		REV	SHEET
DATE	20/8/24	A01	01

Table 13. Revision History

Revisions	Release Date	Change Summary
0.5	21-Nov-2023	Initial Release
0.51	29-Apr-2024	Updated Packaging options in Ordering Code
0.52	13-Aug-2024	Added DFN and TSSOP package in Ordering Code; Added TSSOP package drawing
1.0	27-Sep-2024	Ordering information 4Ku Tape & Reel package code -P to replace 3Ku Tape & Reel options -T

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