

Description

The SiT92112 is a high-performance LVCMOS clock buffer family of devices. It has an additive phase jitter of 50 fs RMS.

The SiT92112 supports a synchronous glitch-free output enable (OE) function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It can operate from a 1.8 V to 3.3 V supply.

Applications

- 5G, 4G Base stations
- Telecom Equipment
- Servers

Features

- High-performance 1:2 Buffer
- LVCMOS clock buffer
- Very low pin-to-pin skew: <50 ps
- Very low additive jitter: <50 fs
- Supply voltage: 1.8 V to 3.3 V
- 3.3 V tolerant input clock
- $F_{MAX} = 200$ MHz
- Integrated serial termination for 50 Ω channel
- Packaged in 8 pin, 2 x 2 mm DFN packages.

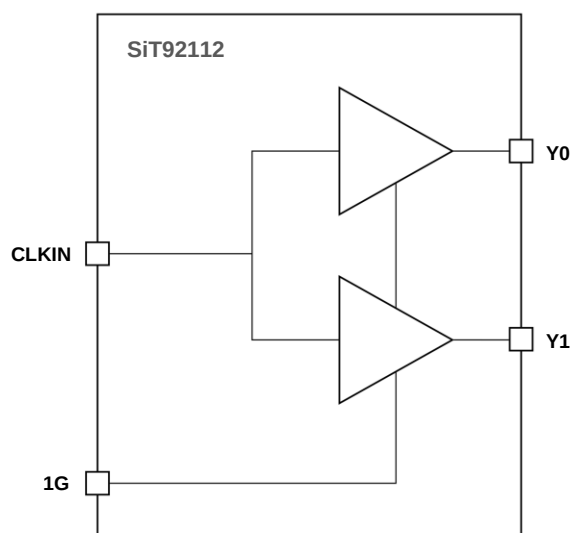


Figure 1. Functional Overview of SiT92112

Table of Contents

Description..... 1

Applications 1

Features..... 1

Ordering Information..... 3

Electrical Characteristics..... 4

Functional Description 9

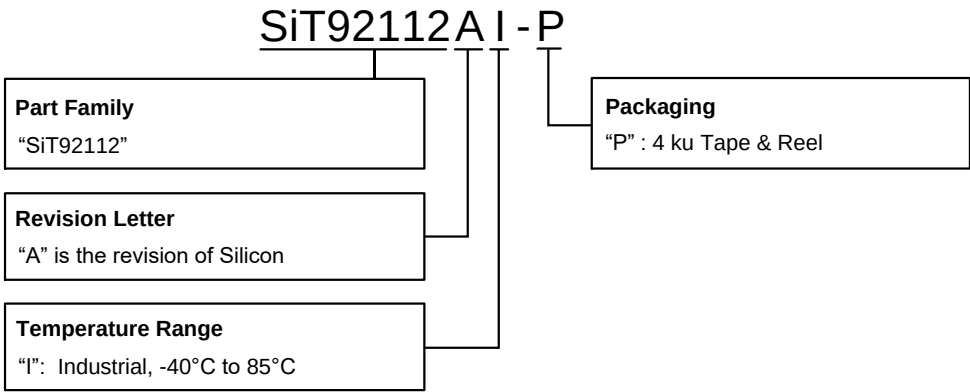
 Output Logic Tables 9

Typical Application Diagram 10

Input Clock and Power Supply Sequencing 11

Package Dimensions and Patterns 12

Ordering Information



Electrical Characteristics

Table 1. Absolute Maximum Ratings

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Supply Voltage, V_{DD}			3.6		3.6	V
Output Enable and All Outputs			-0.4		$V_{DD}+0.3$	V
Input voltage, CLKIN			-0.4		3.465	V
Ambient Operating Temperature			-40		+105	°C
Storage Temperature			-65		+150	°C
Junction Temperature					+150	°C
Soldering Temperature					+260	°C
Moisture Sensitivity Level	8-DFN	MSL	3			

Notes:

1. Exceeding maximum ratings may shorten the useful life of the device.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 2. Recommended Operating Supply and Temperature

Parameter	Symbol	Min	Typ	Max	Units
Ambient Operating Temperature		-40		+105	°C
Power Supply Voltage (Measured in respect to GND)		+1.71		+3.465	V

Table 3. DC Electrical Characteristics – $V_{DD} = 1.8 \text{ V} \pm 5\%$

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Voltage		V_{DD}	1.71	1.8	1.89	V
Input High Voltage, CLKIN ^[1]		V_{IH}	$0.7 \times V_{DD}$			V
Input Low Voltage, CLKIN ^[1]		V_{IL}			$0.3 \times V_{DD}$	V
Input High Voltage, 1G		V_{IH}	1.6		V_{DD}	V
Input Low Voltage, 1G		V_{IL}			0.6	V
Output High Voltage	$I_{OH} = -5 \text{ mA}$	V_{OH}	1.4			V
Output Low Voltage	$I_{OL} = 5 \text{ mA}$	V_{OL}			0.2	V
Nominal Output Impedance		Z_O		50		Ω
Input Capacitance	CLKIN, 1G pin	C_{IN}		5		pF
Operating Supply Current ^[2]	0.001 MHz, $C_L = 5 \text{ pF}$	I_{DD}		0.7	1.7	mA
	0.008 MHz, $C_L = 5 \text{ pF}$			0.7	1.7	
	40 MHz, $C_L = 5 \text{ pF}$			7	8.3	
	100 MHz, $C_L = 5 \text{ pF}$			15.4	18.5	
	156.25 MHz, $C_L = 5 \text{ pF}$			23.2	29.5	
	200 MHz, $C_L = 5 \text{ pF}$			25.2	36.8	

Notes:

1. Nominal switching threshold is $V_{DD}/2$.
2. $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ unless stated otherwise.

Table 4. DC Electrical Characteristics – $V_{DD} = 2.5 \text{ V} \pm 5\%$

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Voltage		V_{DD}	2.375	2.5	2.625	V
Input High Voltage, CLKIN ^[1]		V_{IH}	$0.7 \times V_{DD}$			V
Input Low Voltage, CLKIN ^[1]		V_{IL}			$0.3 \times V_{DD}$	V
Input High Voltage, 1G		V_{IH}	1.8		V_{DD}	V
Input Low Voltage, 1G		V_{IL}			0.7	V
Output High Voltage	$I_{OH} = -8 \text{ mA}$	V_{OH}	1.9			V
Output Low Voltage	$I_{OL} = 8 \text{ mA}$	V_{OL}			0.5	V
Nominal Output Impedance		Z_O		50		Ω
Input Capacitance	CLKIN, 1G pin	C_{IN}		5		pF
Operating Supply Current ^[2]	0.001 MHz, $C_L = 5 \text{ pF}$	I_{DD}		0.9	2	mA
	0.008 MHz, $C_L = 5 \text{ pF}$			0.9	2	
	40 MHz, $C_L = 5 \text{ pF}$			9.7	11.2	
	100 MHz, $C_L = 5 \text{ pF}$			22	26.5	
	156.25 MHz, $C_L = 5 \text{ pF}$			33.2	42.7	
	200 MHz, $C_L = 5 \text{ pF}$			36.7	52.4	

Notes:

- Nominal switching threshold is $V_{DD}/2$.
- $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ unless stated otherwise.

Table 5. DC Electrical Characteristics – $V_{DD} = 3.3 \text{ V} \pm 5\%$

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Voltage		V_{DD}	3.135	3.3	3.465	V
Input High Voltage, CLKIN ^[1]		V_{IH}	$0.7 \times V_{DD}$			V
Input Low Voltage, CLKIN ^[1]		V_{IL}			$0.3 \times V_{DD}$	V
Input High Voltage, 1G		V_{IH}	2.1		V_{DD}	V
Input Low Voltage, 1G		V_{IL}			0.8	V
Output High Voltage	$I_{OH} = -12 \text{ mA}$	V_{OH}	2.4			V
Output Low Voltage	$I_{OL} = 12 \text{ mA}$	V_{OL}			0.7	V
Nominal Output Impedance		Z_O		50		Ω
Input Capacitance	CLKIN, 1G pin	C_{IN}		5		pF
Operating Supply Current ^[2]	0.001 MHz, $C_L = 5 \text{ pF}$	I_{DD}		1.2	2.2	mA
	0.008 MHz, $C_L = 5 \text{ pF}$			1.2	2.2	
	40 MHz, $C_L = 5 \text{ pF}$			12.6	15.5	
Operating Supply Current ^[2]	100 MHz, $C_L = 5 \text{ pF}$	I_{DD}		29.4	35.3	
	156.25 MHz, $C_L = 5 \text{ pF}$			44.1	57.2	
	200 MHz, $C_L = 5 \text{ pF}$			50.9	72.7	

Notes:

- Nominal switching threshold is $V_{DD}/2$.
- $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ unless stated otherwise.

Table 6. AC Electrical Characteristics – $V_{DD} = 1.8\text{ V} \pm 5\%$

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency	DC coupled		0		200	MHz
	AC coupled		0.1		200	MHz
Input Slew rate			2			V/ns
Input swing, AC coupled mode	CLKIN biased at 0.5 VDD	V _{SWING_AC}	0.5			V
Output Rise Time (5 pF load) ^[2]	0.36 V to 1.44 V, C _L = 5 pF	t _{OR}		0.65	1.2	ns
Output Fall Time (5 pF load) ^[2]	1.44 V to 0.36 V, C _L = 5 pF	t _{OF}		0.65	1.2	ns
Start-up Time	Part start-up time for valid outputs after VDD ramp-up	t _{START-UP}			3	ms
Propagation Delay ^[3]		t _{PD}	0.24		1.6	ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz	t _{JIT}			0.06	ps
Output to Output Skew	Rising edges at VDD/2 ^[1]	t _{SK}		35	50	ps
Device to Device Skew	Rising edges at VDD/2				200	ps
Output Enable Time	C _L ≤ 5 pF Frequency = 25 Mhz	t _{EN}			3	cycles
	C _L ≤ 5 pF Frequency = 200 Mhz	t _{EN}			5	cycles
Output Disable Time	C _L ≤ 5 pF. Frequency = 25 Mhz	t _{DIS}			3	cycles
	C _L ≤ 5 pF Frequency = 200 Mhz	t _{DIS}			5	cycles
Duty Cycle	DC couple mode	t _{DC}		50		%
	AC couple mode (AC swing > 0.8 V)					

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40°C to +105°C unless stated otherwise.
3. With rail to rail input clock.

Table 7. AC Electrical Characteristics – $V_{DD} = 2.5\text{ V} \pm 5\%$

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency	DC coupled		0		200	MHz
	AC coupled		0.1		200	MHz
Input Slew rate			2			V/ns
Input swing, AC coupled mode	CLKIN biased at 0.5 VDD	V _{SWING_AC}	0.5			V
Output Rise Time (5 pF load) ^[2]	0.5 V to 2.0 V, C _L = 5 pF	t _{OR}		0.63	1.2	ns
Output Fall Time (5 pF load) ^[2]	2.0 V to 0.5 V, C _L = 5 pF	t _{OF}		0.63	1.2	ns
Start-up Time	Part start-up time for valid outputs after V _{DD} ramp-up	t _{START-UP}			3	ms
Propagation Delay ^[3]		t _{PD}	0.24		1.6	ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz.	t _{JIT}			0.06	ps
Output to Output Skew	Rising edges at V _{DD} /2 ^[1]	t _{SK}		35	50	ps
Device to Device Skew	Rising edges at V _{DD} /2	t _{SKD}			200	ps
Output Enable Time	C _L ≤ 5 pF Frequency = 25 Mhz	t _{EN}			3	cycles
	C _L ≤ 5 pF Frequency = 200 Mhz	t _{EN}			5	cycles
Output Disable Time	C _L ≤ 5 pF. Frequency = 25 Mhz	t _{DIS}			3	cycles
	C _L ≤ 5 pF Frequency = 200 Mhz	t _{DIS}			5	cycles

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Duty Cycle	DC couple mode	t_{DS}		50		%
	AC couple mode (AC swing > 0.8 V)					

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40°C to +105°C unless stated otherwise.
3. With rail to rail input clock

Table 8. AC Electrical Characteristics - $V_{DD} = 3.3\text{ V} \pm 5\%$

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency	DC coupled		0		200	MHz
	AC coupled		0.1		200	MHz
Input Slew rate			2			V/ns
Input swing, AC coupled mode	CLKIN biased at 0.5VDD	V_{SWING_AC}	0.5			V
Output Rise Time (5 pF load) ^[2]	0.66 V to 2.64 V, CL = 5 pF	t_{OR}		0.61	1.2	ns
Output Fall Time (5 pF load) ^[2]	2.64 V to 0.66 V, CL = 5 pF	t_{OF}		0.61	1.2	ns
Start-up Time	Part start-up time for valid outputs after VDD ramp-up	$t_{START-UP}$			3	ms
Propagation Delay ^[3]		t_{PD}	0.24		1.6	ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz	t_{JIT}			0.05	ps
Output to Output Skew	Rising edges at VDD/2 ^[1]	t_{SK}		35	50	ps
Device to Device Skew	Rising edges at VDD/2	t_{SKD}			200	ps
Output Enable Time	CL ≤ 5 pF Frequency = 25 Mhz	t_{EN}			3	cycles
	CL ≤ 5 pF Frequency = 200 Mhz	t_{EN}			5	cycles
Output Disable Time	CL ≤ 5 pF. Frequency = 25 Mhz	t_{DIS}			3	cycles
	CL ≤ 5 pF Frequency = 200 Mhz	t_{DIS}			5	cycles
Duty Cycle	DC couple mode	t_{DC}		50		%
	AC couple mode (AC swing > 0.8 V)					

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40°C to +105°C unless stated otherwise.
3. With rail to rail input clock.

Table 9. ESD Ratings

Parameter	Conditions	Symbol	Min	Typ	Max	Units
ESD (Human Body Model)	AEC-Q100-002	ESD_{HBM}	-	2000	-	V
ESD (Charged Device Model)	AEC-Q100-011	ESD_{CDM}	-	500	-	V

Table 10. Thermal Characteristics

Package	Θ_{JA}	Units
8-DFN	75	°C/W; still air

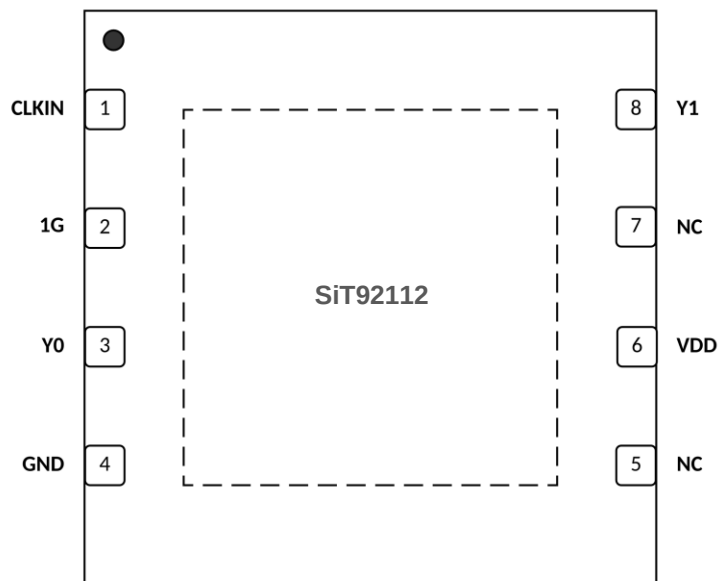


Figure 2. SiT92112 Pin Configuration

Table 11. Detailed Pin Description

Pin Name	Pin Number	Functionality SiT92112
Y0	3	LVC MOS output 0
Y1	8	LVC MOS output 1
NC	5	No Connect
NC	7	No Connect
CLKIN	1	Single Ended Input Clock
1G	2	All outputs enable/disable
VDD	6	Core Supply Voltage, VDD
GND	4	Ground

Functional Description

Output Logic Tables

Table 12. Output Logic Tables

Inputs		Output
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

Typical Application Diagram

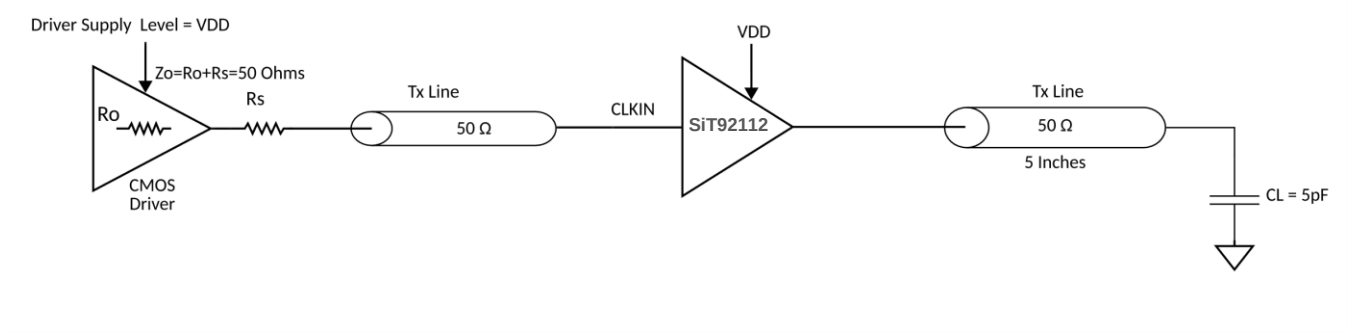


Figure 3. SiT92112 Typical Application Load – DC Coupled Mode

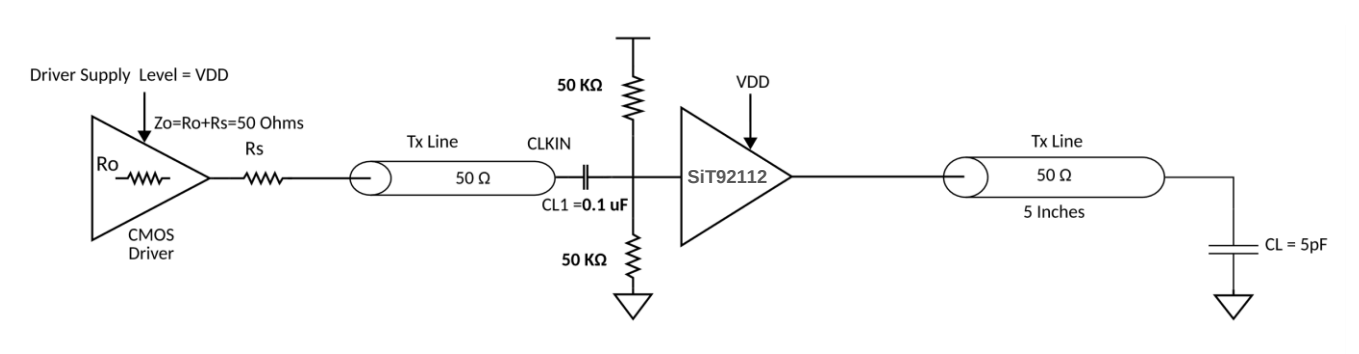


Figure 4. SiT92112 Typical Application Load – AC Coupled Mode

Input Clock and Power Supply Sequencing

The clock input should be available after the SiT92112 power supply is up. An example of the power up sequence is shown in [Figure 5](#).

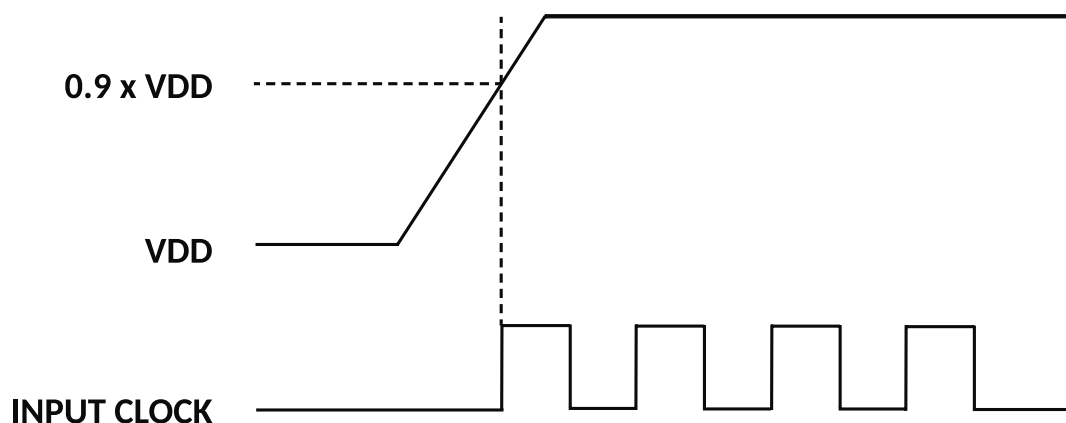
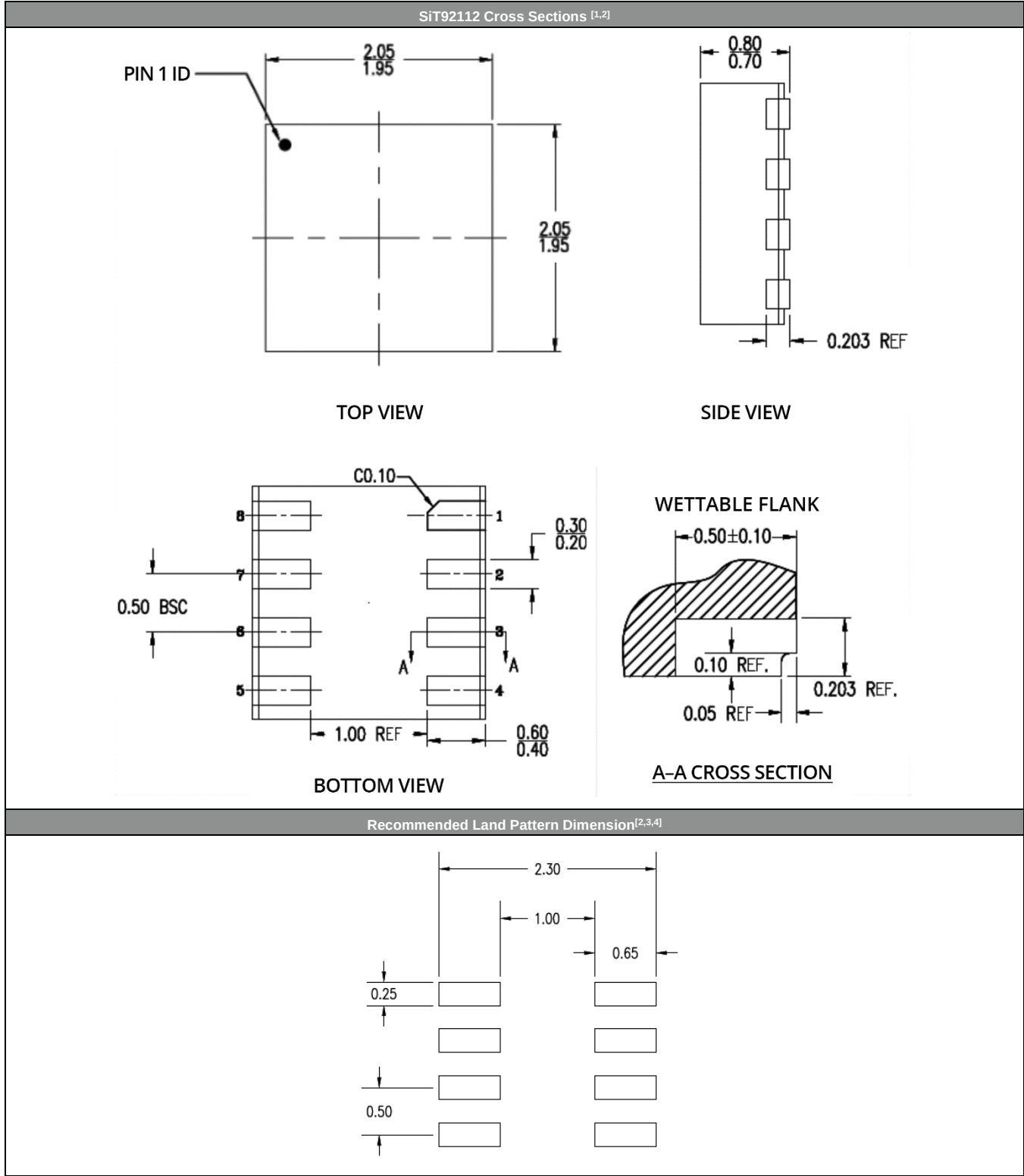


Figure 5. Input clock to VDD ramp timing requirement for SiT92112

Package Dimensions and Patterns



Notes:

1. All Dimensions and Tolerancing Conform to ANSI Y14.5M -1982.
2. All Dimensions are in Millimeters (mm).
3. All Angles are in Degrees.
4. Land Pattern Recommendation per IPC-7351B Generic Requirement for Mount Design and Land Pattern.

Table 13. Revision History

Revisions	Release Date	Change Summary
0.5	8-Nov-2023	Initial Release
0.51	19-Nov-2024	Corrected Features; Corrected Pin Names in Table 11 Datasheet formatting fix
0.52	7-Jan-2025	Updated with "P" reel code

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | Phone: +1-408-328-4400 | Fax: +1-408-328-4439

© SiTime Corporation 2023-2025. The information contained herein is subject to change at any time without notice. SiTime assumes no responsibility or liability for any loss, damage or defect of a Product which is caused in whole or in part by (i) use of any circuitry other than circuitry embodied in a SiTime product, (ii) misuse or abuse including static discharge, neglect or accident, (iii) unauthorized modification or repairs which have been soldered or altered during assembly and are not capable of being tested by SiTime under its normal test conditions, or (iv) improper installation, storage, handling, warehousing or transportation, or (v) being subjected to unusual physical, thermal, or electrical stress.

Disclaimer: SiTime makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any SiTime product and any product documentation. Products sold by SiTime are not suitable or intended to be used in a life support application or component, to operate nuclear facilities, or in other mission critical applications where human life may be involved or at stake. All sales are made conditioned upon compliance with the critical uses policy set forth below.

CRITICAL USE EXCLUSION POLICY
BUYER AGREES NOT TO USE SITIME'S PRODUCTS FOR ANY APPLICATION OR IN ANY COMPONENTS USED IN LIFE SUPPORT DEVICES OR TO OPERATE NUCLEAR FACILITIES OR FOR USE IN OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE OR PROPERTY MAY BE AT STAKE.

SiTime owns all rights, title and interest to the intellectual property related to SiTime's products, including any software, firmware, copyright, patent, or trademark. The sale of SiTime products does not convey or imply any license under patent or other rights. SiTime retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by SiTime. Unless otherwise agreed to in writing by SiTime, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.