SiT8945B PRELIMINARY

115.2 – 137 MHz, -55 to 125°C, Endura™ Series Oscillator

Features

- Best acceleration sensitivity of 0.1 ppb/*g*
- Any frequencies between 115.2 MHz and 137 MHz accurate to 6 decimal points
- 100% pin-to-pin drop-in replacement to quartz-based XO
- Excellent total frequency stability as low as ±20 ppm
- Low power consumption of 3.8 mA typical at 1.8V
- LVCMOS/LVTTL compatible output
- AEC-Q100 qualified
- Industry-standard packages: 2.0 x 1.6, 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free
- Contact SiTime for up-screening and LAT programs

Applications

- Avionics systems
- Field communication systems
- Telemetry applications

Electrical Characteristics

Table 1. Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	115.20	–	137	MHz	Refer to Tables 13 to 15 for the exact list of supported frequencies
Frequency Stability and Aging						
Frequency Stability	F_stab	-20	–	+20	ppm	Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature, rated power supply voltage and load (15 pF ±10%)
		-25	–	+25	ppm	
		-30	–	+30	ppm	
		-50	–	+50	ppm	
Operating Temperature Range						
Operating Temperature Range (ambient)	T_use	-40	–	+85	°C	AEC-Q100 Grade 3
		-40	–	+105	°C	AEC-Q100 Grade 2
		-40	–	+125	°C	AEC-Q100 Grade 1
		-55	–	+125	°C	Extended cold, AEC-Q100 Grade1
Rugged Characteristics						
Acceleration (g) sensitivity, Gamma Vector	F_g	–	–	0.1	ppb/*g*	Low sensitivity grade; total gamma over 3 axes; 15 Hz to 2 kHz; MIL-PRF-55310, computed per section 4.8.18.3.1
Supply Voltage and Current Consumption						
Supply Voltage	Vdd	1.62	1.8	1.98	V	All voltages between 2.25V and 3.63V including 2.5V, 2.8V, 3.0V and 3.3V are supported. Contact SiTime for 1.5V support
		2.25	–	3.63	V	
Current Consumption	Idd	–	6	8	mA	No load condition, f = 125 MHz, Vdd = 2.25V to 3.63V
		–	4.9	6	mA	No load condition, f = 125 MHz, Vdd = 1.62V to 1.98V
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	–	1.5	3	ns	Vdd = 2.25V - 3.63V, 20% - 80%
		–	1.5	2.5	ns	Vdd = 1.8V, 20% - 80%
Output High Voltage	VOH	90%	–	–	Vdd	IOH = -4 mA (Vdd = 3.0V or 3.3V) IOH = -3 mA (Vdd = 2.8V and Vdd = 2.5V) IOH = -2 mA (Vdd = 1.8V)
Output Low Voltage	VOL	–	–	10%	Vdd	IOL = 4 mA (Vdd = 3.0V or 3.3V) IOL = 3 mA (Vdd = 2.8V and Vdd = 2.5V) IOL = 2 mA (Vdd = 1.8V)
Input Characteristics						
Input High Voltage	VIH	70%	–	–	Vdd	Pin 1, OE
Input Low Voltage	VIL	–	–	30%	Vdd	Pin 1, OE
Input Pull-up Impedance	Z_in	–	100	–	kΩ	Pin 1, OE logic high or logic low

Table 1. Electrical Characteristics (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Startup and Resume Timing						
Startup Time	T_start	–	–	5	ms	Measured from the time Vdd reaches its rated minimum value
Enable/Disable Time	T_oe	–	–	130	ns	f = 115.20 MHz. For other frequencies, T_oe = 100 ns + 3 * cycles
Standby Current	I_std	–	2.6	–	µA	Vdd = 2.8V to 3.3V, $\overline{ST}$ = Low, Output is weakly pulled down
		–	1.4	–	µA	Vdd = 2.5V, $\overline{ST}$ = Low, Output is weakly pulled down
		–	0.6	–	µA	Vdd = 1.8V, $\overline{ST}$ = Low, Output is weakly pulled down
Jitter						
RMS Period Jitter	T_jitt	–	1.6	2.5	ps	f = 125 MHz, 2.25V to 3.63V
		–	1.8	3	ps	f = 125 MHz, 1.8V
Peak-to-peak Period Jitter	T_pk	–	12	20	ps	f = 125 MHz, Vdd = 2.5V, 2.8V, 3.0V or 3.3V
		–	14	30	ps	f = 125 MHz, Vdd = 1.8V
RMS Phase Jitter (random)	T_phj	–	0.7	–	ps	f = 125 MHz, Integration bandwidth = 900 kHz to 7.5 MHz
		–	1.5	–	ps	f = 125 MHz, Integration bandwidth = 12 kHz to 20 MHz

Table 2. Pin Description

Pin	Symbol		Functionality
1	OE/NC	Output Enable	H[1]: specified frequency output L: output is high impedance. Only output driver is disabled.
		No Connect	Any voltage between 0 and Vdd or Open[1]: Specified frequency output. Pin 1 has no function.
2	GND	Power	Electrical ground[2]
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage[2]

Top View

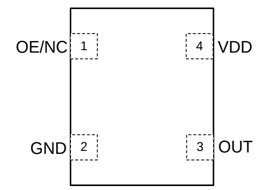


Figure 1. Pin Assignments

Notes:

1. In OE mode, a pull-up resistor of 10kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
2. A capacitor of value 0.1 µF or higher between Vdd and GND is required.

Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Vdd	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Junction Temperature[3]	–	150	°C

Note:

3. Exceeding this temperature for extended period of time may damage the device.

Table 4. Thermal Consideration[4]

Package	θJA, 4 Layer Board (°C/W)	θJA, 2 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050	142	273	30
5032	97	199	24
3225	109	212	27
2520	117	222	26
2016	152	252	36

Note:

4. Refer to JESD51 for θJA and θJC definitions, and reference layout used to determine the θJA and θJC values in the above table.

Table 5. Maximum Operating Junction Temperature[5]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
85°C	93°C
105°C	113°C
125°C	133°C

Note:

5. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 6. Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	**MIL-STD-883F, Method 2002**
Mechanical Vibration	**MIL-STD-883F, Method 2007**
Temperature Cycle	**JESD22, Method A104**
Solderability	**MIL-STD-883F, Method 2003**
Moisture Sensitivity Level	**MSL1 @ 260°C**

Test Circuit and Waveform

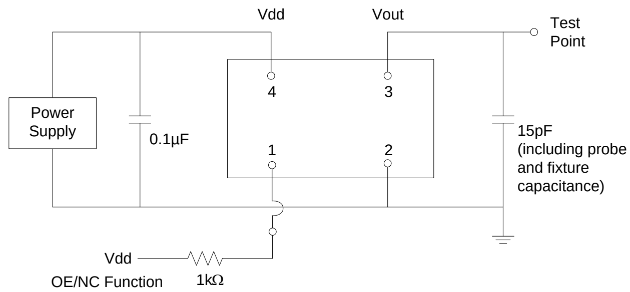


Figure 2. Test Circuit[6]

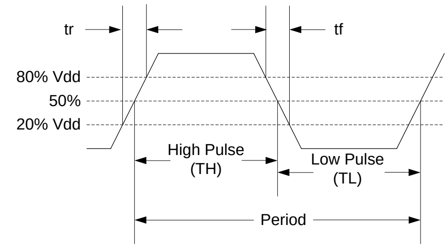


Figure 3. Waveform

Note:

6. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagrams

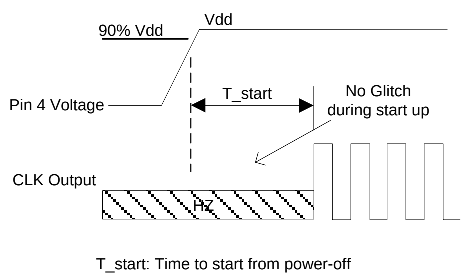


Figure 4. Startup Timing (OE Mode)[7]

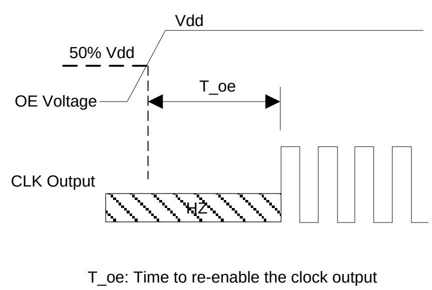


Figure 5. OE Enable Timing (OE Mode Only)

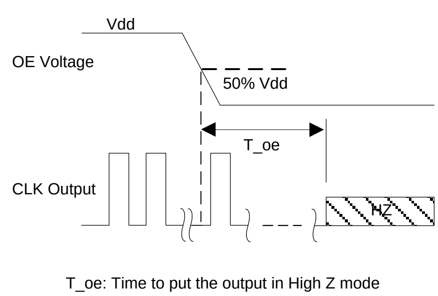


Figure 6. OE Disable Timing (OE Mode Only)

Note:

7. SiT8945 has "no runt" pulses and "no glitch" output during startup or resume.

Performance Plots[8]

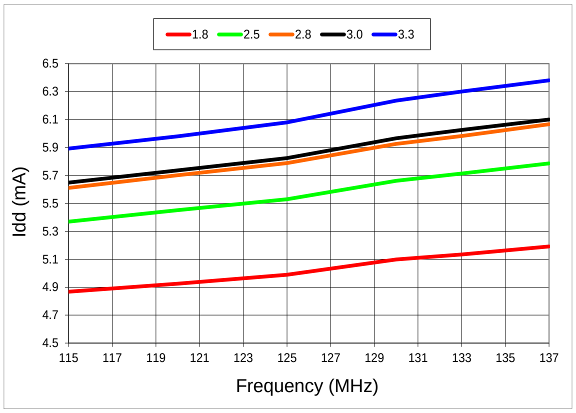


Figure 7. Idd vs Frequency

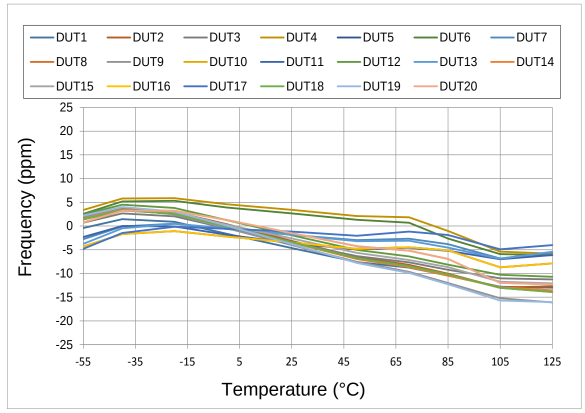


Figure 8. Frequency vs Temperature

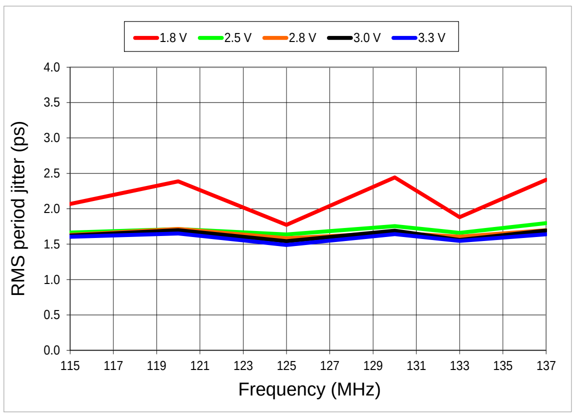


Figure 9. RMS Period Jitter vs Frequency

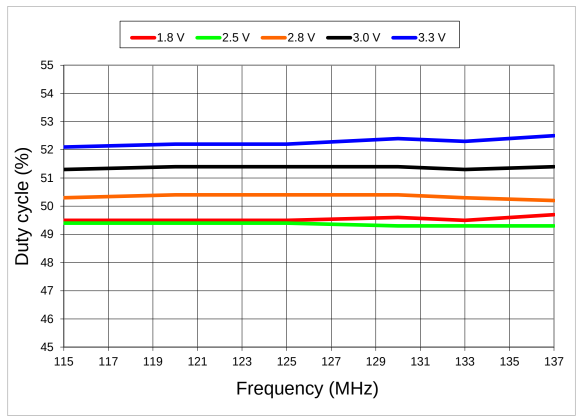


Figure 10. Duty Cycle vs Frequency

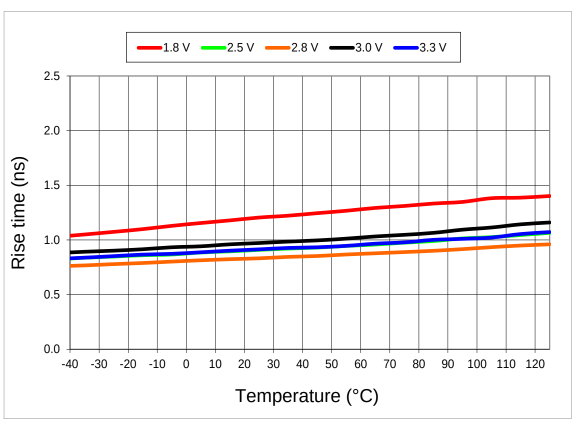


Figure 11. 20%-80% Rise Time vs Temperature

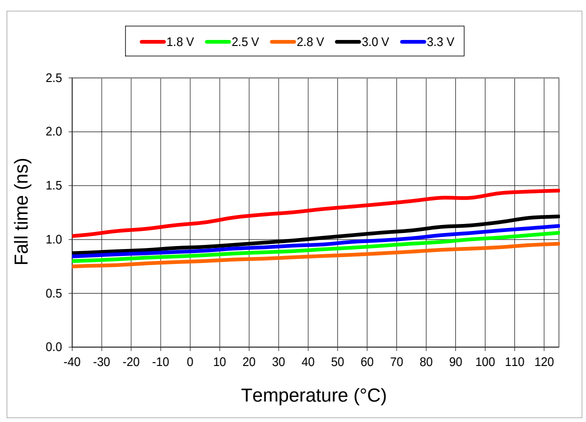


Figure 12. 20%-80% Fall Time vs Temperature

Performance Plots[8]

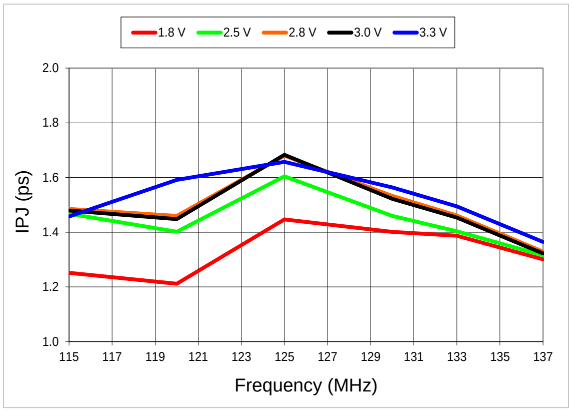


Figure 13. RMS Integrated Phase Jitter Random (12 kHz to 20 MHz) vs Frequency[9]

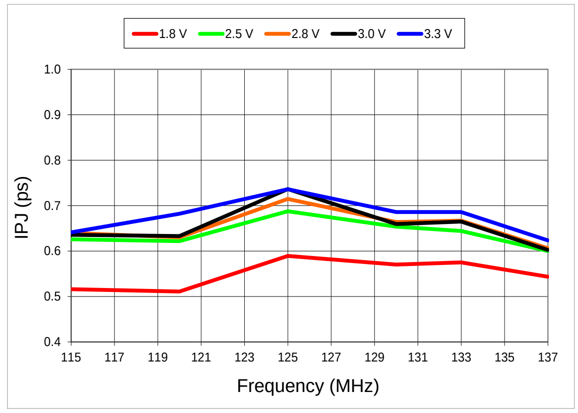


Figure 14. RMS Integrated Phase Jitter Random (900 kHz to 20 MHz) vs Frequency[9]

Notes:

8. All plots are measured with 15 pF load at room temperature, unless otherwise stated.
9. Phase noise plots are measured with Agilent E5052B signal source analyzer.

Programmable Drive Strength

The SiT8945 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time.
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the SiTime Application Notes section.

EMI Reduction by Slowing Rise/Fall Time

Figure 15 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

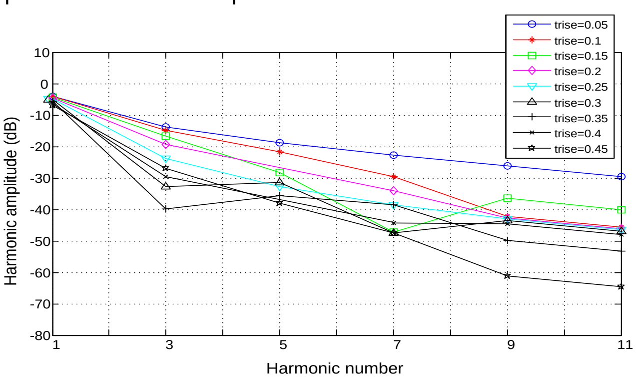


Figure 15. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the Rise/Fall Time Tables (Table 7 to Table 11) to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V SiT8945 device with default drive strength setting, the typical rise/fall time is 0.46 ns for 5 pF output load. The typical rise/fall time slows down to 1 ns when the output load increases to 15 pF. One can choose to speed up the rise/fall time to 0.72 ns by then increasing the driven strength setting on the SiT8945 to "F".

The SiT8945 can support up to 30 pF in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the Rise/Tall Time Tables (Table 7 to 11) to determine the proper drive strength for the desired combination of output load vs. rise/fall time.

SiT8945 Drive Strength Selection

Tables 7 through 11 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the SiT8945 nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V)
2. Select the capacitive load column that matches the application requirement (5 pF to 30 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 7 through 11, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max Frequency} = \frac{1}{5 \times \text{Trf\_20/80}}$$

where Trf_20/80 is the typical value for 20%-80% rise/fall time.

Example 1

Calculate f_{MAX} for the following condition:

- Vdd = 3.3V (Table 11)
- Capacitive Load: 30 pF
- Desired Tr/f time = 1.46 ns (rise/fall time part number code = U)

Part number for the above example:

SiT8945BM**E**12-18EA137.000000

Drive strength code is inserted here. Default setting is "-"

Rise/Fall Time (20% to 80%) vs C_{LOAD} Tables

Table 7. Vdd = 1.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)		
Drive Strength\ C_{LOAD}	**5 pF**	**15 pF**
T	0.93	n/a
E	0.78	n/a
U	0.70	1.48
F or "-": default	0.65	1.30

Table 8. Vdd = 2.5V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)		
Drive Strength \ C_{LOAD}	**5 pF**	**15 pF**
R	1.45	n/a
B	1.09	n/a
T or "-": default	0.62	1.28
E	0.54	1.00
U	0.43	0.96
F	0.34	0.88

Table 9. Vdd = 2.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)			
Drive Strength \ C_{LOAD}	**5 pF**	**15 pF**	**30 pF**
R	1.29	n/a	n/a
B	0.97	n/a	n/a
T or "-": default	0.55	1.12	n/a
E	0.44	1.00	n/a
U	0.34	0.88	n/a
F	0.29	0.81	1.48

Table 10. Vdd = 3.0V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)			
Drive Strength \ C_{LOAD}	**5 pF**	**15 pF**	**30 pF**
R	1.22	n/a	n/a
B	0.89	n/a	n/a
T or "-": default	0.51	1.00	n/a
E	0.38	0.92	n/a
U	0.30	0.83	n/a
F	0.27	0.76	1.39

Table 11. Vdd = 3.3V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)			
Drive Strength \ C_{LOAD}	**5 pF**	**15 pF**	**30 pF**
R	1.16	n/a	n/a
B	0.81	n/a	n/a
T or "-": default	0.46	1.00	n/a
E	0.33	0.87	n/a
U	0.28	0.79	1.46
F	0.25	0.72	1.31

Note:

10. "n/a" indicates that the resulting rise/fall time from the respective combination of the drive strength and output load does not provide rail-to-rail swing and is not available.

Pin 1 Configuration Options (OE or NC)

Pin 1 of the SiT8945 can be factory-programmed to support two modes: Output Enable (OE) or No Connect (NC). These modes can also be programmed with the Time Machine II using Field Programmable Oscillators.

Output Enable (OE) Mode

In the OE mode, applying logic low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in <1µs.

No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and outputs the specified frequency regardless of the logic level on pin 1.

Table 12 below summarizes the key relevant parameters in the operation of the device in OE or NC mode.

Table 12. OE vs. NC

	OE	NC
Active current 125 MHz (max, 1.8V)	6 mA	6 mA
OE disable current (max. 1.8V)	4 mA	N/A
OE enable time at 110 MHz (max)	130 ns	N/A
Output driver in OE disable	High Z	N/A

Output on Startup and OE Enable

The SiT8945 comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup.

In addition, the SiT8945 supports "no runt" pulses and "no glitch" output during startup or when the output driver is reenabled from the OE disable mode as shown in the waveform captures in Figure 16 and Figure 17.

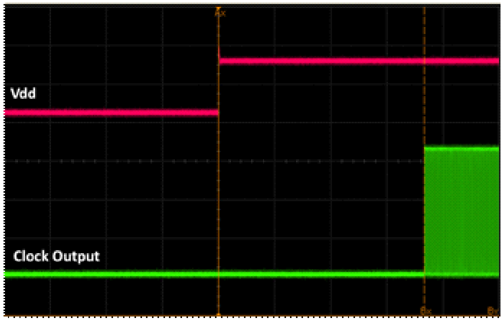


Figure 16. Startup Waveform vs. Vdd

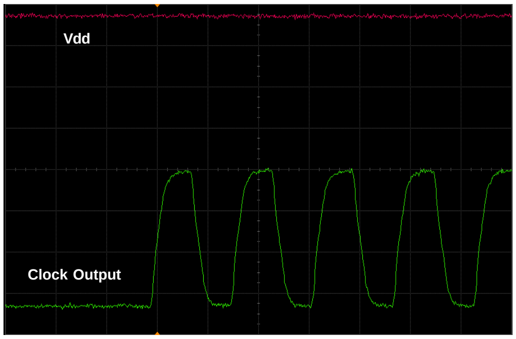
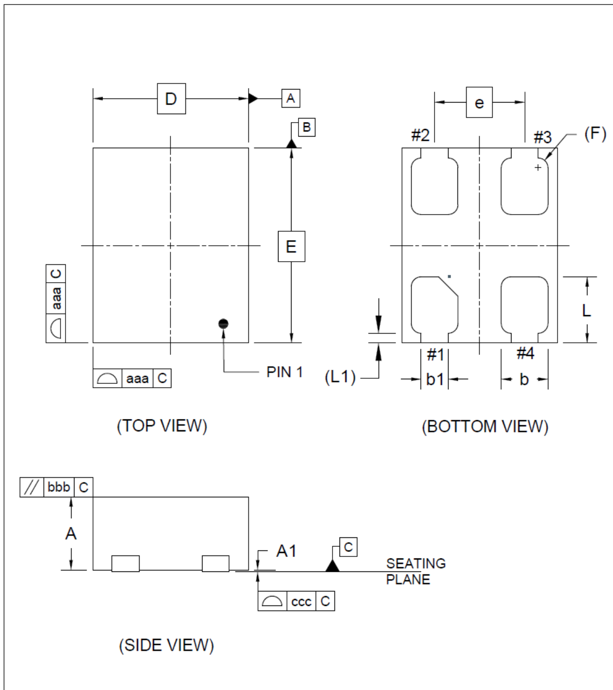


Figure 17. Startup Waveform vs. Vdd
(Zoomed-in View of Figure 16)

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[11] | **Recommended Land Pattern (Unit: mm)[12]**

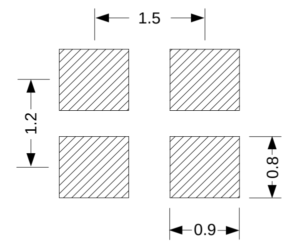
2.0 x 1.6 x 0.75 mm



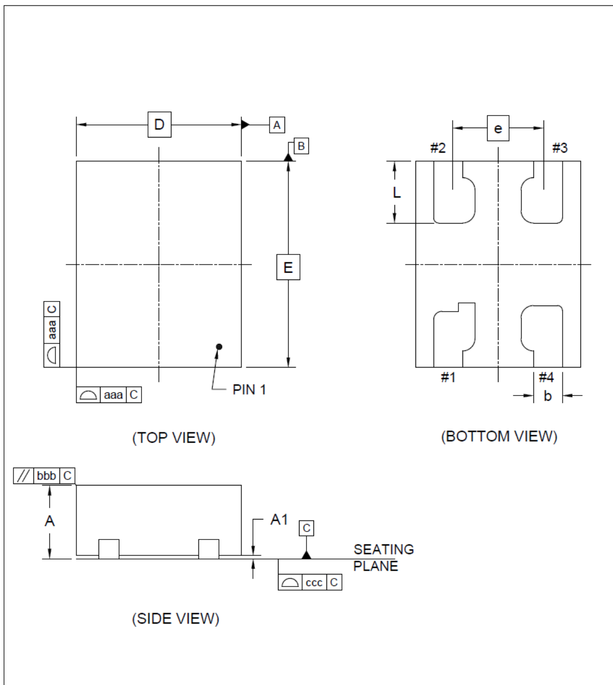
		SYMBOL	MIN	NOM	MAX
PACKAGE THICKNESS		A	0.700	0.750	0.800
STAND OFF		A1	0.000	0.020	0.050
BODY SIZE	X	D		1.600 BSC	
	Y	E		2.000 BSC	
LEAD WIDTH		b	0.430	0.480	0.530
		b1	0.230	0.280	0.330
LEAD LENGTH		L	0.580	0.680	0.780
		L1		0.100 REF	
LEAD PITCH		e		0.930 BSC	
RADIUS		F		0.100 REF	
PACKAGE TOLERANCE		aaa		0.050	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	

NOTES
1. Dimensioning and tolerance conform to ASME Y14.5-2009
2. All dimensions are in millimeters.

SiTime			
TITLE 4L PQFN		DWG NO.	
		POD-PQFN-004-X01620-026	
1.60x2.00x0.75 mm		REV.	SHEET
DATE	01-APR-2019	A02	1 OF 2



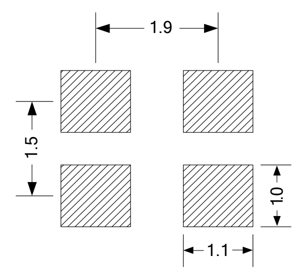
2.5 x 2.0 x 0.75 mm



		SYMBOL	MIN	NOM	MAX
PACKAGE THICKNESS		A	0.700	0.750	0.800
THICKNESS		A1	0.000	0.020	0.050
BODY SIZE	X	D		2.000 BSC	
	Y	E		2.500 BSC	
LEAD WIDTH		b	0.300	0.350	0.400
LEAD LENGTH		L	0.650	0.750	0.850
LEAD PITCH		e		1.250 BSC	
PACKAGE TOLERANCE		aaa		0.050	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	

NOTES
1. Dimensioning and tolerance conform to ASME Y14.5-2009
2. All dimensions are in millimeters.

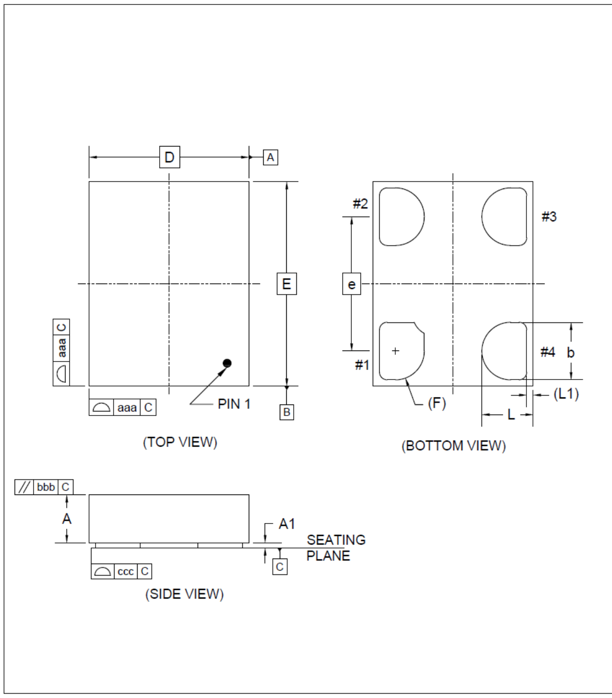
SiTime			
TITLE 4L PQFN		DWG NO.	
		POD-PQFN-004-X02025-010	
2.00x2.50x0.75 mm		REV.	SHEET
DATE	01-APR-2019	A02	1 OF 2



Dimensions and Patterns (continued)

Package Size – Dimensions (Unit: mm)[11]	Recommended Land Pattern (Unit: mm)[12]

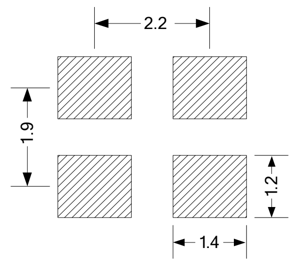
3.2 x 2.5 x 0.75 mm



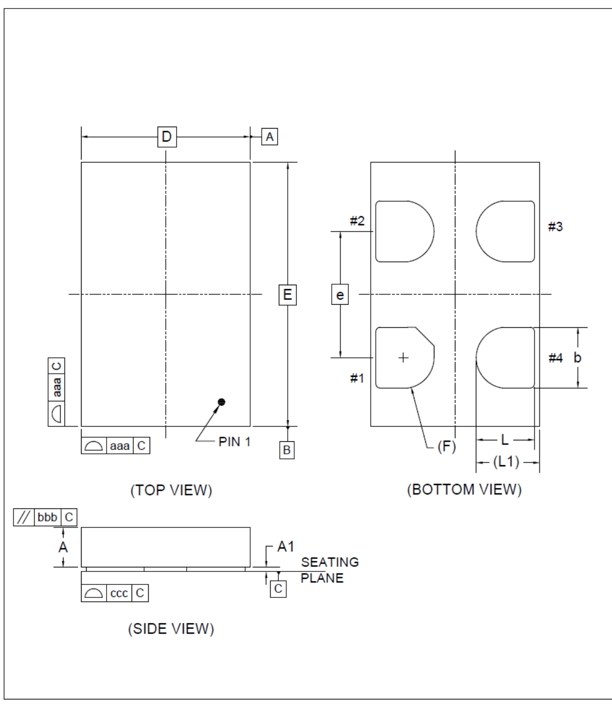
		SYMBOL	MIN	NOM	MAX
PACKAGE THICKNESS		A	0.700	0.750	0.800
STAND OFF		A1	0.000	0.020	0.050
BODY SIZE	X	D		2.500 BSC	
	Y	E		3.200 BSC	
LEAD WIDTH		b	0.800	0.900	1.000
LEAD LENGTH		L	0.700	0.800	0.900
		L1		0.100 REF	
LEAD PITCH		e		2.100 BSC	
RADIUS		F		0.450 REF	
		F1		0.120 REF	
PACKAGE TOLERANCE		aaa		0.050	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	

NOTES
1. Dimensioning and tolerance conform to ASME Y14.5-2009
2. All dimensions are in millimeters.

SiTime			
TITLE	4L PQFN	DWG NO.	
		POD-PQFN-004-X03225-002	
	3.20x2.50x0.75 mm	REV.	SHEET
DATE	01-APR-2019	A04	1 OF 2



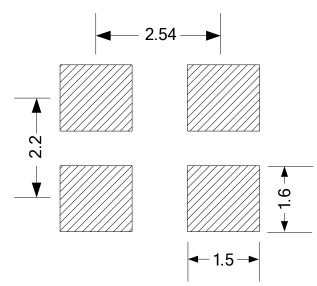
5.0 x 3.2 x 0.75 mm



		SYMBOL	MIN	NOM	MAX
PACKAGE THICKNESS		A	0.700	0.750	0.800
STAND OFF		A1	0.000	0.020	0.050
BODY SIZE	X	D		3.200 BSC	
	Y	E		5.000 BSC	
LEAD WIDTH		b	1.000	1.100	1.200
LEAD LENGTH		L	1.050	1.100	1.150
		L1		1.200 REF	
LEAD PITCH		e		2.390 BSC	
RADIUS		F		0.575	
PACKAGE TOLERANCE		aaa		0.050	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	

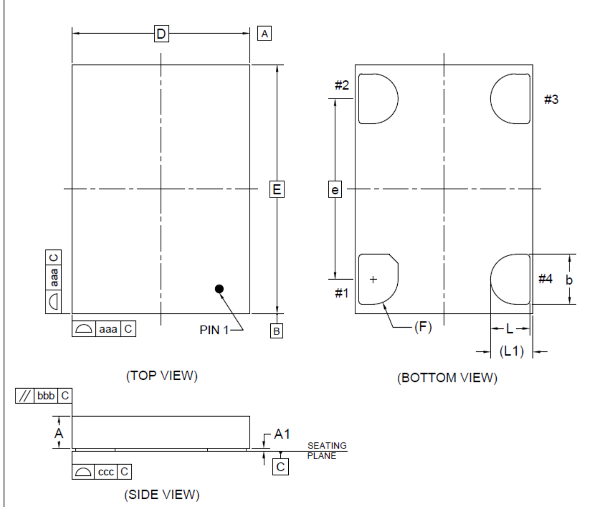
NOTES
1. Dimensioning and tolerance conform to ASME Y14.5-2009
2. All dimensions are in millimeters.

SiTime			
TITLE	4L PQFN	DWG NO.	
		POD-PQFN-004-X05032-003	
	5.00x3.20x0.75 mm	REV.	SHEET
DATE	01-APR-2019	A04	1 OF 2



Dimensions and Patterns (continued)

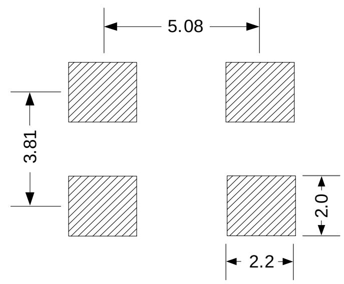
Package Size – Dimensions (Unit: mm)[11]	Recommended Land Pattern (Unit: mm)[12]
7.0 x 5.0 x 0.90 mm	



		SYMBOL	MIN	NOM	MAX
PACKAGE THICKNESS		A	0.800	0.900	1.000
STAND OFF		A1	0.000	0.020	0.050
BODY SIZE	X	D	5.000 BSC		
	Y	E	7.000 BSC		
LEAD WIDTH		b	1.350	1.400	1.450
LEAD LENGTH		L	1.050	1.100	1.150
		L1	1.200 REF		
LEAD PITCH		e	5.080 BSC		
RADIUS		F	0.080 REF		
PACKAGE TOLERANCE		aaa	0.050		
MOLD FLATNESS		bbb	0.100		
COPLANARITY		ccc	0.080		

NOTES
1. Dimensioning and tolerance conform to ASME Y14.5-2009
2. All dimensions are in millimeters.

SiTime			
TITLE 4L PQFN		DWG NO. POD-PQFN-004-X07050-011	
7.00x5.00x0.90 mm		REV.	SHEET
DATE	01-APR-2019	A02	1 OF 2



Notes:

11. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
12. A capacitor of value 0.1 µF or higher between Vdd and GND is required.

Ordering Information

The following part number guide is for reference only. To customize and build an exact part number, use the SiTime Part Number Generator.

SiT8945BA-12-18EA125.123456D

Part Family
"SiT8945"

Revision Letter
"B" is the revision

Temperature Range
"I" -40ºC to 85ºC, AEC-Q100 Grade3
"E" -40ºC to 105ºC, AEC-Q100 Grade2
"A" -40ºC to 125ºC, AEC-Q100 Grade1
"M" -55ºC to 125ºC, Ext. cold AEC-Q100 Grade1

Output Drive Strength
"–" Default (datasheet limits)
See Tables 7 to 11 for rise/fall times
"R" "E"
"B" "U"
"T" "F"

Package Size
"7" 2.0 x 1.6 mm
"1" 2.5 x 2.0 mm
"2" 3.2 x 2.5 mm
"3" 5.0 x 3.2 mm
"8" 7.0 x 5.0 mm

Packing Method
"T": 12 mm Tape & Reel, 3ku reel
"Y": 12 mm Tape & Reel, 1ku reel
"D": 8 mm Tape & Reel, 3ku reel
"E": 8 mm Tape & Reel, 1ku reel
Blank for Bulk

Frequency
Refer to the Supported Frequency Tables Below

Special Features
"A" for Low *g*-Sensitivity, 0.1 ppb/*g*

Feature Pin
"E" for Output Enable
"S" for Standby
"N" for No Connect

Supply Voltage[13]
"18" for 1.8V
"25" for 2.5V
"28" for 2.8V
"30" for 3.0V
"33" for 3.3V
"XX" for 2.5V -10% to 3.3V +10%

Frequency Stability
"1" for ±20 ppm
"2" for ±25 ppm
"8" for ±30 ppm
"3" for ±50 ppm

Note:

13. The voltage portion of the SiT8945 part number consists of two characters that denote the specific supply voltage of the device. The SiT8945 supports either 1.8V ±10% or any voltage between 2.25V and 3.63V. In the 1.8V mode, one can simply insert 18 in the part number. In the 2.5V to 3.3V mode, two digits such as 18, 25 or 33 can be used in the part number to reflect the desired voltage. Alternatively, "XX" can be used to indicate the entire operating voltage range from 2.25V to 3.63V.

Table 13. Supported Frequencies (-40°C to +85°C) [14]

Frequency Range	
Min.	**Max.**
115.200000 MHz	137.000000 MHz

Table 14. Supported Frequencies (-40°C to +105°C or -40°C to +125°C) [14, 15]

Frequency Range	
Min.	**Max.**
115.194001 MHz	117.810999 MHz
118.038001 MHz	118.593999 MHz
118.743001 MHz	122.141999 MHz
122.705001 MHz	123.021999 MHz
123.348001 MHz	137.000000 MHz

Table 15. Supported Frequencies (-55°C to +125°C) [14, 15]

Frequency Range	
Min.	**Max.**
119.342001 MHz	120.238999 MHz
120.262001 MHz	121.169999 MHz
121.243001 MHz	121.600999 MHz
123.948001 MHz	137.000000 MHz

Notes:

14. Any frequency within the min and max values in the above tables are supported with 6 decimal places of accuracy.
15. Please contact SiTime for frequencies that are not listed in the tables above.

Table 16. Ordering Codes for Supported Tape & Reel Packing Method

Device Size	16 mm T&R (3ku)	16 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	8 mm T&R (3ku)	8 mm T&R (1ku)
2.0 x 1.6 mm	–	–	–	–	D	E
2.5 x 2.0 mm	–	–	–	–	D	E
3.2 x 2.5 mm	–	–	–	–	D	E
5.0 x 3.2 mm	–	–	T	Y	–	–
7.0 x 5.0 mm	T	Y	–	–	–	–

Table 17. Revision History

Revision	Release Date	Change Summary
0.5	07/22/2019	First release

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