SiT7910

Endura™ Ruggedized 0.1 ppm, µPower, 32.768 kHz Super-TCXO

Features

- 32.768 kHz ±0.1 ppm frequency stability over temperature
- 30 ms drift over 7 days
- Operating temperature range up to -55°C to 105°C
- Benchmark frequency stability for faster GNSS signal acquisition
- Benchmark 32 kHz oscillator g-sensitivity
- Ultra-low power: 5.0 µA typical IDD
- 2.1 ns_{RMS} typical phase jitter
- Operating supply voltage range: 1.62 V to 3.63 V
- Pb-free, RoHS and REACH compliant

Applications

- Precision sleep timer
- RTC reference clock

TempFlat MEMS

Electrical Specifications

Conditions: Min/Max limits are over temperature, Vdd = 1.8 V ±10%, unless otherwise stated. Typical are at 25°C and Vdd = 1.8 V.

Table 1. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Output Frequency	Fout		32.768		kHz	
Operating Temperature Range						
Operating Temperature Range	Op_Temp	-40	-	85	°C	"I" temperature range ordering code
		-40	-	105	°C	"E" temperature range ordering code
		-55	-	105	°C	"L" temperature range ordering code
Initial Tolerance	F_tol	-1	-	1	ppm	Initial tolerance at 25°C after 2 reflows
Frequency Stability[1]	F_stab	-0.1	-	0.1	ppm	-40°C to 85°C, measured at 2°C/min including hysteresis Frequency stability code "Q" "I" temperature range code only Voltage ordering code: "18"
		-0.2	-	0.2		Measured at 2°C/min including hysteresis Frequency stability code "P" Voltage ordering code: "18"
		-0.4	-	0.4		Measured at 2°C/min including hysteresis Frequency stability code "L" Voltage ordering code: "18" and "YY"
Root Allen Variance	AD_10s	-	-	5e-8		1 and 10 second averaging time
7 day Aging	F_aging_7d	-0.1	-	0.1	ppm	T_A = 85°C, Vdd = 1.8 V, relative to initial frequency, after 2 days of continued operation. Aging is measured with respected to Day 3.
One-year Aging	F_aging_1y	-1.3	-	1.3	ppm	
20 Year Aging	F_aging_20y	-4	-	4	ppm	
***g*-sensitivity**	G_sen	-	-	20	ppb/*g*	Total gamma over 3 axes; 15 Hz to 2 kHz; 55g_{RMS} MIL-PRF-55310, computed per section 4.8.18.3.1.
Jitter and Frequency Response Performance						
Integrated Phase Jitter	IPJ	-	2.1	2.5	ns_{RMS}	Integration bandwidth = 100 Hz to 16.384 kHz, without noise.
		-	2.1	2.5	ns_{RMS}	Integration bandwidth = 100 Hz to 16.384 kHz. Inclusive of 50 mV peak-to-peak sinusoidal noise on Vdd. Noise frequency 10 kHz to 36 MHz.
		-	2.1	6.5	ns_{RMS}	Integration bandwidth = 100 Hz to 16.384 kHz. Inclusive of 50 mV peak-to-peak sinusoidal noise on Vdd. Noise frequency 100 Hz to 36 MHz, VDD ≥ 1.8 V
			2.1	9.0	ns_{RMS}	Integration bandwidth = 100 Hz to 16.384 kHz. Inclusive of 50 mV peak-to-peak sinusoidal noise on Vdd. Noise frequency 100 Hz to 36 MHz, VDD <1.8 V
RMS Period Jitter	PJ_{RMS}	-	2.5	4.0	ns_{RMS}	10,000 samples, per JEDEC standard 65B Peak-to-peak Period Jitter = ±3.79 * PJ_{RMS}

Table 1. Electrical Characteristics (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.62	1.8	1.98	V	Ordering Code “18”
		1.62	-	3.63	V	Ordering Code “YY”
Supply Current	Idd	-	5.0	6.0	µA	-40°C to 85°C, Vin = 1.8 V, no load
		-	5.0	6.7		-55°C to 105°C, Vin = 1.8 V, no load
		-	5.0	7.0		-55°C to 105°C, no load, “YY” voltage code
Start-up Time at Power-up	t_start	-	-	300	ms	Measured when supply reaches 90% of final Vdd to the first output pulse
Stabilization Time	T_stable	-	-	900	ms	Time between first output pulse to frequency accuracy ≤ ±0.1 ppm
Output Frequency Accuracy during Stabilization Time	F_stable	-100	-	100	ppm	
LVCMOS Output						
Output Rise/Fall Time	tr, tf	-	9	20	ns	10 – 90% Vdd, 15 pF load
Output Clock Duty Cycle	DC	45	-	55	%	
Output Voltage High	VOH	90%	-		Vdd	I_{OH} = -50 µA, 15 pF load
Output Voltage Low	VOL		-	10%	Vdd	I_{OL} = 50 µA, 15 pF load

Note:

1. Relative to 32.768 kHz, excludes initial tolerance. Includes frequency stability over temperature, Vdd, and 20% load variation. Tested with Agilent 53132A frequency counter. Measured with 10 s gate time for accurate frequency measurement.

Table 2. Pin Configuration

Pin	Symbol	I/O	Functionality
1	NC	Internal Test	Leave Floating. Do not connect to GND.
2	GND	Power Supply Ground	Connect to ground.
3	CLK out	OUT	Oscillator clock output. LVCMOS compatible logic.
4	Vdd	Power Supply	Vdd does not require external bypass/decoupling capacitor(s) on normal operating condition. SiT7910 includes on-chip filtering capacitors. 10-100 nF low ESR ceramic bypass capacitor may be recommended close to the Vdd pin under extreme noise on the supply, a 10-100 nF low ESR ceramic bypass capacitor may be recommended close to the Vdd pin.

2520 Ceramic (Top View)

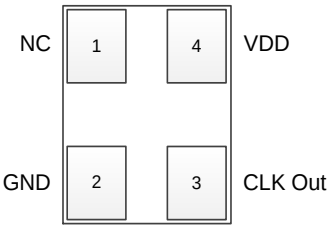


Figure 1. Pin Assignment

Table 3. Absolute Maximum Ratings

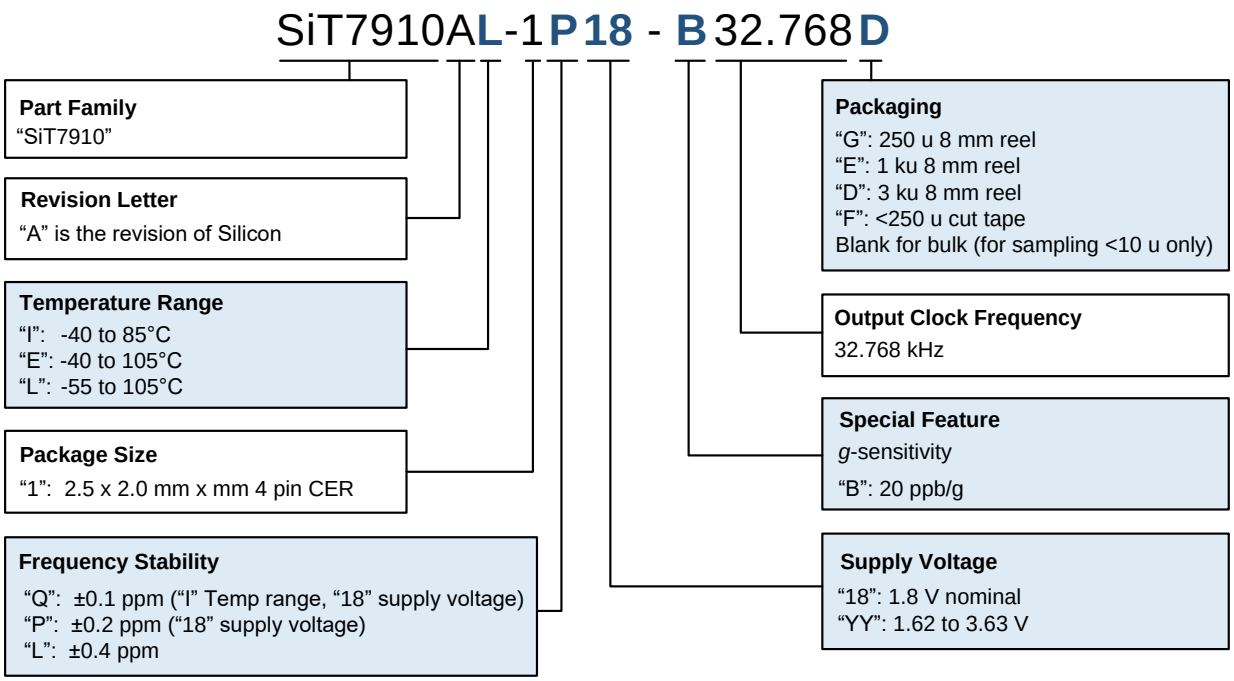
Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the electrical specifications, not at absolute maximum ratings.

Parameters	Test Conditions	Value	Unit
Continuous Power Supply Voltage Range (Vdd)	-	-0.5 to 3.63	V
Short Duration Maximum Power Supply Voltage (Vdd)	<30 minutes	4.0	V
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Charge-Device Model (CDM) ESD Protection	JESD22-C101	750	V
Latch-up Tolerance	JESD78 Compliant		
Storage Temperature	-	-65 to 110	°C
Altitude	-	-2,300 – 80,000	ft
Maximum Junction Temperature	-	150	°C

Table 4. Environmental Compliance

Parameters	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883, Method 2002	20,000	*g*
Mechanical Vibration Resistance	MIL-STD-883, Method 2007	70	*g*
Solderability	JESD22-B102		

Ordering Information



System Block Diagram

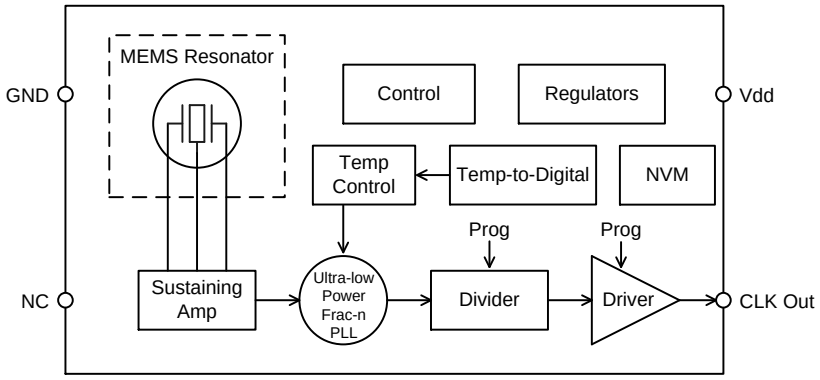


Figure 2. SiT7910 Block Diagram

Description

SiT7910 is an ultra-small, micro-power 32.768 kHz TCXO optimized for battery-powered, high precision applications. SiTime's silicon MEMS technology enables the first 32 kHz ±0.1 ppm TCXO in the world. Typical supply current is 5 µA under no load condition.

SiTime's MEMS oscillator consists of a MEMS resonator and a programmable mixed signal circuit. The SiT7910 MEMS resonator is built with SiTime's unique MEMS First® process. A key manufacturing step is EpiSeal® during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, SiTime's MEMS resonator die can be used like any other semiconductor die.

TCXO Frequency Stability

SiT7910 is factory calibrated (trimmed) over multiple temperature points to guarantee extremely tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point and with a -0.04 ppm/°C^2 temperature coefficient, the SiT7910 temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is a 32 kHz TCXO with extremely tight frequency variation of ±0.2 ppm over the -55°C to 105°C temperature range.

Typical Performance Plots

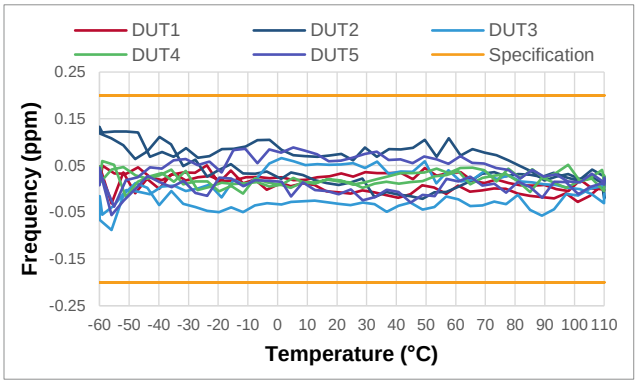


Figure 3. Frequency Stability vs. Temperature

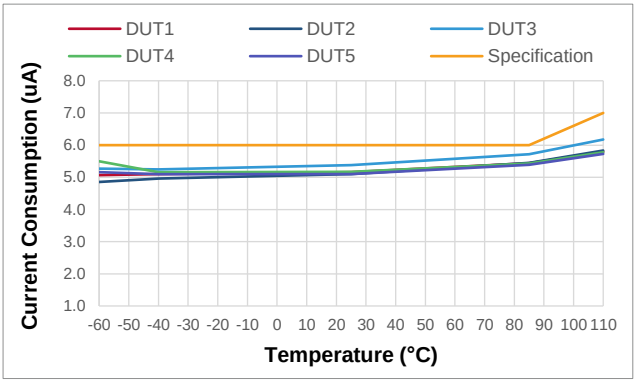


Figure 4. Supply Current vs. Temperature

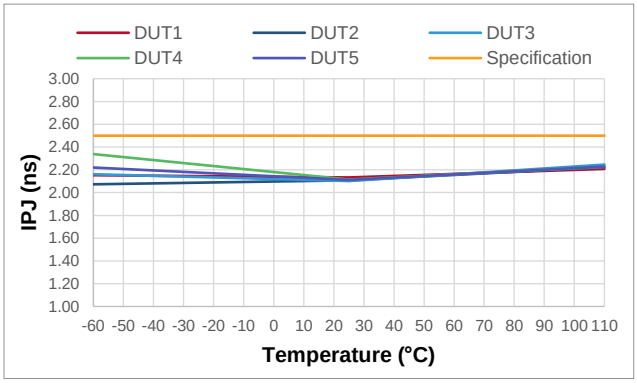
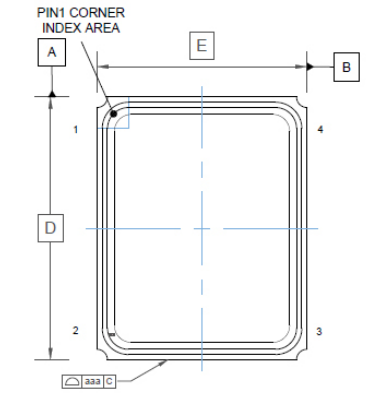
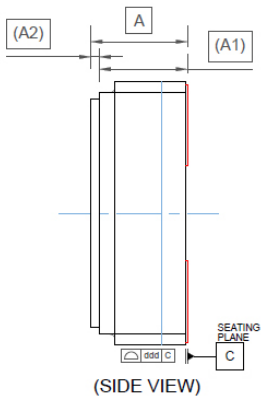


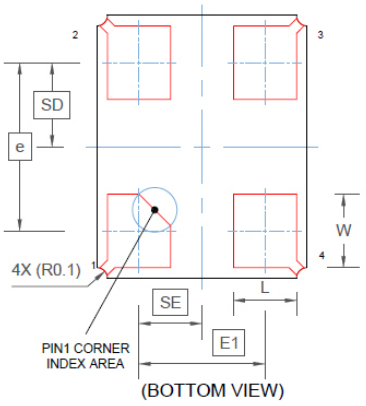
Figure 5. Integrated Phase Jitter vs. Temperature

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[2]







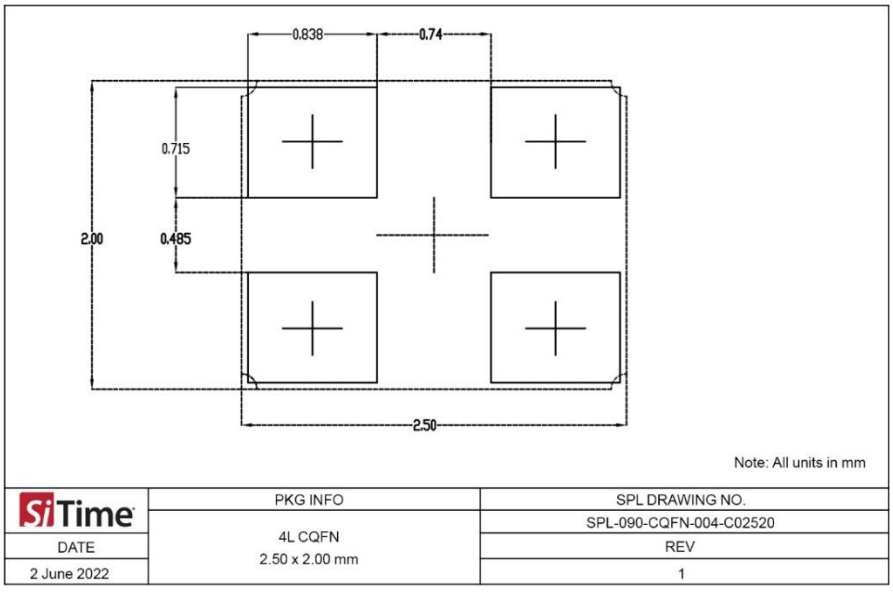
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.78	0.90	1.02
SUBSTRATE THK		A1		0.84 REF	
LID THICKNESS		A2		0.06 REF	
BODY SIZE	X	D		2.50 BSC	
	Y	E		2.00 BSC	
LEAD WIDTH		W	0.620	0.700	0.780
LEAD LENGTH		L	0.520	0.600	0.680
LEAD PITCH		e		1.60 BSC	
EDGE LEAD CENTER TO CENTER		E1		1.20 BSC	
BODY CENTER TO CONTACT LEAD		SD		0.80 BSC	
		SE		0.60 BSC	
PACKAGE TOLERNCE		aaa		0.08	

NOTE

1. ALL DIMENSION IN MM

PKG INFO	DRAWING NO.
4L CQFN 2.50x2.00x0.92 mm	POD-090-CQFN-004-X02520
	REV
DATE 25 Apr 2023	4

Recommended Land Pattern (Unit: mm)



PKG INFO	SPL DRAWING NO.
4L CQFN 2.50 x 2.00 mm	SPL-090-CQFN-004-C02520
	REV
DATE 2 June 2022	1

Note:

2. Lead finish is Electrolytic Ni: 1.27 – 8.89 um and Electrolytic Au: 0.3 – 0.8 um.

Manufacturing Guidelines

1. Refer to Manufacturing Guidelines for proper reflow profile and PCB cleaning recommendations to ensure best performance.
2. No Ultrasonic or Megasonic cleaning: Do not subject SiT7910 to an ultrasonic or megasonic cleaning environment. Permanent damage or long term reliability issues may occur.
3. Reflow profile, per JESD22-A113D.

Additional Information

Table 5. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Evaluation Boards	SiT6100EBB Evaluation Board User Manual	—
Demo Board	SiT6100DB Demo Board User Manual	Contact SiTime
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products
Qualification Reports	RoHS report, reliability reports, composition reports	Contact SiTime
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	Contact SiTime
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Revision History

Table 6. Revision History

Version	Release Date	Change Summary
0.9	2-Apr-2024	Evaluation board number correction

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