

SiT7201/2

10 MHz–220 MHz, ± 20 ppb, -159 dBc/Hz @ 10 kHz

Ultra-Low Phase Noise | Endura™ Ruggedized Precision Super-TCXO



Description

The SiT7201/2 are ± 20 ppb to ± 250 ppb precision Endura™ MEMS Super-TCXOs ideally optimized for ruggedized synchronization RF applications, such as secure radio, satellite, radar, and GNSS systems. The SiT7201 covers frequencies from 10 MHz to 60 MHz and the SiT7202 covers frequencies >60 MHz to 220 MHz.

The SiT7201/2 combines SiTime’s MEMS technology with a low-noise digital PLL to deliver:

- RF-quality phase noise
- Excellent dynamic stability in the presence of airflow and thermal excursions
- Extreme resistance to shock and vibration

Multiple on-chip regulators are included to filter power supply noise, eliminating the need for an external dedicated LDO.

The SiT7201/2 offer two device configurations for:

- 1) TCXO with non-pullable output frequency
- 2) DCTCXO enabling digital pulling of output frequency via an I²C/SPI interface with a resolution of 0.05 ppt (parts per trillion)

The SiT7201/2 are factory programmed for frequency, stability, voltage, and pull range, eliminating long lead times and customization costs associated with quartz devices. Refer to [Manufacturing Guideline](#) for proper reflow profile and PCB cleaning recommendations.



Features

- Any frequency from 10 MHz to 220 MHz
- Ultra-low Phase Noise -159 dBc/Hz (10 kHz) at 19.2 MHz
- Best dynamic stability under airflow, thermal shock
 - ± 20 ppb stability across temperature
 - ± 2 ppb/°C frequency slope (dF/dT)
 - 1e-11 ADEV at 10 seconds averaging time
 - 0.009 ppb/g max acceleration sensitivity
- -55°C to +125°C operating temperature range
- No activity dips or micro jumps
- Resistant to shock, vibration, and board bending
- On-chip regulators eliminate the need for external LDOs
- Digital frequency pulling (DCTCXO) via I²C/SPI
 - Digital control of output frequency and pull range
 - Up to ± 400 ppm pull range
 - Frequency pull resolution down to 0.05 ppt (5e-14)
- 1.8 V to 3.3 V supply voltage
- LVC MOS (SiT7201/2) or clipped sinewave (SiT7201) output
- RoHS and REACH compliant
- Pb-free, Halogen-free, Antimony-free

Applications

- Ruggedized radios
- RF upconverters and downconverters
- Radar, satellite, microwave equipment
- GPS, GNSS systems
- SATCOM
- Military, defense, space, avionics systems

Block Diagram

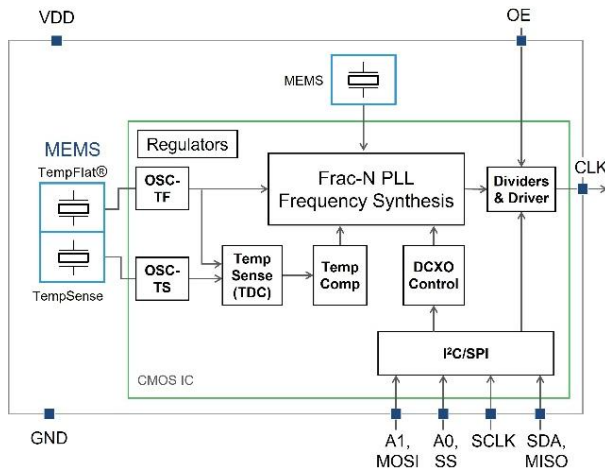


Figure 1. SiT7201/2 Block Diagram

5.0 mm x 3.5 mm Package Pinout

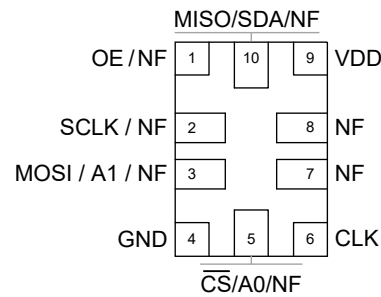
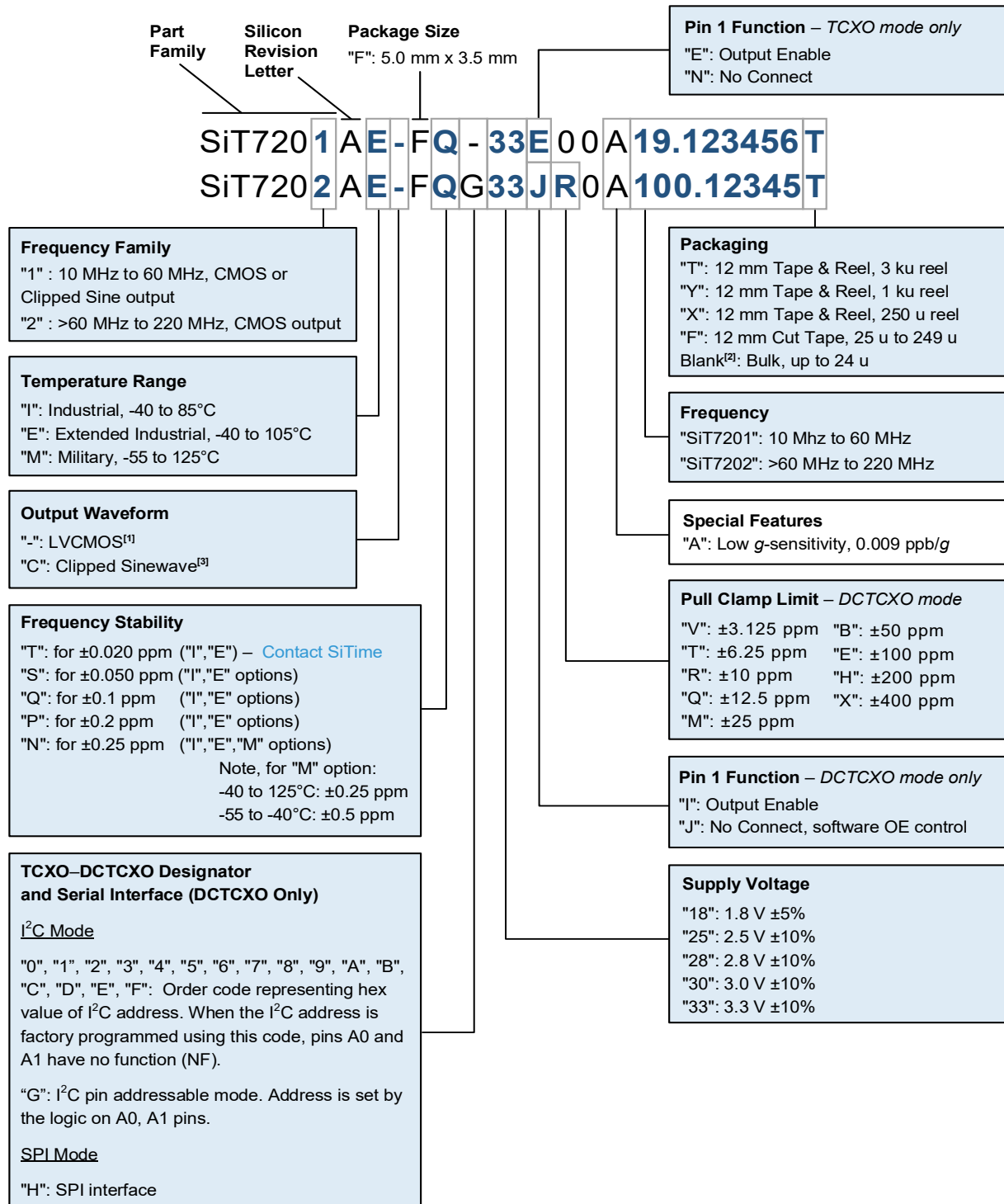


Figure 2. Pin Assignments (Top view)
(Refer to [Table 11](#) for Pin Descriptions)

Ordering Information

The part number guide illustrated below is for reference only, in which **blue** boxes identify order codes having more than one option.



Notes:

- "-" corresponds to the default rise/fall time for LVCMOS output as specified in [Table 1](#) (Electrical Characteristics). [Contact SiTime](#) for other rise/fall time options for best EMI or driving multiple loads. For differential outputs, [contact SiTime](#).
- Bulk is available for sampling only.
- [Contact SiTime](#) for Availability.

Table Of Contents

Description	1
Features.....	1
Applications	1
Block Diagram	1
5.0 mm x 3.5 mm Package Pinout	1
Ordering Information.....	2
Electrical Characteristics.....	4
Device Configurations and Pin-outs.....	9
Typical Performance Plots	10
Test Circuit Diagrams for LVCMOS and Clipped Sinewave Outputs	11
Waveforms.....	13
Timing Diagrams.....	14
Stability Diagrams	14
Dimensions and Patterns.....	15
Additional Information	16
Elite RF Digital Control Guide	17
Introduction.....	17
Register Map	17
SPI Usage Notes	18
Using the DCXO Function	19
Pull Range, Absolute Pull Range.....	19
DCTCXO-Specific Design Considerations.....	20
Pull Range and Absolute Pull Range.....	20
Output Frequency	20
Using the TDC Information	22
Revision History.....	23

Electrical Characteristics

All Min and Max limits are specified over the rated temperature and operating voltage with 8 pF output load unless otherwise stated. Typical values are at 25°C and 3.3 V V_{dd}.

Table 1. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Nominal Output Frequency Range	F _{nom}	10	–	220	MHz	
Temperature Range						
Operating Temperature Range	T _{use}	-40	–	+85	°C	Industrial "I"
		-40	–	+105		Extended Industrial "E"
		-55	–	+125		Military "M"
Rugged Characteristics						
Acceleration (g) Sensitivity, Gamma Vector	F _g	–	±0.004	±0.009	ppb/g	Total gamma over 3 axes; 15 Hz to 2 kHz; MIL-PRF-55310, computed per section 4.8.18.3.1
Frequency Stability – 0.020 ppm, 0.050 ppm, 0.1 ppm, Industrial and Extended Industrial Temp Ranges						
Frequency Stability over Temperature	F _{stab}	–	±0.005	±0.020 ±0.050 ±0.1	ppm	Temp Ranges: "I" -40°C to +85°C, "E" -40°C to +105°C Referenced to (max frequency + min frequency)/2 over the rated temperature range, in TCXO or DCTCXO
Initial Tolerance	F _{init}	–	±0.01	±0.3	ppm	Initial frequency at 25°C at 48 hours after 2 reflows
Supply Voltage Variation	F _{Vdd}	–	±2	±4	ppb	V _{dd} ±5%
Output Load Sensitivity	F _{load}	–	±0.4	–	ppb	SiT7201: LVCMOS output, 8 pF ±10%. Clipped sinewave output, 10 kΩ 10 pF ±10%
		–	±1.5	–	ppb	SiT7202: LVCMOS output, 8 pF ±10%.
Frequency vs. Temperature Slope	dF/dT	–	±2	±2.5	ppb/°C	1°C/min temperature ramp rate
Dynamic Frequency Change during Temperature Ramp	F _{dynamic}	–	±0.033	±0.042	ppb/s	1°C/min temperature ramp rate
24-hour holdover stability	F _{24_Hold}	–	–	±0.11	ppm	Inclusive of frequency variation due to temperature, ±10% supply variation, ±0.8 pF load variation and 24-hour aging
Hysteresis Over Temperature	F _{hys}	–	±5	±10	ppb	1°C/min ramp rate, defined as ±dF/2 as shown in Figure 18
One-Day (24-hr) Aging	F _{1d}	–	±0.2	–	ppb	At 50°C, after 30-days of continued operation. Aging is measured with respect to day 31
One-Year Aging	F _{1y}	–	±40	–	ppb	At 50°C, after 2-days of continued operation. Aging is measured with respect to day 3
10-Year Aging	F _{10y}	–	±50	–		
20-Year Aging	F _{20y}	–	±70	–		
20-Year Total Stability	F _{tot_20y}	–	±0.087	–	ppm	SiT7201 ±0.020 ppm option
		–	±0.089	–		SiT7202 ±0.020 ppm option
Allan deviation	ADEV	–	1e-11	–	–	10 second averaging time ^[4]

Table 1. Output Characteristics (continued)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Stability – 0.2 ppm and 0.25 ppm Industrial, Extended Industrial, and Military Temp Ranges						
Frequency Stability over Temperature	F_stab	–	±0.01	±0.2	ppm	Temp Ranges: "I" -40°C to +85°C, "E" -40°C to +105°C Referenced to (max frequency + min frequency)/2 over the rated temperature range
			±0.02	±0.25	ppm	Temp Ranges: "I" -40°C to +85°C, "E" -40°C to +105°C
		–	±0.02	±0.25 ±0.5	ppm	Temp Range: "M" -55°C to +125°C only offered in ±0.25 ppm option. -40°C to +125°C = ±0.25 ppm -55°C to -40°C = ±0.50 ppm Referenced to (max frequency + min frequency)/2 over the rated temperature range.
Initial Tolerance	F_init	–	±0.08	±1	ppm	Initial frequency at 25°C at 48 hours after 2 reflows
Supply Voltage Variation	F_Vdd	–	±2.5	±5	ppb	Vdd ±5%
Output Load Sensitivity	F_load	–	±4.5	–	ppb	LVC MOS output, 8 pF ±10%. Clipped sinewave output (SiT7201 only), 10 kΩ 10 pF ±10%
Frequency vs. Temperature Slope	dF/dT	–	±6.4	±10	ppb/°C	
Dynamic Frequency Change during Temperature Ramp	F_dynamic	–	±0.11	±0.17	ppb/s	1°C/min temperature ramp rate
Hysteresis Over Temperature	F_hys	–	±5	±10	ppb	1°C/min ramp rate, defined as ±dF/2 as shown in Figure 18
24-hour holdover stability	F_24_Hold	–	–	±0.22	ppm	Inclusive of frequency variation due to temperature, ±10% supply variation, ±0.8 pF load variation and 24-hour aging
One-Day (24-hr) Aging	F_1d	–	–	±3	ppb	At 50°C, after 30-days of continued operation. Aging is measured with respect to day 31
One-Year Aging	F_1y	–	±1	–	ppm	At 50°C, after 2-days of continued operation. Aging is measured with respect to day 3
10-Year Aging	F_10y	–	±0.20	–	ppm	
20-Year Aging	F_20y	–	±0.28	–	ppm	
20-Year Total Stability	F_tot_20y	–	±0.377	–	ppm	0.2 ppm, SiT7201/SiT7202
		–	±0.387	–		0.25 ppm, SiT7201/SiT7202
Allan Deviation	ADEV	–	1e-11	–	–	10 second averaging time ⁽⁴⁾
LVC MOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	0.3	0.6	2	ns	20% to 80% Vdd
Output Voltage High	VOH	80%	–	–	Vdd	IOH = +3 mA
Output Voltage Low	VOL	–	–	4%	Vdd	IOL = -3 mA
Output Impedance	Z_out_c	–	20	–	Ohms	Impedance looking into output buffer, Vdd = 3.3 V
		–	20	–	Ohms	Impedance looking into output buffer, Vdd = 2.5 V
		–	20	–	Ohms	Impedance looking into output buffer, Vdd = 1.8 V
Clipped Sinewave Output Characteristics						
Output Voltage Swing	V_out	0.8	–	1.2	V	Clipped sinewave output, 10 kΩ 10 pF ±10%
Rise/Fall Time	Tr, Tf	15%	–	25%	1/F_nom	20% to 80% Vdd
Start-up Characteristics						
Start-up Time	T_start	–	5	10	ms	Time to first pulse, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 100 µs from 0 V to Vdd
Output Enable Time	T_oe	–	–	400	ns	SiT7201: F_nom = 10 MHz
		–	–	125	ns	SiT7202: F_nom = 122.8 MHz
Time to Rated Frequency Stability	T_stability	–	10	–	ms	Time to first accurate pulse within rated stability, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 100 µs
OE Disable Characteristics						
Time to Disable from OE Pin	T_od	–	–	200	ns	SiT7201: F_nom = 10 MHz
		–	–	110		SiT7202: F_nom = 122.8 MHz

Note:

4. Measured 2 hours after startup in a temperature chamber with a constant temperature in still air.

Table 2. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	Vdd	1.71	1.8	1.89	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.70	3.0	3.30	V	
		2.97	3.3	3.63	V	
Current Consumption						
Current Consumption	Idd	–	80	90	mA	SiT7201: F _{nom} = 19.2 MHz, No Load, TCXO and DCTCXO modes
		–	92	110	mA	SiT7202: F _{nom} = 122.8 MHz, No Load, TCXO and DCTCXO modes
OE Disable Current	I _{od}	–	78	88	mA	OE = GND, output weakly pulled down. TCXO, DCTCXO

Table 3. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics – OE Pin						
Input Impedance	Z _{in}	75	–	–	kΩ	Internal pull up to Vdd
Input High Voltage	VIH	70%	–	–	Vdd	
Input Low Voltage	VIL	–	–	30%	Vdd	
Frequency Tuning Range – I²C (DCTCXO) modes						
Pull Range	PR	±400	–	–	ppm	DCTCXO mode
Absolute Pull Range ⁵⁾	APR	±399.53	–	–	ppm	±0.1 ppm F _{stab} , DCTCXO for PR = ±400 ppm
		±399.43	–	–	ppm	±0.2 ppm F _{stab} , DCTCXO for PR = ±400 ppm
		±399.38	–	–	ppm	±0.25 ppm F _{stab} , DCTCXO for PR = ±400 ppm
Frequency Pull Clamp Limit ⁶⁾	PC _L	±3.125, ±6.25, ±10, ±12.5, ±25, ±50, ±100, ±200, ±400			ppm	DCTCXO mode
I²C Interface Characteristics, 200 Ohm, 550 pF (Max I²C Bus Load), DCTCXO mode						
Bus Speed	F _{I2C}	≤ 1000			kHz	SDA capacitance <20 pF
		≤ 400				SDA capacitance <50 pF
		≤ 100				SDA capacitance <165 pF
Input Voltage Low	VIL _{I2C}	–	–	30%	Vdd	
Input Voltage High	VIH _{I2C}	70%	–	–	Vdd	
Output Voltage Low	VOL _{I2C}	–	–	10%	Vdd	
Output Voltage High	VOH _{I2C}	90%	–	–	Vdd	
Input Leakage current	I _L	0.5	–	24	μA	0.1 V _{DD} < V _{OUT} < 0.9 V _{DD} . Includes typical leakage current from 200 kΩ pull resistor to VDD.
Input Capacitance	C _{IN}	–	5	–	pF	
Aggregate Pull-Up Impedance	Z _{PU}	5	–	–	kΩ	
SPI Interface Characteristics, DCTCXO mode						
Bus Speed	F _{SPI}	≤5000			kHz	MISO capacitance < 15 pF
		≤1000				MISO capacitance < 50 pF
Input Voltage Low	VIL _{SPI}	–	–	10%	Vdd	
Input Voltage High	VIH _{SPI}	90%	–	–	Vdd	
Output Voltage Low	VOL _{SPI}	–	–	10%	Vdd	IOL = 2.7 mA (Vdd = 2.5 V)
Output Voltage High	VOH _{SPI}	90%	–	–	Vdd	IOH = 2.2 mA (Vdd = 2.5 V)
Input Capacitance	C _{SPIIN}	–	5	–	pF	
Leakage in High Impedance Mode	I _{SPI L}	0.5	–	24	μA	0.1 V _{DD} < V _{OUT} < 0.9 V _{DD} .

Notes:

- APR = PR – initial tolerance – 20-year aging – frequency stability over temperature.
- Clamp limit is specified at time of order, which prevents pulling the frequency beyond the specified value.

Table 4. Jitter & Phase Noise – LVCMOS

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	80	–	fs	F_nom = 19.2 MHz, Integration bandwidth = 12 kHz to 5 MHz
RMS Period Jitter	T_jitt_per	–	1	–	ps	F_nom = 19.2 MHz, measured per JESD65B
Peak Cycle-to-Cycle Jitter	T_jitt_cc	–	6	–	ps	F_nom = 19.2 MHz, measured per JESD65B
Phase Noise (SiT7201)						
1 Hz offset		–	-84	–	dBc/Hz	F_nom = 19.2 MHz TCXO and DCTCXO modes
10 Hz offset		–	-113	–	dBc/Hz	
100 Hz offset		–	-135	–	dBc/Hz	
1 kHz offset		–	-145	–	dBc/Hz	
10 kHz offset		–	-159	–	dBc/Hz	
100 kHz offset		–	-170	–	dBc/Hz	
1 MHz offset		–	-171	–	dBc/Hz	
5 MHz offset		–	-172	–	dBc/Hz	
Spurious	T_spur	–	-105	–	dBc	F_nom = 19.2 MHz, 1 kHz to 5 MHz offsets, 8 pF ±10%
Phase Noise (SiT7202)						
1 Hz offset		–	-68	–	dBc/Hz	F_nom = 122.8 MHz TCXO and DCTCXO modes
10 Hz offset		–	-97	–	dBc/Hz	
100 Hz offset		–	-116	–	dBc/Hz	
1 kHz offset		–	-131	–	dBc/Hz	
10 kHz offset		–	-142	–	dBc/Hz	
100 kHz offset		–	-153	–	dBc/Hz	
1 MHz offset		–	-153	–	dBc/Hz	
5 MHz offset		–	-161	–	dBc/Hz	
10 MHz offset		–	-166	–	dBc/Hz	
20 MHz offset		–	-170	–	dBc/Hz	
Spurious	T_spur	–	-93	–	dBc	F_nom = 122.8 MHz, 1 kHz to 20 MHz offsets, 8 pF ±10%
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ⁽⁷⁾	PSJS	–	0.2	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-70	–	dBc	19.2 MHz, 50 mV peak-peak ripple on VDD

Table 5. Jitter & Phase Noise – Clipped Sinewave

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	100	–	fs	F_nom = 19.2 MHz, Integration bandwidth = 12 kHz to 5 MHz
Phase Noise						
1 Hz offset		–	-84	–	dBc/Hz	F_nom = 19.2 MHz TCXO and DCTCXO modes
10 Hz offset		–	-113	–	dBc/Hz	
100 Hz offset		–	-135	–	dBc/Hz	
1 kHz offset		–	-140	–	dBc/Hz	
10 kHz offset		–	-155	–	dBc/Hz	
100 kHz offset		–	-164	–	dBc/Hz	
1 MHz offset		–	-165	–	dBc/Hz	
5 MHz offset		–	-165	–	dBc/Hz	
Spurious	T_spur	–	-105	–	dBc	F_nom = 19.2 MHz, 1 kHz to 5 MHz offsets, 10 pF ±10%
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ⁽⁷⁾	PSJS	–	0.1	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-70	–	dBc	SiT7201 : 19.2 MHz, 50 mV peak-peak ripple on VDD

Note:

- Terminology chosen for clarity; referred to historically as power-supply noise rejection (PSNR).

Table 6. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Value	Unit
Storage Temperature		-65 to 150	°C
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 4	V
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C
Junction Temperature ^[8]		150	°C
Input Voltage, Maximum	Any input pin	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	V

Note:

- Exceeding this temperature for an extended period of time may damage the device.

Table 7. Thermal Considerations^[9]

Package	θ_{JA} ^[10] (°C/W)	θ_{JB} , Board (°C/W)	θ_{JC} , Top (°C/W)	Ψ_{JT} ^[8] (°C/W)
Ceramic 5.0 mm x 3.5 mm	61	11	34	12

Notes:

- Simulated in still air. Refer to [SiTime Application Note AN23033](#) for more information on thermal considerations
- Devices soldered on a JESD51 2s2p compliant board.

Table 8. Maximum Operating Junction Temperature^[11]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	85°C
85°C	100°C
105°C	120°C
125°C	140°C

Note:

- Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 9. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	20,000	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	g
Ambient Pressure	MIL-STD-202 TM 105 Condition C	70,000	ft
Temperature Cycle	JESD22, Method A104	–	–
Solderability	MIL-STD-883F, Method 2003	–	–
Moisture Sensitivity Level	MSL1 @260°C	–	–

Device Configurations and Pin-outs

Table 10. Device Configurations

Configuration	Pin 1	Pin 2	Pin 3	Pin 5	Pin 10	I ² C and SPI Programmable Parameters
TCXO	OE / NF	NF	NF	NF	NF	–
DCTCXO	OE / NF	SCLK	A1	A0	SDA	I ² C: Frequency Pull Range, Frequency Pull Value, Output Enable control
	OE / NF	SCLK	MOSI	\overline{SS} / NF	MISO	SPI: Frequency Pull Range, Frequency Pull Value, Output Enable control

Pin-outs (Top View)

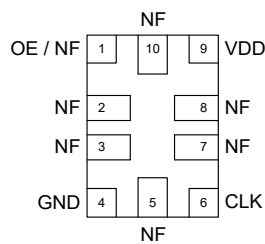


Figure 3. TCXO

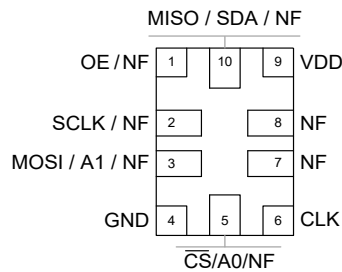


Figure 4. DCTCXO

Table 11. Pin Description

Pin	Symbol	I/O	Internal Pull-up/Pull Down Resistor	Function
1	OE / NF	OE – Input	100 kΩ Pull-Up	H ^[12] : specified frequency output L: output is high impedance. Only output driver is disabled
		NF ^[13] – No Function	–	H or L or Open: No effect on output frequency or other device functions
2	SCLK / NF ^[13]	SCLK – Input	200 kΩ Pull-Up	I ² C/SPI serial clock input
		No Function	–	H or L or Open: No effect on output frequency or other device functions
3	MOSI / A1 / NF ^[13]	MOSI – Input	100 kΩ Pull-Up	SPI serial data input
		A1 – Input	100 kΩ Pull-Up	I ² C address, most significant bit (MSB), when address is selected via pins.
		No Function	–	H or L or Open: No effect on output frequency or other device functions
4	GND	Power	–	Connect to ground
5	\overline{CS} / A0 / NF ^[13]	CS – SPI Chip Select	100 kΩ Pull-Up	SPI Chip select, active low
		A0 – Input	100 kΩ Pull-Up	I ² C address, least significant bit (LSB), when address is selected via pins. This pin is NF when I ² C device address is specified in the ordering code. \overline{CS} is SPI chip select, active low
		NF – No Function	–	H or L or Open: No effect on output frequency or other device functions.
6	CLK	Output	–	LVC MOS, or clipped sinewave oscillator output
7	NF ^[13]	No Function	–	H or L or Open: No effect on output frequency or other device functions
8	NF ^[13]	No Function	–	H or L or Open: No effect on output frequency or other device functions
9	VDD	Power	–	Connect to power supply. A 0.1 μF capacitor in parallel with a 10 μF capacitor are required between VDD and GND. The 0.1 μF capacitor is recommended to place close to the device, and place the 10 μF capacitor less than 2 inches away.
10	MISO / SDA / NF ^[13]	MISO – Output	–	SPI serial data output
		SDA – Input/Output	200 kΩ Pull Up	I ² C Serial Data
		NF – No Function	–	H or L or Open: No effect on output frequency or other device functions

Notes:

12. In OE mode for noisy environments, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NF option.
13. All NF pins can be left floating and do not need to be soldered down.
14. Vias from the GND pins to the GND plane should be maximized.

Typical Performance Plots

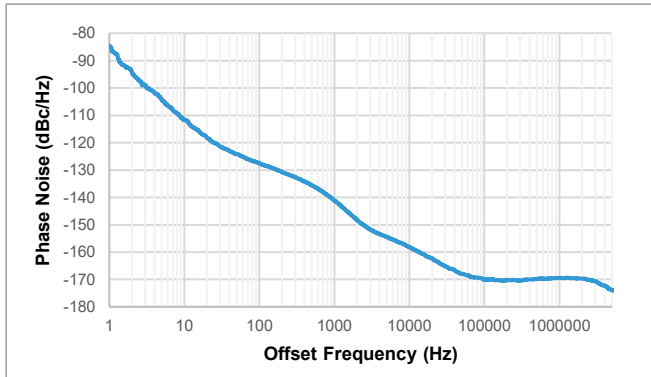


Figure 5. Phase Noise – 19.2 MHz Fc

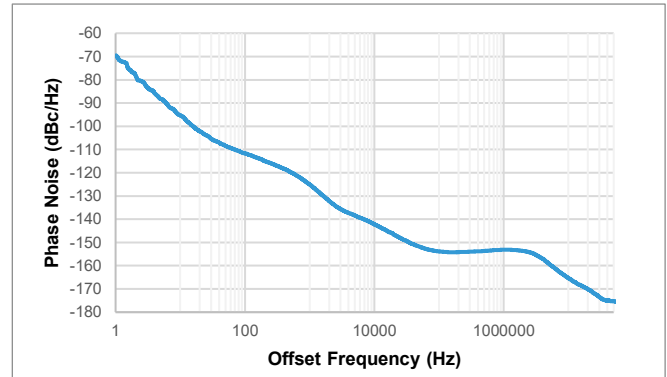


Figure 6. Phase Noise – 122.8 MHz Fc

Test Circuit Diagrams for LVCMOS and Clipped Sinewave Outputs

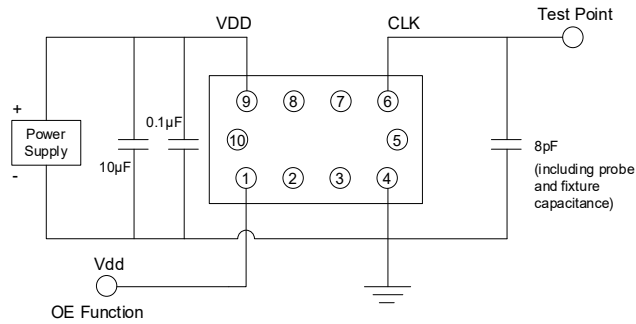


Figure 7. LVCMOS Test Circuit (OE Function)

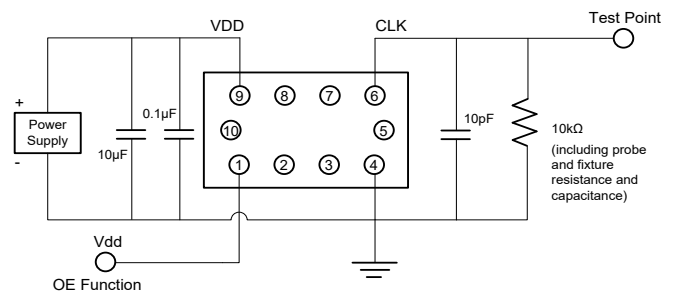


Figure 8. Clipped Sinewave Test Circuit (OE Function) for AC and DC Measurements

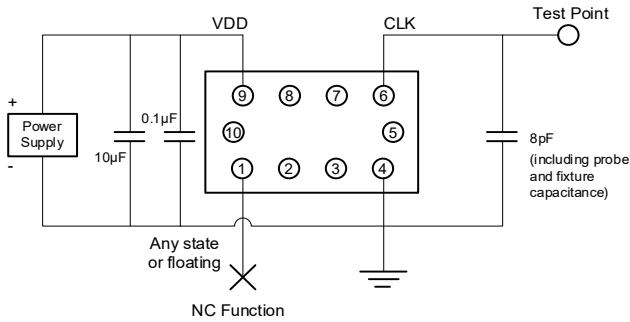


Figure 9. LVCMOS Test Circuit (NF Function)

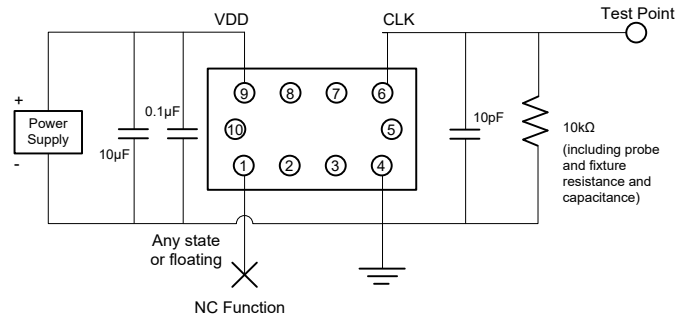


Figure 10. Clipped Sinewave Test Circuit (NF Function) for AC and DC Measurements

Test Circuit Diagrams for LVCMOS and Clipped Sinewave Outputs (continued)

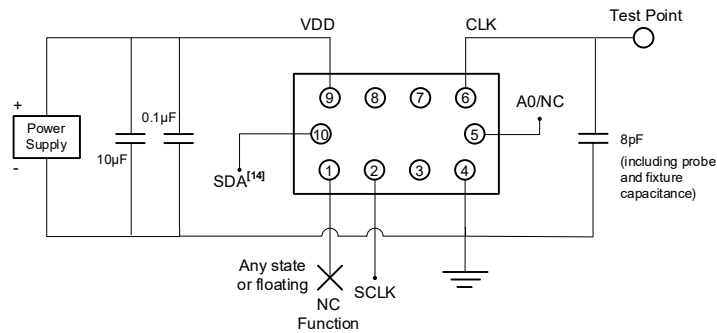


Figure 11. LVCMOS Test Circuit (I²C Control), DCTCXO mode for AC and DC Measurements

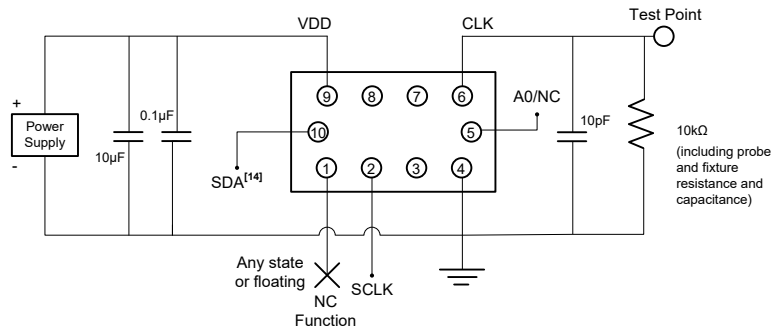


Figure 12. Clipped Sinewave Test Circuit (I²C Control), DCTCXO mode for AC and DC Measurements

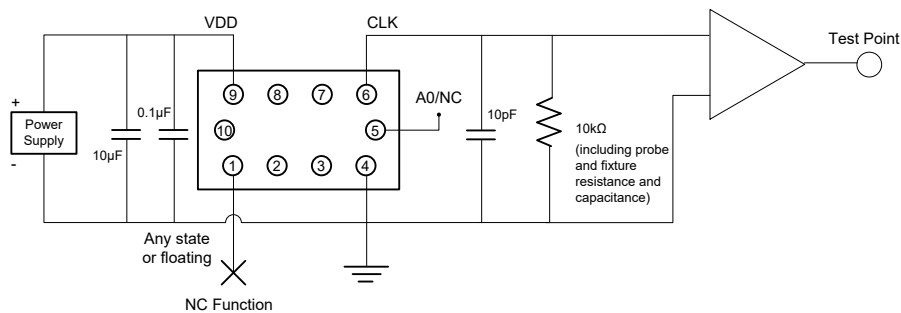


Figure 13. Clipped Sinewave Test Circuit for Phase Noise Measurements, Applies to All Configurations (NF Function shown for example only)

Note:

15. SDA is open-drain and may require pull-up resistor if not present in I²C test setup.

Waveforms

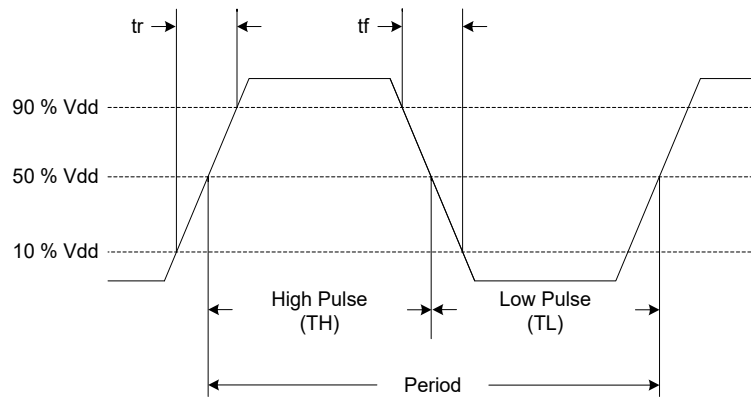


Figure 14. LVCMOS Waveform Diagram^[16]

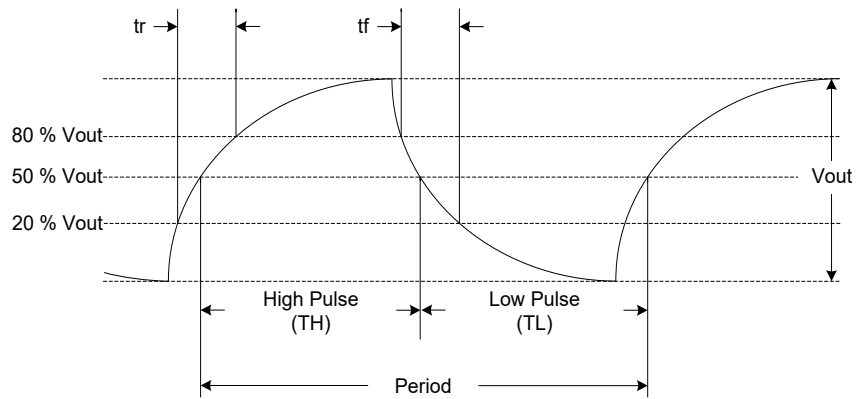
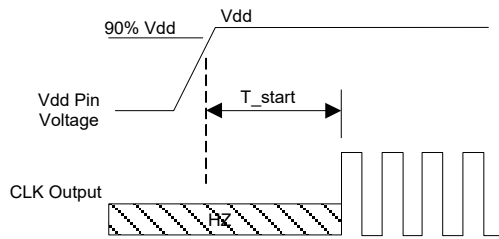


Figure 15. Clipped Sinewave Waveform Diagram^[16]

Note:

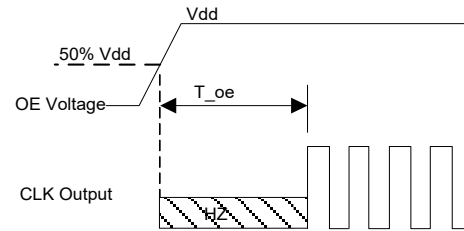
16. Duty Cycle is computed as $\text{Duty Cycle} = \text{TH}/\text{Period}$.

Timing Diagrams



T_{start} : Time to start from power-off

Figure 16. Startup Timing



T_{oe} : Time to re-enable the clock output

Figure 17. OE Enable Timing (OE Mode Only)

Stability Diagrams

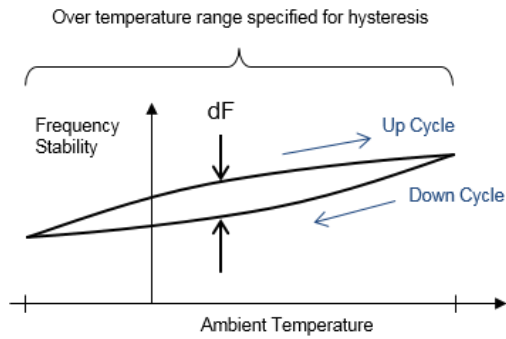


Figure 18. Illustration of hysteresis, where dF is max frequency difference between up and down cycles across temperature

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)

(TOP VIEW)

(SIDE VIEW)

(BOTTOM VIEW)

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.91	1.03	1.15
SUBSTRATE THICKNESS	A1	0.95 ref		
LID THICKNESS	A2	0.08 ref		
BODY SIZE	X	E		
	Y	D		
LEAD WIDTH	W	0.47	0.6	0.73
	W1	0.82	0.95	1.08
LEAD LENGTH	L	1.145	1.275	1.405
	L1	0.77	0.9	1.03
	L2	0.795	0.925	1.055
LEAD PITCH	e	1.2 BSC		
	e1	2.075 BSC		
EDGE LEAD CENTER TO CENTER	D1	3.9 BSC		
	E1	2.35 BSC		
BODY CENTER TO CONTACT LEAD	SD	0.6 BSC		
	SE	1.175 BSC		
PACKAGE EDGE TOLERANCE	aaa	0.13		

NOTE

- ALL DIMENSIONS IN MM
- BOTTOM PAD PLATING:
 ELECTROLYTIC Ni: 1.27~8.89 μm
 ELECTROLYTIC Au (≥99.9%): 0.30~0.80 μm

PKG INFO		DRAWING NO.	
10L CQFN 5.0X3.5X1.03 mm		POD-087-CQFN-010-X5035	
DATE	10/14/2025	REV	SHEET
		05	01

Recommended Land Pattern (Unit: mm)

+ POD Center-mark
 + SPL Center-mark

Note: All units in mm.

SiTime		PKG INFO		SPL DRAWING NO.	
DATE	2025/11/12	10L CQFN 5.000x3.500 mm		SPL-087-CQFN-010-C05035	
		REV	A07	SHEET	01

Additional Information

Table 12. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Elite RF Digital Control Guide

Introduction

This document details the SiT7201/2 Elite RF register map. The detailed description focuses on the sections of the register map that control DCXO mode operation and determine ambient temperature with the temperature to digital converter (TDC) function. DCXO mode is a mode of operation where the TCXO output can be precisely controlled via digital inputs applied through the serial (I2C or SPI) interface. It is used commonly to phase lock the TCXO output to another reference or to do aging compensation of the TCXO output frequency. [Using the DCXO Function](#) Section covers the details of DCXO mode operation. Finally, we describe how to determine ambient temperature from the TDC temperature in [Using the TDC Information](#) Section.

Register Map

[Table DG1](#) below shows the details of the Elite RF register map dealing with the DCXO mode. For parts preprogrammed with fixed addresses, Elite RF's I2C address is 0x5x where the last x can be any hex number from 0 to F. For parts that use the A1 A0 pins to set the address the address decode is shown in the last part of [Table DG1](#).

Table DG1. Elite RF Register Detail

Description of Registers					
Register	Name	Size (bits)	Format (16 bit registers)	Scaling	Read/Write
Address					
0x00	DCXO_Clip	13	DCXO_Clip[12:0] register bits[12:0]		R
0x0C	DCXO	16	DCXO[38:23]		R/W
0x0D	DCXO	16	DCXO[22:7]		R/W
0x0E	DCXO	7	DCXO[6:0] register bits[15:9]		R/W
0x13	Output disables	1	Output disables bit 12		R/W
0x20	TDC	16	TDC[45:30]		R
0x21	TDC	16	TDC[29:14]		R
0x22	TDC	14	TDC[13:0] register bits[15:2]		R
0x2A	Chip ID	16	Chip ID [15:0] (Expected readback D0xx)		R

Table DG2. Preprogrammed Address Decode (I2C)

Ordering Code	Address (in binary)
0	101 0000
1	101 0001
2	101 0010
3	101 0011
4	101 0100
5	101 0101
6	101 0110
7	101 0111
8	101 1000
9	101 1001
A	101 1010
B	101 1011
C	101 1100
D	101 1101
E	101 1110
F	101 1111

Table DG3. A1 A0 Pin Address Decode (I2C)

A1 A0 Pin Address Decode (I2C)		
A1	A0	Address (in binary)
0	0	101 0000
0	1	101 0010
1	0	101 1000
1	1	101 1010

SPI Usage Notes

The SPI bus for the Epoch family uses the below standard pin definitions.

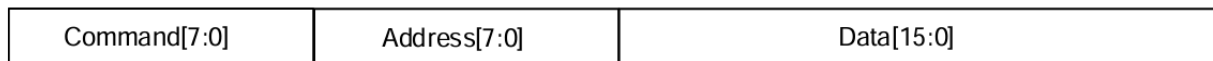
SCLK – Serial clock

MOSI – Master output slave input

MISO – Master input slave output

$\overline{\text{CS}}$ – Chip select, active low

The general format of communication to the chip via SPI is as shown below.



The write and read commands are as shown below:

Write: 57h

Read: A5h

Address and data are as shown in [Table DG1](#).

Using the DCXO Function

The DCXO function is controlled by 39 bits contained in registers 0x0C, 0x0D and 0x0E. The bits are arranged as shown in [Table DG1](#). The maximum pull range is controlled by the 13 bits contained in register 0x00 and called DCXO_Clip.

The DCXO binary control number represents the fractional portion of the total possible pull of the output frequency. The total pull available is ± 800 ppm. The next sections describe how to determine the DCXO control words based upon a desired frequency.

Pull Range, Absolute Pull Range

Pull range (PR) is the amount of frequency deviation that will result from changing the control word over its maximum range under nominal conditions.

Absolute pull range (APR) is the guaranteed controllable frequency range over all environmental and aging conditions. Effectively, it is the amount of pull range remaining after taking into account frequency stability,

tolerances over variables such as temperature, power supply voltage, and aging, i.e.:

$$APR = PR - F_{\text{stability}} - F_{\text{aging}}$$

where $F_{\text{stability}}$ is the device frequency stability due to initial tolerance and variations on temperature, power supply, and load. For the case of the Elite RF $F_{\text{stability}}$ and F_{aging} are so small compared to PR APR is essentially equal to PR.

[Figure DG1](#) shows a typical SiTime DCXO Freq vs Frequency Control Word (FCW) characteristic. The Frequency vs FCW characteristic varies with conditions, so that the frequency output at a given FCW can vary by as much as the specified frequency stability of the DCXO. For such DCXOs, the frequency stability and APR are independent of each other. This allows very wide range of pull options without compromising frequency stability.

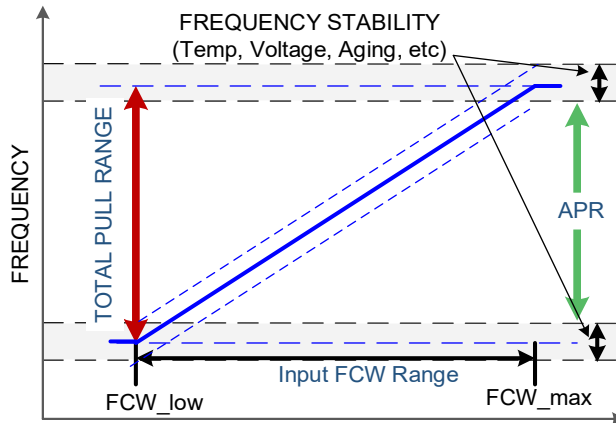


Figure DG1. Typical SiTime Frequency vs FCW graph for DCTCXO

The FCW_low and FCW_max are the specified limits of the FCW range as shown in [Figure DG1](#) above. Applying FCW values beyond the upper and lower limits does not result in noticeable changes of output frequency. In other words, the Frequency vs FCW characteristic of the DCXO saturates beyond FCW_low or FCW_max.

DCTCXO-Specific Design Considerations

Pull Range and Absolute Pull Range

Pull range and absolute pull range are described in the previous section. [Table DG4](#) below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

Table DG4. APR Options

Pull Range Ordering Code	Pull Range ppm	APR ppm ±3 ppb option ±80ppb 20-year aging	APR ppm ±5 ppb option ±80ppb 20-year aging
V	±3.125	±3.039	±3.035
T	±6.25	±6.164	±6.160
R	±10	±9.914	±9.910
Q	±12.5	±12.414	±12.410
M	±25	±24.914	±24.910
B	±50	±49.914	±49.910
E	±100	±99.914	±99.910
H	±200	±199.914	±199.910
X	±400	±399.914	±399.910

Output Frequency

The device powers up at the nominal operating frequency and pull range specified by the ordering code. After power-up output frequency can be controlled via I2C writes to the respective control registers. The maximum output frequency change is constrained by the pull range limits.

The frequency output is specified by the value loaded in the DCXO register. The output frequency is determined by the following equation: $F_{out} = (1 + DCXO \cdot 800e-6) F_o$. DCXO is a signed 39 bit fraction, S.38f, with range ±1. F_o is the nominal output frequency.

[Table DG5](#) below shows the frequency resolution versus pull range programmed.

Table DG5. Frequency Resolution versus Pull Range

Programmed Pull Range	Frequency Resolution
±3.125 ppm	5.0×10^{-14}
±6.25 ppm	5.0×10^{-14}
±10 ppm	5.0×10^{-14}
±12.5 ppm	5.0×10^{-14}
±25 ppm	5.0×10^{-14}
±50 ppm	5.0×10^{-14}
±100 ppm	5.0×10^{-14}
±200 ppm	5.0×10^{-14}
±400 ppm	5.0×10^{-14}

The ppm frequency offset is specified by the 39 bit DCXO frequency control word in two's complement format as described in the I2C Register Descriptions. The power up default value is 000000000000000000000000b which sets the output frequency at its nominal value (0 ppm). To change the output frequency, a frequency control word is written to 0x0C[38:23] (Most Significant Word), 0x0D[22:7] (Next Significant Word) and 0x0E[6:0] register bits[15:9] (Least Significant Word). The MSW value should be written first followed by NSW and finally the LSW value; the

frequency change is initiated after the LSW value is written.

Figure DG2 shows how the two's complement signed value of the frequency control word sets the output frequency within the ±800 ppm full pull range. To set the desired output frequency, one just needs to calculate the fraction of full scale value ppm, convert to two's complement binary, and then write these values to the frequency control registers.

Bits	38:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Hex	011	1111	1111	1111	1111	1111	1111	1111	1111	1111
Decimal	(2 ³⁸)-1 = 274,877,906,943									
ppm	+800ppm									

Bits	38:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Hex	000	0000	0000	0000	0000	0000	0000	0000	0000	0000
Decimal	0									
ppm	0ppm									

Bits	38:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Hex	100	0000	0000	0000	0000	0000	0000	0000	0000	0000
Decimal	(2 ³⁸) = -274,877,906,944									
ppm	-800ppm									

Figure DG2. Frequency Control Word

The following formula generates the control word value:

Control word value = RND((238-1) × ppm shift from nominal/800ppm), where RND is the rounding function which rounds the number to the nearest whole number.

3 examples follow. Examples 1 and 2 cover the case where DCXO_Clip=0. In this case the full pull range is ±800 ppm. Example 3 shows how the DCXO_Clip factory setting is used to reduce the max pull range.

Example 1:

- Default Output Frequency = 19.2 MHz
- Desired Output Frequency = 19.201728 MHz (+90 ppm)

2³⁸-1 corresponds to +800 ppm, and the fractional value required for +90 ppm can be calculated as follows.

- 90 ppm / 800 ppm × (2³⁸-1) = 30,923,764,531.0875.

Rounding to the nearest whole number yields 30,923,764,531 and converting to two's complement gives a binary value of, 0111 0011 0011 0011 0011 0011 0011 0011 0011 0011 or 733333333 in hex.

In general, the max pull range is calculated using the below relation.

Equation 1
 MaxDCXOpull = +/-((800ppm*(DCXO_Clip/(2¹³))).

The only exception is when DCXO_Clip=0. In this case, the DCXO pull range is ±800ppm.

Example 2:

- Default Output Frequency = 10 MHz
- Desired Output Frequency = 9.9995 MHz (-50 ppm)

Following the formula shown above,

- (-50 ppm / 800 ppm) × (2³⁸) = -17,179,869,184.

Converting this to two's complement binary results in -1*(000 0100 0000 0000 0000 0000 0000 0000 0000 0000) = 111 1100 0000 0000 0000 0000 0000 0000 0000 0000, or 3C00000000 in hex. The negative number is represented as a 2's complement.

Since the DCXO_Clip value is 0 the DCXO pull range is ±800 ppm.

Example 3:

In this final example let's look at the case when the max pull range is factory set to 200 ppm. Now the DCXO_Clip value will be set at shown below. Solving Equation 1 from Example 1 and rounding gives:

Equation 2

$$DCXO_Clip := RND\left(\left(2^{13}\right) \cdot \left(\frac{MaxDCXOPull}{800\text{ ppm}}\right)\right) = 2.048 \cdot 10^3$$

Converting 2048 into binary gives, 010000000000. This is the value that will be read from register 0x00. The formula to calculate the FCW for a given desired ppm offset remains the same. So the FCW for 90 ppm is still calculated as in Example 1 and is the two's complement value 0111 0011 0011 0011 0011 0011 0011 0011 or 733333333 in hex. Negative values are still calculated as in Example 2. This means the DCXO_Clip value does not change the DCXO slope. It only changes the DCXO saturation point. This is illustrated in Figure A3 below.

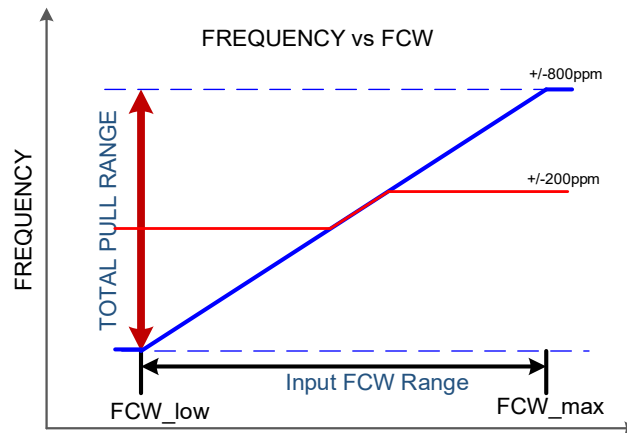


Figure DG3. DCXO_Clip Illustration

It is important to note that the maximum DCXO update rate is 50 kHz for an SPI bus speed of 5 MHz and 10 kHz for an I2C bus rate of 1 MHz. For faster update rates [contact SiTime](#). The minimum read cycle time, or the minimum time between successive reads of a register, is 50 ms.

Using the TDC Information

The Elite RF platform has an on-board dual resonator temperature to digital converter (TDC) with 46 bit resolution. This TDC can be used to measure the on-chip MEMS temperature with very high resolution. It can also, with some simple calibration, be correlated to ambient temperature.

The relationship between the TDC bits TDC [45:0] and ambient temperature will be linear. The linear equation that relates ambient temperature to the TDC output can be found by reading the TDC bits at 2 separate ambient temperatures, plotting the ambient temperature vs TDC value and then deriving the linear equation that relates TDC value to ambient temperature. It is recommended to choose 2 temperatures at least 10°C apart.

Revision History

Table 13. Revision History

Version	Release Date	Change Summary
1.0	22-Dec-2025	Initial Release

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | Phone: +1-408-328-4400 | Fax: +1-408-328-4439

© SiTime Corporation 2025. The information contained herein is subject to change at any time without notice. SiTime assumes no responsibility or liability for any loss, damage or defect of a Product which is caused in whole or in part by (i) use of any circuitry other than circuitry embodied in a SiTime product, (ii) misuse or abuse including static discharge, neglect or accident, (iii) unauthorized modification or repairs which have been soldered or altered during assembly and are not capable of being tested by SiTime under its normal test conditions, or (iv) improper installation, storage, handling, warehousing or transportation, or (v) being subjected to unusual physical, thermal, or electrical stress.

Disclaimer: SiTime makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any SiTime product and any product documentation. This product is not suitable or intended to operate in nuclear facilities. All sales are made conditioned upon compliance with the critical uses policy set forth below.

SiTime owns all rights, title and interest to the intellectual property related to SiTime's products, including any software, firmware, copyright, patent, or trademark. The sale of SiTime products does not convey or imply any license under patent or other rights. SiTime retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by SiTime. Unless otherwise agreed to in writing by SiTime, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.