SiT5541

1 MHz – 60 MHz, Endura™ Ruggedized Super-TCXO Oscillator

Description

The SiT5541 is a ruggedized precision oscillator optimized for ±10 ppb stability from -40°C to 105°C. Engineered for exceptional dynamic performance, it is ideal for replacing larger and less robust quartz OCXOs. SiT5541 is uniquely designed for highly accurate aerospace and defense applications, military radios, IEEE 1588 PTP and optical transport applications.

Leveraging SiTime's unique DualMEMS® temperature sensing and TurboCompensation® technologies, the SiT5541 delivers the best dynamic performance for timing stability in the presence of environmental stressors such as air flow, temperature perturbation, vibration, shock, and electromagnetic interference. This device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for a dedicated external LDO.

The SiT5541 can be factory programmed for any combination of frequency, voltage, and pull range. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each frequency is custom built.

Refer to Manufacturing Guideline for proper reflow profile and PCB cleaning recommendations to ensure best performance.

Features

- Any frequency from 1 MHz to 60 MHz in 1 Hz steps
- Factory programmable options for low lead time
- Best dynamic stability under airflow, thermal shock
  - ±10 ppb frequency stability over temperature
  - -40°C to 105°C operating temperature range
  - ±0.3 ppb/°C typical frequency slope (dF/dT)
  - 1.5e-11 ADEV at 10 second averaging time
- 0.01 or 0.1 ppb/g acceleration sensitivity.
- Digital frequency control up to ±3200 ppm
- No activity dips or micro jumps
- Resistant to shock, vibration and board bending
- On-chip regulators eliminate external LDOs
- 2.5 V, 2.8 V, 3.0 V and 3.3 V supply voltage
- LVCMOS or clipped sinewave output
- 7.0 mm x 5.0 mm ceramic package
- Contact SiTime for tighter stability, wider temperature, and alternate package options

Applications

- Ruggedized communication networks
- Military radios
- SATCOM
- Precision GPS/GNSS systems
- Military, defense, space, avionics systems

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Block Diagram

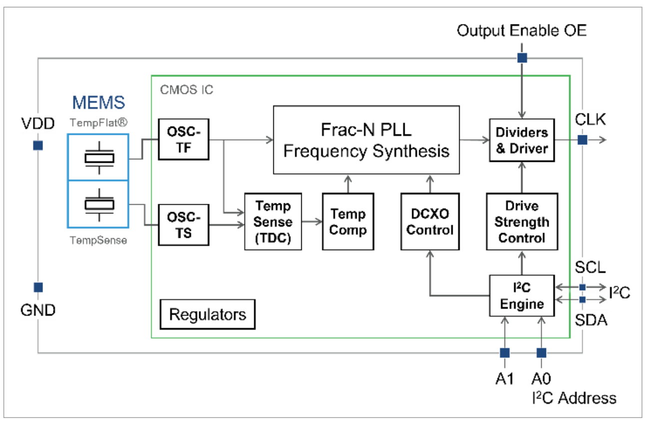


Figure 1. SiT5541 Block Diagram

7.0 mm x 5.0 mm Package Pinout

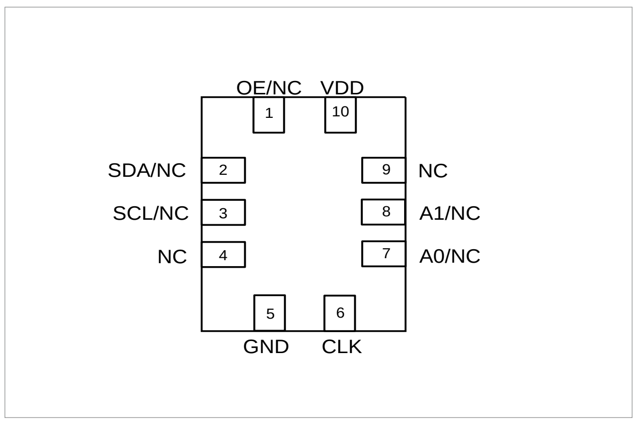
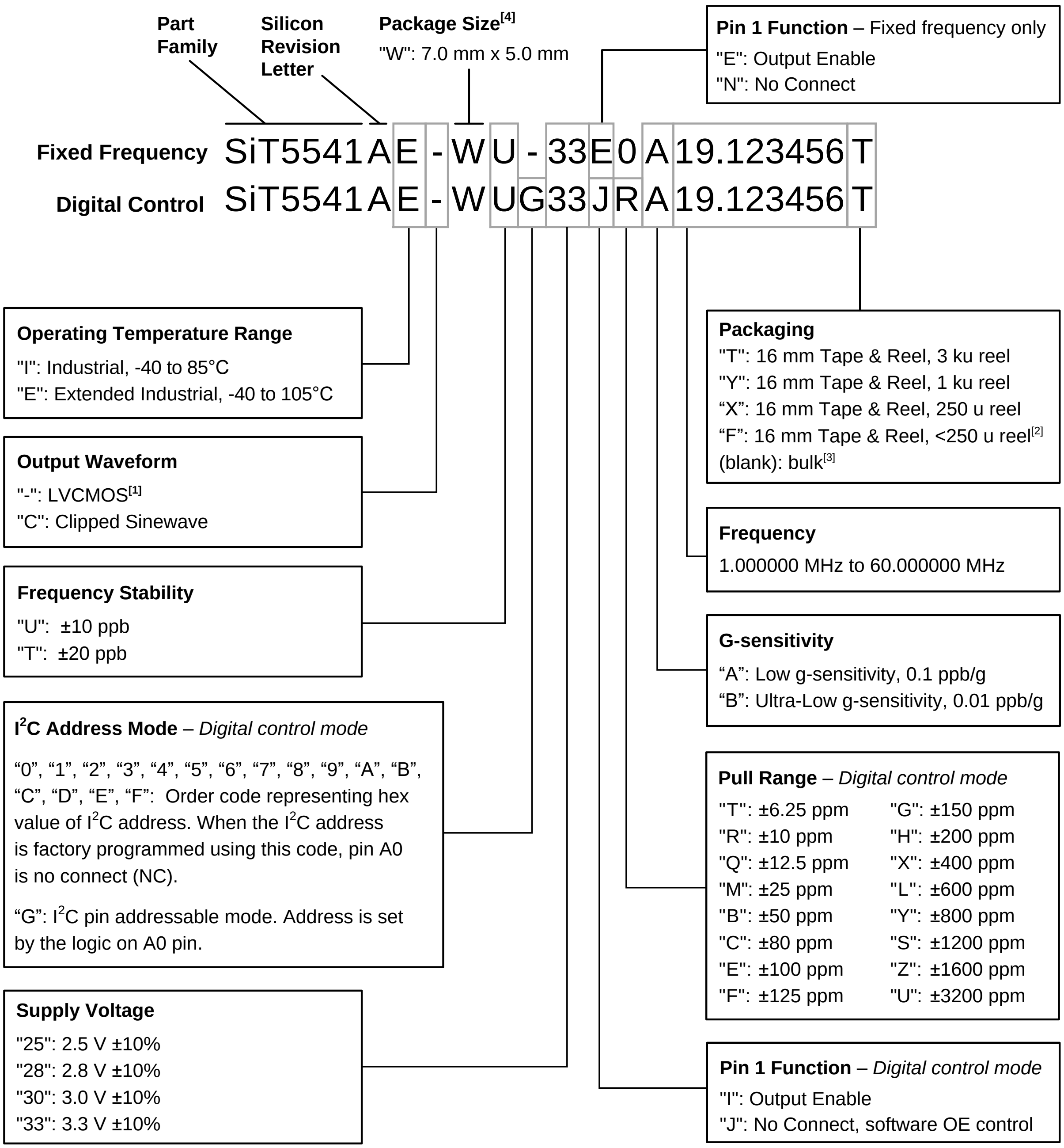


Figure 2. Pin Assignments (Top view)

Ordering Information

The part number guide illustrated below is for reference only, in which boxes identify order codes having more than one option. To customize and build an exact part number, use the SiTime Part Number Generator. To validate the part number, use the SiTime Part Number Decoder.



Notes:

1. "-" corresponds to the default rise/fall time for LVCMOS output as specified in Table 1 (Electrical Characteristics). Contact SiTime for other rise/fall time options for best EMI or driving multiple loads. For differential outputs, contact SiTime.
2. "F" cut-tape packaging option has a minimum limit of 10 units.
3. Bulk is available for sampling only.
4. Contact SiTime for alternate package options.

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Appendix

Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and 3.3 V Vdd.

Table 1. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Nominal Output Frequency Range	F_nom	1	–	60	MHz	Contact SiTime for higher frequency options
Temperature Range						
Operating Temperature Range	T_oper	-40	–	+85	°C	Industrial, ambient temperature "I"
		-40	–	+105	°C	Extended industrial, ambient temperature, "E"
Rugged Characteristics						
Acceleration (*g*) Sensitivity, Gamma Vector	F_g	–	–	±0.01	ppb/*g*	Low sensitivity grade; total gamma over 3 axes; 15 Hz to 2 kHz; MIL-PRF-55310, computed per section 4.8.18.3.1 Ordering option "B"
		–	–	±0.1	ppb/*g*	Ordering option "A"
Frequency Stability – Stratum 3E Grade						
Frequency Stability over Temperature	F_stab	–	–	±10	ppb	Over operating temperature range (T_oper); referenced to (max frequency + min frequency)/2 over the temperature range. Frequency stability option "U".
Initial Tolerance	F_init	–	–	±0.1	ppm	Initial frequency at 25°C at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_Vdd	–	±0.5	±0.7	ppb	Over operating temperature range (T_oper); Vdd ±5%
Output Load Sensitivity	F_load	–	±0.1	±0.2	ppb	Over operating temperature (T_oper); LVCMOS output, 15 pF ±10%. Clipped sinewave, 10 kΩ || 10 pF ±10%
Frequency vs. Temperature Slope	dF/dT	–	±0.3	±0.5	ppb/°C	0.5°C/min temperature ramp rate, over operating temperature (T_oper)
Dynamic Frequency Change during Temperature Ramp	F_dynamic	–	±0.003	±0.004	ppb/s	0.5°C/min temperature ramp rate, over operating temperature (T_oper)
Hysteresis Over Temperature Contact SiTime for lower hysteresis	F_hys	–	±0.8	±2	ppb	0.5°C/min ramp rate, defined as ±ΔF/2, over operating temperature (T_oper)
One-Day Aging	F_1d	–	±0.2	±0.5	ppb	At 85°C, after 30-days of continued operation. Aging is measured with respect to day 31
One-Year Aging	F_1y	–	–	±80	ppb	At 85°C, after 2-days of continued operation. Aging is measured with respect to day 3
20-Year Aging	F_20y	–	–	±150	ppb	
20-Year Total Stability	F_tot_20y	-270		+270	ppb	Includes aging, temperature stability, ±10% load and ±5% supply sensitivity. Exceeds GR-1244-CORE Stratum 3E spec of 4.6 ppm.
Allan deviation	ADEV	–	1.5e-11	–	–	10 second averaging time, measured 2 hours after startup in a temperature chamber with a constant temperature in still air.
Frequency Stability – Synchronization Grade						
Frequency Stability over Temperature	F_stab	–	–	±20	ppb	Over operating temperature range (T_oper); referenced to (max frequency + min frequency)/2 over the temperature range. Frequency stability option "U".
Initial Tolerance	F_init	–	–	±0.2	ppm	Initial frequency at 25°C at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_Vdd	–	±1	±2	ppb	Over operating temperature range (T_oper); Vdd ±5%
Output Load Sensitivity	F_load	–	±0.5	±1	ppb	Over operating temperature (T_oper); LVCMOS output, 15 pF ±10%. Clipped sinewave, 10 kΩ || 10 pF ±10%
Frequency vs. Temperature Slope	dF/dT	–	±0.6	±1	ppb/°C	0.5°C/min temperature ramp rate, over operating temperature (T_oper)
Dynamic Frequency Change during Temperature Ramp	F_dynamic	–	±0.006	±0.008	ppb/s	0.5°C/min temperature ramp rate, over operating temperature (T_oper)
Hysteresis Over Temperature Contact SiTime for lower hysteresis	F_hys	–	±2	±5	ppb	0.5°C/min ramp rate, defined as ±ΔF/2, over operating temperature (T_oper)
One-Day Aging	F_1d	–	±0.6	±1	ppb	At 85°C, after 30-days of continued operation. Aging is measured with respect to day 31
One-Year Aging	F_1y	–	–	±120	ppb	At 85°C, after 2-days of continued operation. Aging is measured with respect to day 3
20-Year Aging	F_20y	–	–	±200	ppb	
20-Year Total Stability	F_tot_20y	-300		300	ppm	Includes aging, temperature stability, ±10% load and ±5% supply sensitivity. Exceeds GR-1244-CORE Stratum 3E spec of 4.6 ppm.
Allan deviation	ADEV	–	1.5e-11	–	–	10 second averaging time, measured 2 hours after startup in a temperature chamber with a constant temperature in still air.

Table 1. Output Characteristics (continued)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	0.8	1.2	1.9	ns	10% - 90% Vdd
Output Voltage High	VOH	90%	–	–	Vdd	IOH = +3 mA
Output Voltage Low	VOL	–	–	10%	Vdd	IOL = -3 mA
Output Impedance	Z_out_c	13	19	31	Ohms	Impedance looking into output buffer
Clipped Sinewave Output Characteristics (by special request)						
Output Voltage Swing	V_out	0.8	–	1.2	V	Clipped sinewave output, 10 kΩ || 10 pF ±10%
Rise/Fall Time	Tr, Tf	–	3.5	4.6	ns	20% - 80% Vdd, F_nom = 19.2 MHz
Start-up Characteristics						
Start-up Time	T_start	–	2.5	3.5	ms	Time to first pulse, measured from the time Vdd reaches 90% of its final value. Vdd ramp time is 150 µs, 0 V to Vdd
Output Enable Time	T_oe	–	–	680	ns	F_nom = 10 MHz. See Timing Diagrams section below
Time to Rated Frequency Stability	T_stability	–	0.2	1.6	s	Time to first accurate pulse within rated stability, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 500 µs

Table 2. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	Vdd	2.25	2.5	2.75	V	Contact SiTime for 2.25 V to 3.63 V continuous supply voltage support
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
Supply Voltage Ramp Time [5]	Vdd_rt	500	–	–	µs	Measured from power up to 100% of Vdd
Current Consumption						
Current Consumption	Idd	–	44	53	mA	F_nom = 19.2 MHz, No Load
OE Disable Current	I_od	–	43	51	mA	OE = GND, output weakly pulled down

Note:

5. SiT5541 requires a minimum supply voltage ramp time of 500 µs.

Table 3. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics – OE Pin						
Input Impedance	Z_in	75	–	–	kΩ	Internal pull up to Vdd
Input High Voltage	VIH	70%	–	–	Vdd	
Input Low Voltage	VIL	–	–	30%	Vdd	
Frequency Tuning Range – I²C mode						
Pull Range	PR	±6.25 ±10 ±12.5 ±25 ±50 ±80 ±100 ±125 ±150 ±200 ±400 ±600 ±800 ±1200 ±1600 ±3200	–	–	ppm	Digitally controlled mode
Absolute Pull Range[6]	APR	±5.68	–	–	ppm	Over operating temperature range (T_rated); Digitally controlled mode for PR = ±6.25 ppm
I²C Interface Characteristics, 200 Ohm, 550 pF (Max I²C Bus Load)						
Bus Speed	F_I2C	≤ 400			kHz	-40 to 105°C
		≤ 1000			kHz	-40 to 85°C
Input Voltage Low	VIL_I2C	–	–	30%	Vdd	Digitally controlled mode
Input Voltage High	VIH_I2C	70%	–	–	Vdd	Digitally controlled mode
Output Voltage Low	VOL_I2C	–	–	0.4	V	Digitally controlled mode
Input Leakage current	I_L	0.5	–	24	µA	0.1 V_{DD}< VOUT < 0.9 V_{DD}. Includes typical leakage current from 200 kΩ pull resister to VDD. Digitally controlled mode
Input Capacitance	C_{IN}	–	–	5	pF	Digitally controlled mode

Note:

6. APR = PR – initial tolerance – 20-year aging – frequency stability over temperature.

Table 4. Phase Noise

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Phase Noise						
1 Hz offset		–	-80	-77	dBc/Hz	F_nom = 10 MHz Fixed frequency and digitally controlled mode with ±6.25 ppm pull range
10 Hz offset		–	-109	-106	dBc/Hz	
100 Hz offset		–	-130	-124	dBc/Hz	
1 kHz offset		–	-145	-140	dBc/Hz	
10 kHz offset		–	-148	-146	dBc/Hz	
100 kHz offset		–	-148	-146	dBc/Hz	
1 MHz offset		–	-163	-160	dBc/Hz	
5 MHz offset		–	-165	-160	dBc/Hz	
Spurious		–	–	-95	dBc	

Table 5. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Value	Unit
Storage Temperature		-65 to 125	°C
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 4	V
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Charge Device Model (CDM) ESD Protection	JS-002-2018	750	V
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C
Junction Temperature[8]		130	°C
Input Voltage, Maximum	Any input pin	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	V

Table 6. Thermal Considerations[7]

Package	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	θ_{JB} (°C/W)	θ_{JC}, Top (°C/W)
Ceramic 7.0 mm x 5.0 mm	60.2	16.6	15.4	24.8

Note:

7. θ_{JA}, Ψ_{JT}, θ_{JB} and θ_{JC} are provided according to JEDEC 51-2 and 51-3 with a 25C ambient and 150 mW power consumption. θ_{JB} and θ_{JC} values apply for a two resistor model of the part in which heat flows from the junction to a heat sink through either the top of the case (θ_{JC}, Top) or the PCB (θ_{JB}). For a one resistor model θ_{JB} is representative. θ_{JA} is the thermal resistance to ambient on a JEDEC PCB - it is a highly conservative estimate of the thermal resistance to ambient for these parts, since the JEDEC board does not have vias to PCB planes in the vicinity of the part. Ψ_{JT} can be used to estimate the junction temperature from measurements of the temperature at the top of the part, as described in JEDEC 51-2.

Table 7. Maximum Operating Junction Temperature[8]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	**79°C**
85°C	**94°C**
105°C	**113°C**

Note:

8. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 8. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	**MIL-STD-883F, Method 2002**	**20,000**	*g*
Mechanical Vibration Resistance	**MIL-STD-883F, Method 2007**	**70**	*g*
Temperature Cycle	**JESD22, Method A104**	–	–
Solderability	**MIL-STD-883F, Method 2003**	–	–
Moisture Sensitivity Level	**MSL1 @260°C**	–	–

Device Configurations and Pin-outs

Table 9. Device Configurations

Configuration	I^2C Programmable Parameters
Fixed Frequency	–
Digitally Controlled	Frequency Pull Range, Frequency Pull Value, Output Enable control

Pin-out Top Views

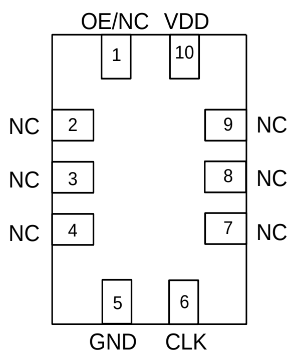


Figure 3. Fixed Frequency Device

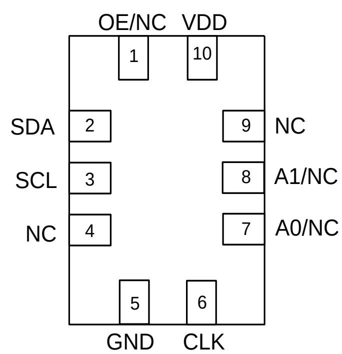


Figure 4. Digitally Controlled Device

Table 10. Pin Description

Pin	Symbol	I/O	Internal Pull-up/Pull Down Resistor	Function
1	OE / NC[11]	OE – Input	100 kΩ Pull-Up	H[9]: specified frequency output L: output is high impedance. Only output driver is disabled
		NC[9] – No Connect	–	H or L or Open: No effect on output frequency or other device functions
2	SDA / NC[11]	SDA – Input/Output	200 kΩ Pull Up	I^2C Serial Data
		NC – No Connect	–	H or L or Open: No effect on output frequency or other device functions
3	SCL / NC[10]	SCL – Input	200 kΩ Pull-Up	I^2C serial clock input
		No Connect		H or L or Open: No effect on output frequency or other device functions
4	NC[11]	No Connect	–	H or L or Open: No effect on output frequency or other device functions
5	GND	Power	–	Connect to ground
6	CLK	Output	–	LVCMOS, or clipped sinewave oscillator output
7	A0/NC[11]	A0 – Input	100 kΩ Pull-Up	For DCTCXO ordering code “G” only: I^2C Address Select, Least Significant Bit (LSB) A1 A0 I^2C Address 0 0 1100000 0 1 1100010 1 0 1101000 1 1 1101010 (Default)
8	A1/NC[11]	A1 – Input	100 kΩ Pull-Up	
9	NC[11]	No Connect	–	H or L or Open: No effect on output frequency or other device functions
10	VDD	Power	–	Connect to power supply[10]

Notes:

9. In OE mode for noisy environments, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
10. A 0.1 µF capacitor in parallel with a 10 µF capacitor are required between VDD and GND. The 0.1 µF capacitor is recommended to place close to the device, and place the 10 µF capacitor less than 2 inches away.
11. All NC pins can be left floating and do not need to be soldered down.

Waveforms

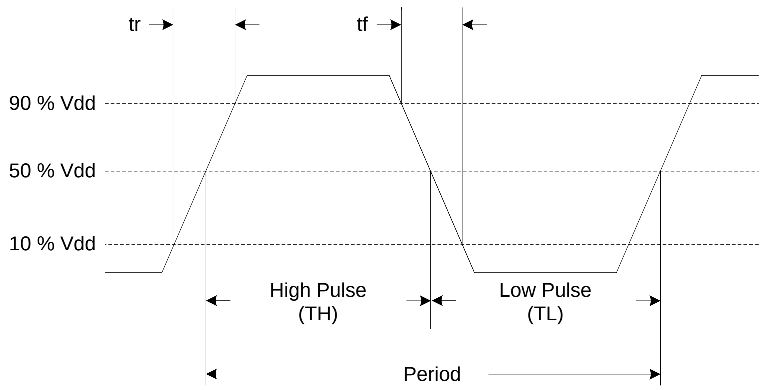


Figure 5. LVCMOS Waveform Diagram[12]

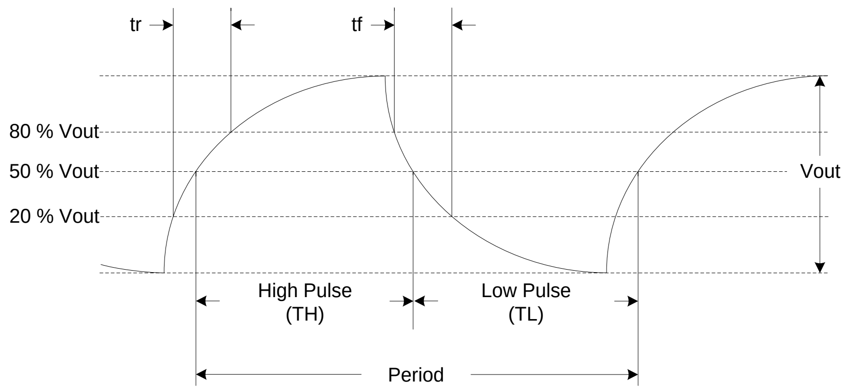
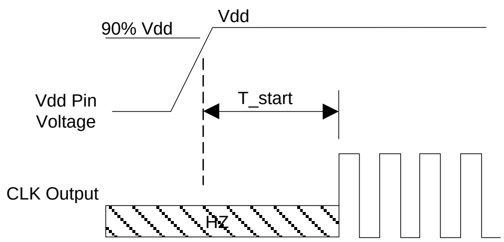


Figure 6. Clipped Sinewave Waveform Diagram[12]

Note:

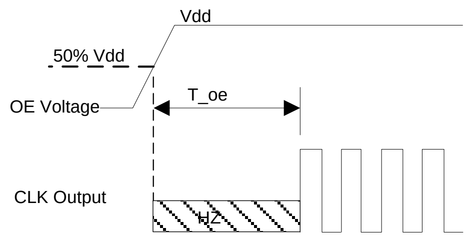
12. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagrams



T_start: Time to start from power-off

Figure 7. Startup Timing



T_oe: Time to re-enable the clock output

Figure 8. OE Enable Timing (OE Mode Only)

Stability Diagrams

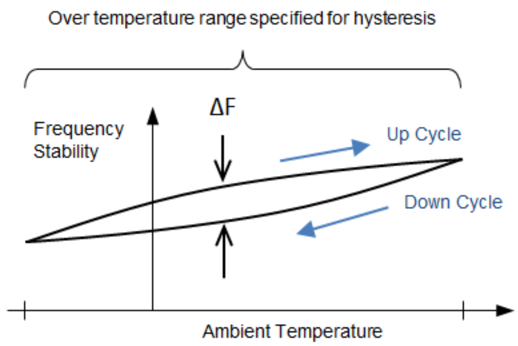


Figure 9. Illustration of hysteresis, where ΔF is max frequency difference between up and down cycles across temperature

Typical Performance Plots

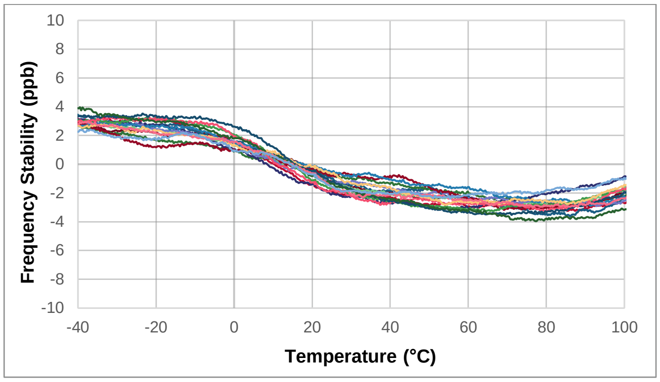


Figure 10. Frequency Stability

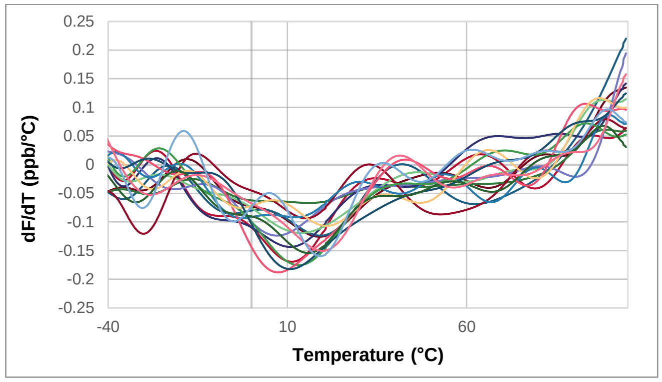


Figure 11. dF/dT

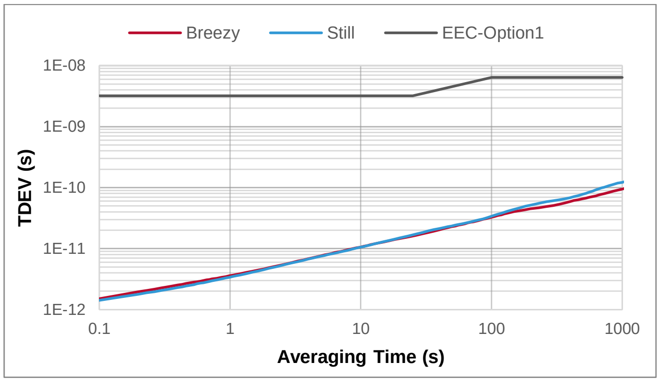


Figure 12. TDEV – Loop Bandwidth 3 Hz

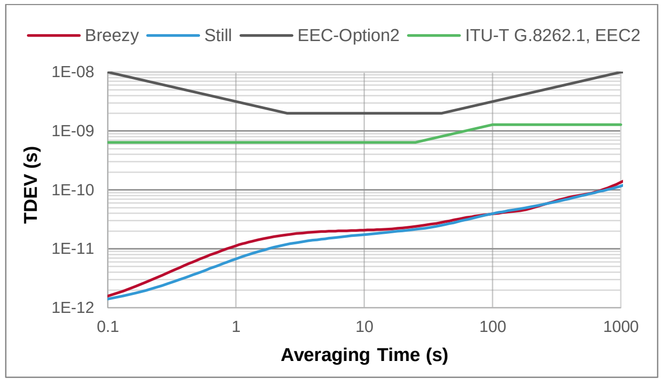


Figure 13. TDEV – Loop Bandwidth 0.1 Hz

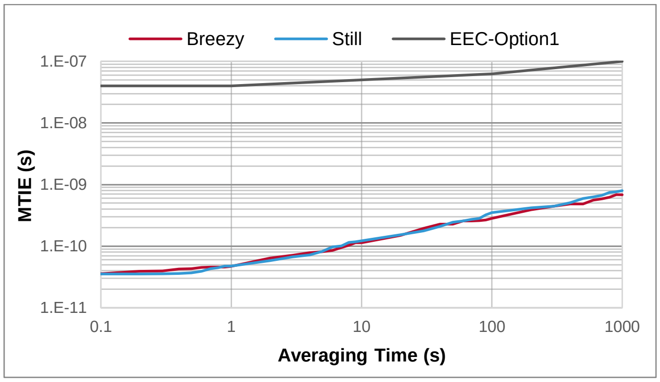


Figure 14. MTIE – Loop Bandwidth 3 Hz

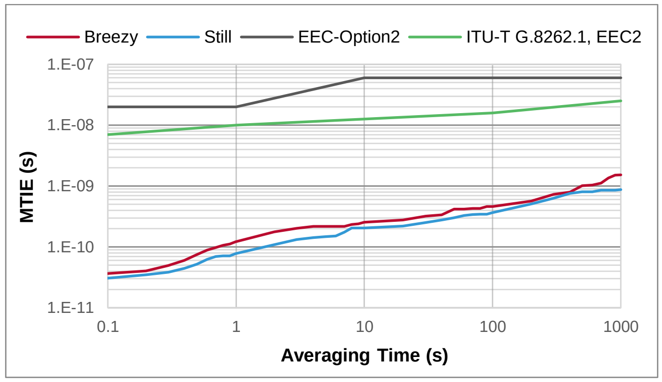


Figure 15. MTIE – Loop Bandwidth 0.1 Hz

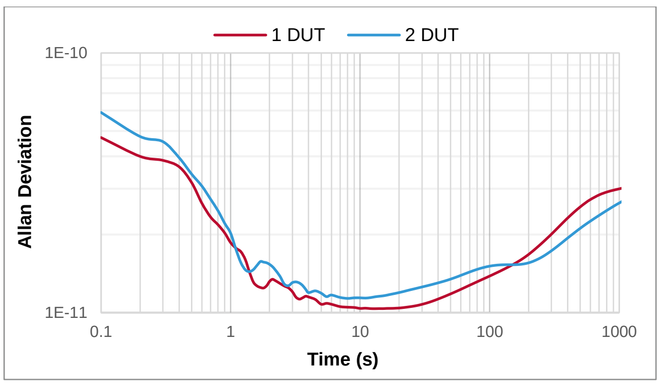


Figure 16. ADEV – Still Air

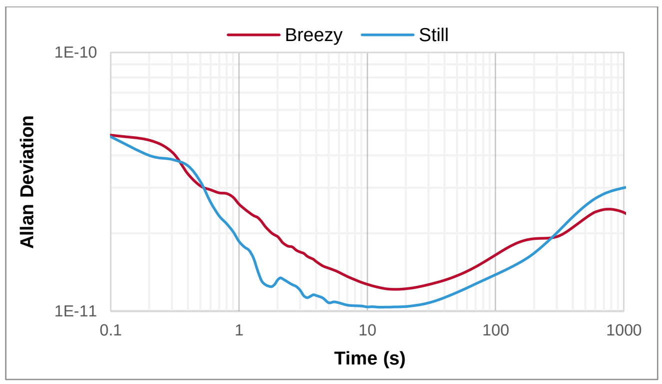


Figure 17. ADEV – Breezy Air

Typical Performance Plots (continued)

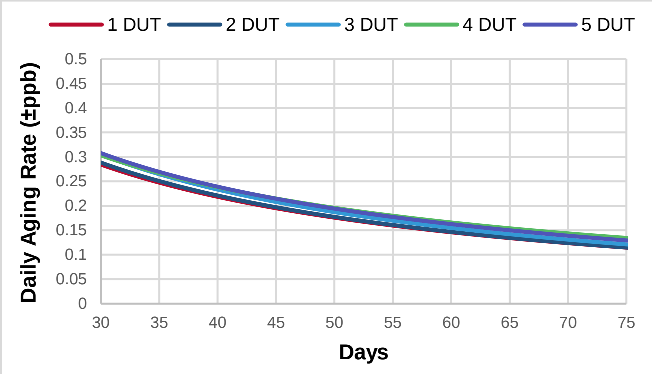


Figure 18. Daily Aging Rate After 30 Days

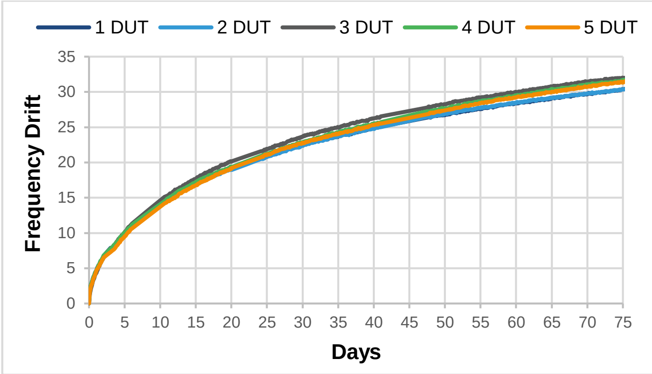


Figure 19. Frequency Drift

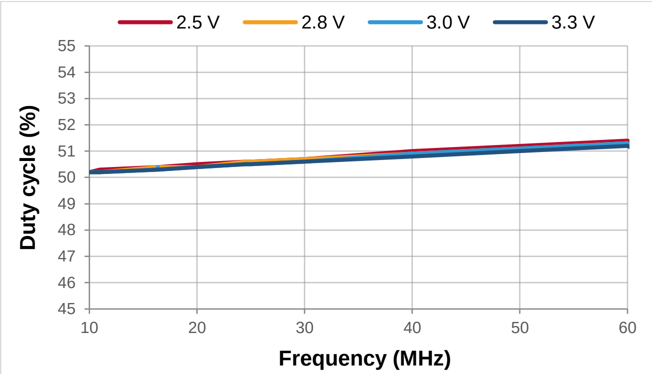


Figure 20. Duty Cycle (LVCMOS)

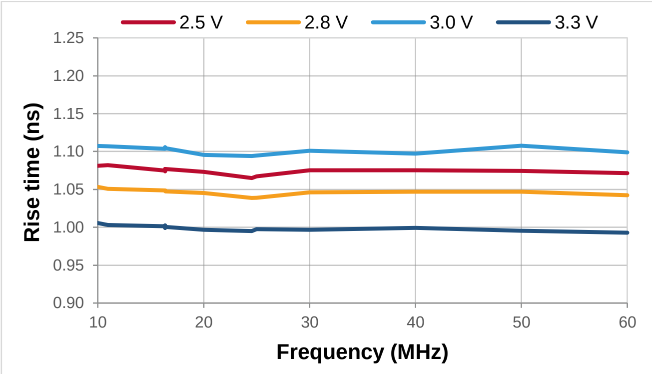


Figure 21. Rise Time (LVCMOS)

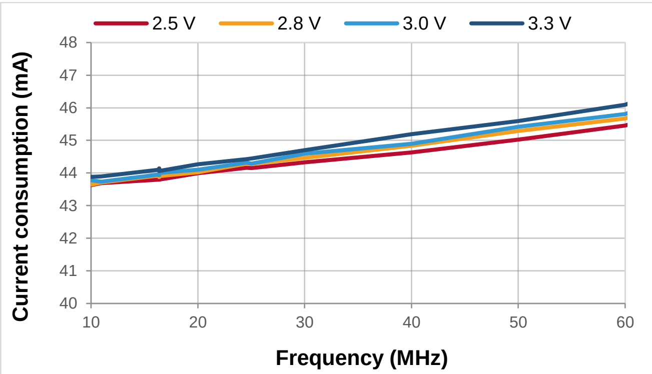


Figure 22. IDD TCXO (LVCMOS)

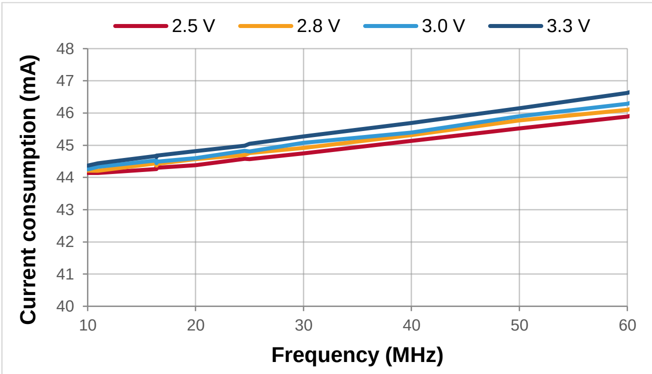


Figure 23. IDD DCTCXO (LVCMOS)

Typical Performance Plots (continued)

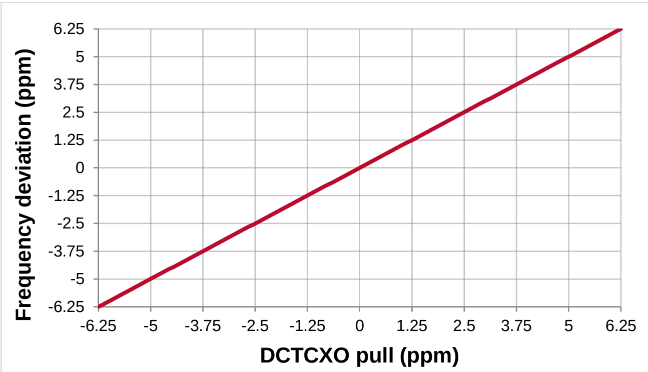


Figure 24. DCTCXO frequency pull characteristic

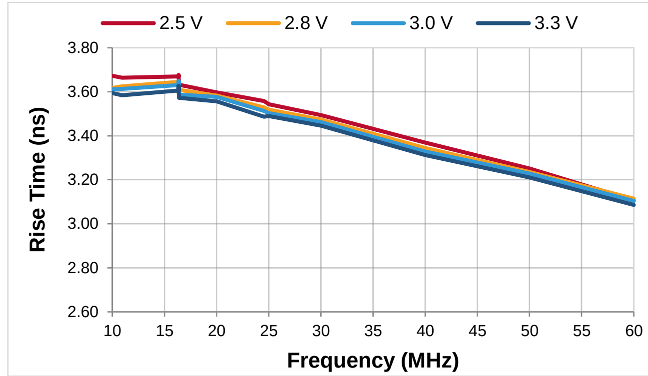


Figure 25. Rise Time (Clipped Sinewave)

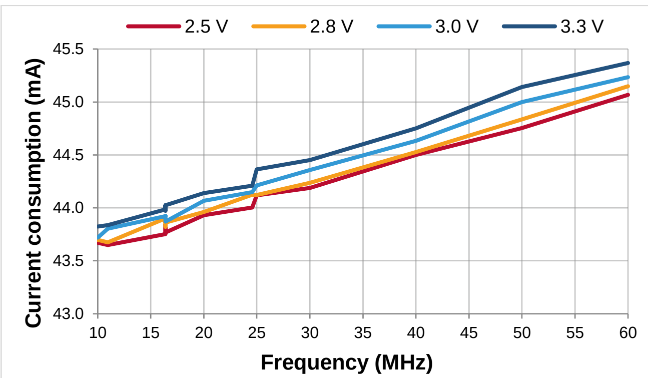


Figure 26. IDD TCXO (Clipped Sinewave)

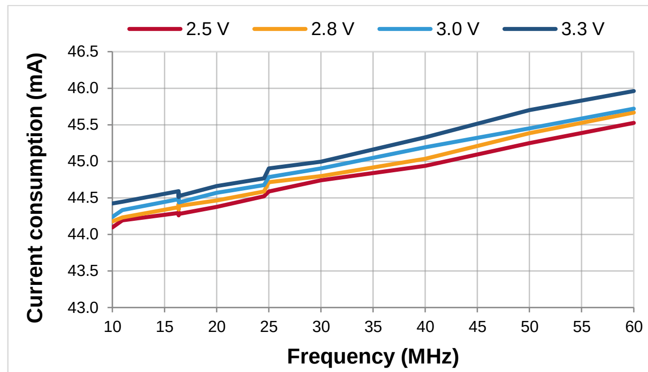


Figure 27. IDD DCTCXO (Clipped Sinewave)

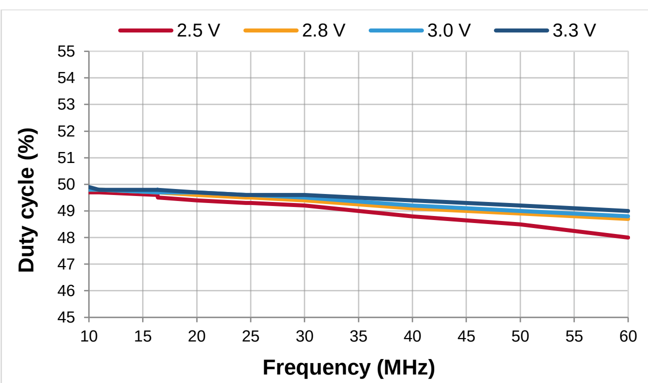


Figure 28. Duty Cycle (Clipped Sinewave)

Architecture Overview

Based on SiTime's innovative Elite Platform®, the SiT5541 delivers exceptional dynamic performance, i.e. resilience to environmental stressors such as shock, vibration, and fast temperature transients. Underpinning the Elite platform are SiTime's unique DualMEMS® temperature sensing architecture and TurboCompensation™ technologies.

DualMEMS is a noiseless temperature compensation scheme. It consists of two MEMS resonators fabricated on the same die substrate. The TempFlat® MEMS resonator is designed with a flat frequency characteristic over temperature whereas the temperature sensing resonator is by design sensitive to temperature changes. The ratio of frequencies between these two resonators provides an accurate reading of the resonator temperature with 20 µK resolution.

By placing the two MEMS resonators on the same die, this temperature sensing scheme eliminates any thermal lag and gradients between resonator and temperature sensor, thereby overcoming an inherent weakness of legacy quartz TCXOs.

The DualMEMS temperature sensor drives a state-of-the-art CMOS temperature compensation circuit. The TurboCompensation design, with >100 Hz compensation bandwidth, achieves a dynamic frequency stability that is far superior to any quartz TCXO. The digital temperature compensation enables additional optimization of frequency stability and frequency slope over temperature within any chosen temperature range for a given system design.

The Elite platform also incorporates a high resolution, low noise frequency synthesizer along with the industry standard I^2C bus. This unique combination enables system designers to digitally control the output frequency in steps as low as 5 ppt and over a wide range up to ±3200 ppm.

For more information regarding the Elite platform and its benefits please visit:

- SiTime's breakthroughs section
- TechPaper: DualMEMS Temperature Sensing Technology
- TechPaper: DualMEMS Resonator TDC

Functional Overview

The SiT5541 is designed for maximum flexibility with an array of factory programmable options, enabling system designers to configure this precision device for optimal performance in a given application.

Output Frequency and Format

The SiT5541 can be factory programmed for an output frequency without sacrificing lead time or incurring an upfront customization cost typically associated with custom-frequency quartz TCXOs.

The device supports both LVCMOS and clipped sinewave output. Ordering codes for the output format are shown below:

Table 11. Output Formats vs. Ordering Codes

Output Format	Ordering Code
LVCMOS	"-"
Clipped Sinewave	"C"

Output Frequency Tuning

In addition to the non-pullable TCXO, the SiT5541 can also support output frequency tuning through an I^2C interface (DCTCXO). The I^2C interface enables 16 factory programmed pull-range options from ±6.25 ppm to ±3200 ppm. The pull range can also be reprogrammed via I^2C to any supported pull-range value. Refer to Device Configuration section for details.

Pin 1 Configuration (OE, VC, or NC)

Pin 1 of the SiT5541 can be factory programmed to support two modes: Output Enable (OE) or No Connect (NC).

Table 12. Pin Configuration Options

Pin 1 Configuration	Operating Mode	Output
OE	TCXO/DCTCXO	Active or High-Z
NC	TCXO/DCTCXO	Active

When pin 1 is configured as OE pin, the device output is guaranteed to operate in one of the following two states:

- Clock output with the frequency specified in the part number when Pin 1 is pulled to logic high
- Hi-Z mode with weak pull down when pin 1 is pulled to logic low.

When pin 1 is configured as NC, the device is guaranteed to output the frequency specified in the part number at all times, regardless of the logic level on pin 1.

Device Configurations

The SiT5541 supports 2 device configurations – TCXO and DCTCXO. The TCXO option is directly compatible with the quartz TCXO. The DCTCXO configuration provides performance enhancement by eliminating VCTCXO's sensitivity to control voltage noise with an I^2C digital interface for frequency tuning.

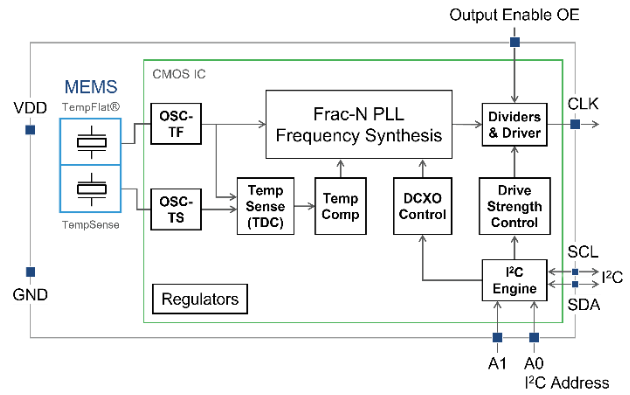


Figure 29. Block Diagram – TCXO

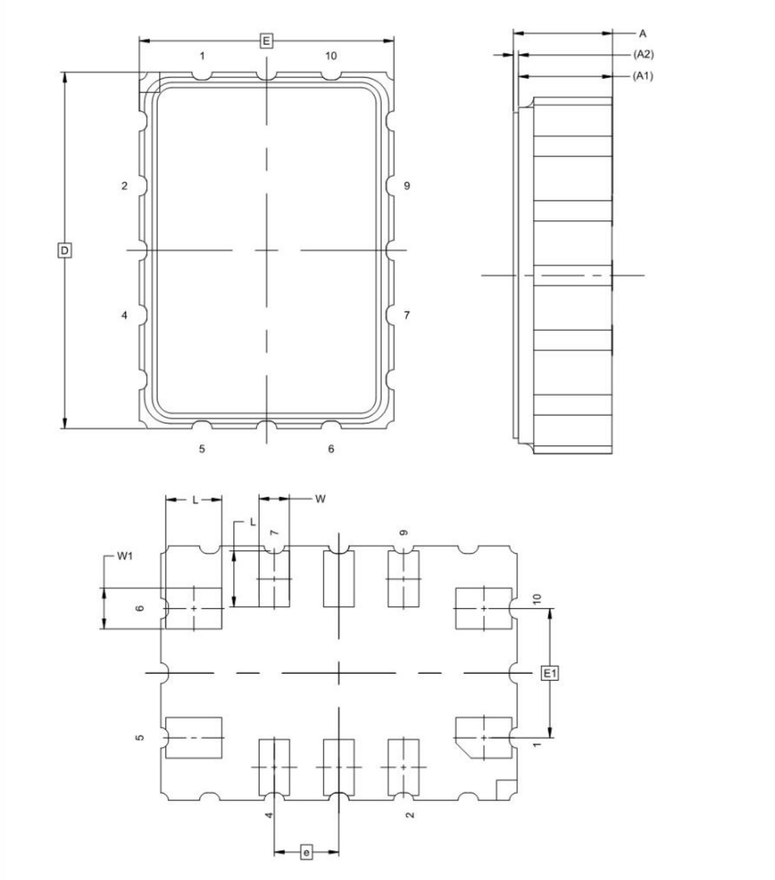
TCXO Configuration

The TCXO configuration generates a fixed frequency output, as shown in Figure 29. The frequency is specified by the user in the frequency field of the device ordering code and then factory programmed. Other factory programmable options include supply voltage, output types (LVCMOS or clipped sinewave), and pin 1 functionality (OE or NC).

Refer to the Ordering Information section at the end of the datasheet for a list of all ordering options.

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A			2.2000
CERAMIC THICKNESS	A1		1.85 ref	
LID THICKNESS	A2		0.100 ref	
BODY SIZE X	D		7 BSC	
BODY SIZE Y	E		5 BSC	
LEAD WIDTH	W	0.550	0.600	0.650
LEAD WIDTH	W1	0.750	0.800	0.850
LEAD LENGTH	L	1.050	1.100	1.150
LEAD PITCH	e		1.27 BSC	
LEAD PITCH	e1		2.54 BSC	
PACKAGE EDGE TOLERANCE	aaa		0.150	
COPLANARITY	ccc		0.080	

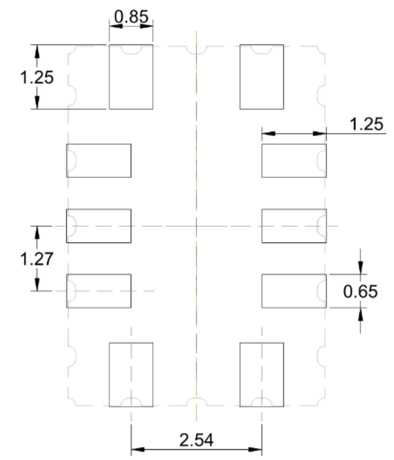
NOTE

1. ALL DIMENSION IN MM

SiTime

PKG INFO	DRAWING NO.	
10L CQFN 7.000x5.00X2.2 mm	POD-086-CQFN-010-X7050	
	REV	SHEET
DATE 6/30/2021	A00	01

Recommended Land Pattern (Unit: mm)



Note : All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.	
		SPL-086-CQFN-010-C07050	
DATE	10L CQFN 5.000x7.000 mm	REV	SHEET
02/03/2023		01	01

- RoHS and REACH compliant
- Pb-free, Halogen-free, Antimony-free

Table 13. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Evaluation Boards	SiT6723DM Evaluation Board User Manual	Contact SiTime
Demo Board	SiT6702DM Demo Board User Manual	Contact SiTime
Time Machine II	MEMS oscillator programmer	http://www.sitime.com/support/time-machine-oscillator-programmer
Time Master Web-based Configurator	Web tool to establish proper programming	https://www.sitime.com/time-master-web-based-configurator
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/api/gated/Manufacturing-Notes-for-SiTime-Products.pdf
Qualification Reports	RoHS report, reliability reports, composition reports	
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	Contact SiTime
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Revision History

Table 14. Revision History

Version	Release Date	Change Summary
1.03	13-Mar-2024	Updated *I²C Device Address Modes* section. Various updates. Production release update
1.1	11-Oct-2024	Updated 20 year stability, added Ultra-low g-sensitivity option (“B”)

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Appendix

DCTCXO Device Configuration

The SiT5541 offers digital control of the output frequency, as shown in Figure 30. The output frequency is controlled by writing frequency control words over the I^2C interface.

There are several advantages of DCTCXOs relative to VCTCXOs:

1) Frequency control resolution as low as 5 ppt. This high resolution minimizes accumulated time error in synchronization applications.
2) Lower system cost – A VCTCXO may need a Digital to Analog Converter (DAC) to drive the control voltage input. In a DCTCXO, the frequency control is achieved digitally by register writes to the control registers via I^2C, thereby eliminating the need for a DAC.
3) Better noise immunity – The analog signal used to drive the voltage control pin of a VCTCXO can be sensitive to noise, and the trace over which the signal is routed can be susceptible to noise coupling from the system. The DCTCXO does not suffer from analog noise coupling since the frequency control is performed digitally through I^2C.

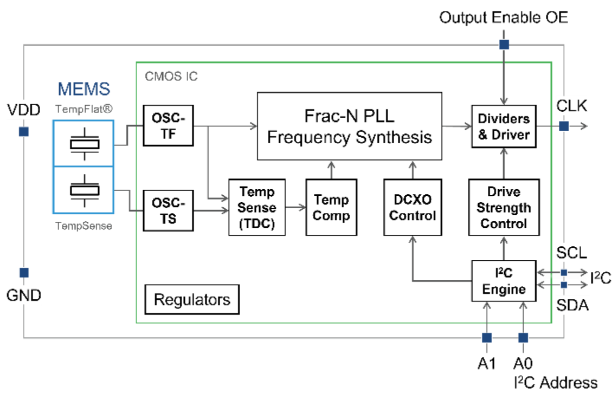

Figure 30. Block Diagram

4) No frequency-pull non-linearity – The frequency pulling is achieved via fractional feedback divider of the PLL, eliminating any pull non-linearity concerns typical of quartz-based VCTCXOs. This improves dynamic performance in closed-loop applications.
5) Programmable wide pull range – The DCTCXO pulling mechanism is via the fractional feedback divider and is therefore not constrained by resonator pullability as in quartz-based solutions. The SiT5541 offers 16 frequency pull-range options from ±6.25 ppm to ±3200 ppm, providing system designers great flexibility.

Refer to DCTCXO-Specific Design Considerations for more information on critical DCTCXO parameters including pull range, absolute pull range, frequency output, and I^2C control registers.

DCTCXO-Specific Design Considerations

Pull Range and Absolute Pull Range

Pull range and absolute pull range are described in the previous section. Table 15 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

Table 15. APR Options[13]

Pull Range Ordering Code	Pull Range ppm	APR ppm ±10 ppb option	APR ppm ±20 ppb option
T	±6.25	±5.84	±5.68
R	±10	±9.59	±9.43
Q	±12.5	±12.09	±11.93
M	±25	±24.59	±24.43
B	±50	±49.59	±49.43
C	±80	±79.59	±79.43
E	±100	±99.59	±99.43
F	±125	±124.59	±124.43
G	±150	±149.59	±149.43
H	±200	±199.59	±199.43
X	±400	±399.59	±399.43
L	±600	±599.59	±599.43
Y	±800	±799.59	±799.43
S	±1200	±1199.59	±1199.43
Z	±1600	±1599.59	±1599.43
U	±3200	±3199.59	±3199.43

Notes:

13. APR includes initial tolerance, frequency stability vs. temperature, and the indicated 20-year aging.

Output Frequency

The device powers up at the nominal operating frequency and pull range specified by the ordering code. After power-up both pull range and output frequency can be controlled via I²C writes to the respective control registers. The maximum output frequency change is constrained by the pull range limits.

The pull range is specified by the value loaded in the digital pull-range control register. The 16 pull range choices are specified in the control register and range from ±6.25 ppm to ±3200 ppm.

Table 16 below shows the frequency resolution versus pull range programmed value

Table 16. Frequency Resolution versus Pull Range

Programmed Pull Range	Frequency Resolution
±6.25 ppm	$5x10^{-12}$
±10 ppm	$5x10^{-12}$
±12.5 ppm	$5x10^{-12}$
±25 ppm	$5x10^{-12}$
±50 ppm	$5x10^{-12}$
±80 ppm	$5x10^{-12}$
±100 ppm	$5x10^{-12}$
±120 ppm	$5x10^{-12}$
±150 ppm	$5x10^{-12}$
±200 ppm	$5x10^{-12}$
±400 ppm	$1x10^{-11}$
±600 ppm	$1.4x10^{-11}$
±800 ppm	$2.1x10^{-11}$
±1200 ppm	$3.2x10^{-11}$
±1600 ppm	$4.7x10^{-11}$
±3200 ppm	$9.4x10^{-11}$

The ppm frequency offset is specified by the 26 bit DCXO frequency control register in two's complement format as described in the I²C Register Descriptions. The power up default value is 00000000000000000000000000b which sets the output frequency at its nominal value (0 ppm). To change the output frequency, a frequency control word is written to 0x00[15:0] (Least Significant Word) and 0x01[9:0] (Most Significant Word). The LSW value should be written first followed by the MSW value; the frequency change is initiated after the MSW value is written.

Bits	25:24	23:20	19:16	15:12	11:8	7:4	3:0
Value (Hex)	01	1111	1111	1111	1111	1111	1111
Dec. Value	2^{25} -1 = 33,554,431						

Bits	25:24	23:20	19:16	15:12	11:8	7:4	3:0
Value (Hex)	00	0000	0000	0000	0000	0000	0000
Dec. Value	0						

Bits	25:24	23:20	19:16	15:12	11:8	7:4	3:0
Value (Hex)	10	0000	0000	0000	0000	0000	0000
Dec. Value	-(2^{25}) = -33,554,432						

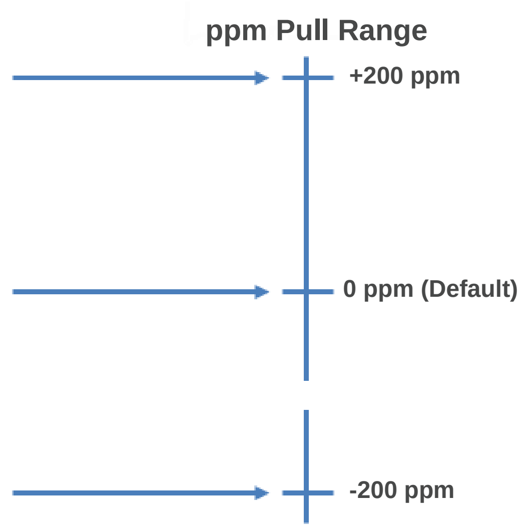

Figure 31. Pull Range and Frequency Control Word

Figure 31 shows how the two's complement signed value of the frequency control word sets the output frequency within the ppm pull range set by 0x02:[3:0]. This example shows use of the ±200 ppm pull range. Therefore, to set the desired output frequency, one just needs to calculate the fraction of full scale value ppm, convert to two's complement binary, and then write these values to the frequency control registers.

The following formula generates the control word value:

Control word value = RND((2^{25}-1) × ppm shift from nominal/pull range), where RND is the rounding function which rounds the number to the nearest whole number. Two examples follow, assuming a ±200 ppm pull range:

Example 1:

- Default Output Frequency = 19.2 MHz
- Desired Output Frequency = 19.201728 MHz (+90 ppm)

2^{25}-1 corresponds to +200 ppm, and the fractional value required for +90 ppm can be calculated as follows.

- 90 ppm / 200 ppm × (2^{25}-1) = 15,099,493.95.

Rounding to the nearest whole number yields 15,099,494 and converting to two's complement gives a binary value of 111001100110011001100110, or E66666 in hex.

Example 2:

- Default Output Frequency = 10 MHz
- Desired Output Frequency = 9.9995 MHz (-50 ppm)

Following the formula shown above,

- (-50 ppm / 200 ppm) × (2^{25}) = -8,388,608.

Converting this to two's complement binary results in 11100000000000000000000000, or 3800000 in hex.

To summarize, the procedure for calculating the frequency control word associated with a given ppm offset is as follows:

1) Calculate the fraction of the half-pull range needed. For example, if the total pull range is set for ±100 ppm and a +20 ppm shift from the nominal frequency is needed, this fraction is 20 ppm/100 ppm = 0.2
2) Multiply this fraction by the full-half scale word value, 2^{25}-1 = 33,554,431, round to the nearest whole number, and convert the result to two's complement binary. Following the +20 ppm example, this value is 0.2 × 33,554,431 = 6,710,886.2 and rounded to 6,710,886.
3) Write the two's complement binary value starting with the Least Significant Word (LSW) 0x00[16:0], followed by the Most Significant Word (MSW), 0x01[9:0]. If the user desires that the output remains enabled while changing the frequency, a 1 must also be written to the OE control bit 0x01[10] if the device has software OE Control Enabled.

It is important to note that the maximum Digital Control update rate is 38 kHz regardless of I^2C bus speed.

I²C Control Registers

The SiT5541 enables control of frequency pull range, frequency pull value, and Output Enable via I²C writes to the control registers. Table 17 below shows the register map summary, and detailed register descriptions follow.

Table 17. Register Map Summary

Address	Bits	Access	Description
0x00	[15:0]	RW	DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW)
0x01	[15:11]	R	NOT USED
	[10]	RW	OE Control. This bit is only active if the output enable function is under software control. If the device is configured for hardware control using the OE pin, writing to this bit has no effect.
	[9:0]	RW	DIGITAL FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW)
0x02	[15:4]	R	NOT USED
	[3:0]	RW	DIGITAL PULL RANGE CONTROL

Register Descriptions

Register Address: 0x00. Digital Frequency Control Least Significant Word (LSW)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW)[15:0]															

Bits	Name	Access	Description
15:0	DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD	RW	Bits [15:0] are the lower 16 bits of the 26 bit FrequencyControlWord and are the Least Significant Word (LSW). The upper 10 bits are in regsiter 0x01[9:0] and are the Most Significant Word (MSW). The lower 16 bits together with the upper 10 bits specify a 26-bit frequency control word. This power-up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After power-up, the system can write to these two registers to pull the frequency across the pull range. The register values are two's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the previous section.

Register Address: 0x01. OE Control, Digital Frequency Control Most Significant Word (MSW)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	NOT USED					OE	DCXO FREQUENCY CONTROL[9:0] MSW									

Bits	Name	Access	Description
15:11	NOT USED	R	Bits [15:10] are read only and return all 0's when read. Writing to these bits has no effect.
10	OE Control	RW	Output Enable Software Control. Allows the user to enable and disable the output driver via I^2C. 0 = Output Disabled (Default) 1 = Output Enabled This bit is only active if the Output Enable function is under software control. If the device is configured for hardware control using the OE pin, writing to this bit has no effect.
9:0	DIGITAL FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW)	RW	Bits [9:0] are the upper 10 bits of the 26 bit FrequencyControlWord and are the Most Significant Word (MSW). The lower 16 bits are in register 0x00[15:0] and are the Least Significant Word (LSW). These lower 16 bits together with the upper 10 bits specify a 26-bit frequency control word. This power-up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After power-up, the system can write to these two registers to pull the frequency across the pull range. The register values are two's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the previous section.

Register Address: 0x02. DIGITAL PULL RANGE CONTROL[14]

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X
Name	NONE												DIGITAL PULL RANGE CONTROL			

Notes:

14. Default values are factory set but can be over-written after power-up.

Bits	Name	Access	Description
15:4	NONE	R	Bits [15:4] are read only and return all 0's when read. Writing to these bits has no effect.
3:0	DIGITAL PULL RANGE CONTROL	RW	Sets the digital pull range of the DCXO. The table below shows the available pull range values and associated bit settings. The default value is factory programmed. **Bit** **3 2 1 0** 0 0 0 0: ±6.25 ppm 0 0 0 1: ±10 ppm 0 0 1 0: ±12.5 ppm 0 0 1 1: ±25 ppm 0 1 0 0: ±50 ppm 0 1 0 1: ±80 ppm 0 1 1 0: ±100 ppm 0 1 1 1: ±125 ppm 1 0 0 0: ±150 ppm 1 0 0 1: ±200 ppm 1 0 1 0: ±400 ppm 1 0 1 1: ±600 ppm 1 1 0 0: ±800 ppm 1 1 0 1: ±1200 ppm 1 1 1 0: ±1600 ppm 1 1 1 1: ±3200 ppm

Serial Interface Configuration Description

The SiT5541 includes an I²C interface to access registers that control the DCTCXO frequency pull range, and frequency pull value. The SiT5541 I²C slave-only interface supports clock speeds up to 1 Mbit/s. The SiT5541 I²C module is based on the I²C specification, UM1024 (Rev.6 April 4, 2014 of NXP Semiconductor).

Serial Signal Format

The SDA line must be stable during the high period of the SCL. SDA transitions are allowed only during SCL low level for data communication. Only one transition is allowed during the low SCL state to communicate one bit of data. Figure 32 shows the detailed timing diagram.

An idle I²C bus state occurs when both SCL and SDA are not being driven by any master and are therefore in a logic HI state due to the pull up resistors. Every transaction begins with a START (S) signal and ends with a STOP (P) signal. A START condition is defined by a high to low transition on the SDA while SCL is high. A STOP condition is defined by a low to high transition on the SDA while SCL is high. START and STOP conditions are always generated by the master. This slave module also supports repeated START (Sr) condition which is same as START condition instead of STOP condition (the blue-color line shows repeated START in Figure 33).

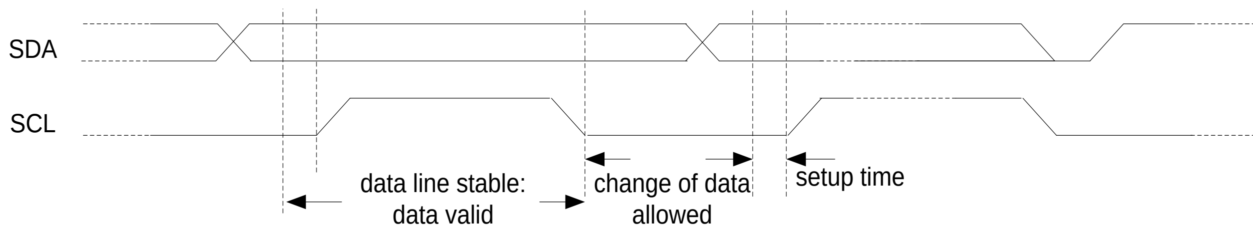

Figure 32. Data and clock timing relation in I²C bus

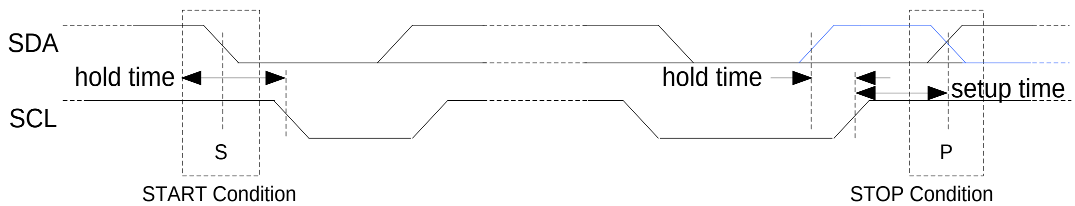

Figure 33. START and STOP (or repeated START, blue line) condition

Parallel Signal Format

Every data byte is 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the MSB (Most Significant Bit) first. The detailed data transfer format is shown in Figure 35 below.

The acknowledge bit must occur after every byte transfer and it allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The acknowledge signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. Setup and hold times must also be taken into account. When SDA remains high during this ninth clock pulse, this is defined as the Not-Acknowledge signal (NACK). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer. The only condition that leads to the generation of NACK from the SiT5541 is when the transmitted address does not match the slave address. When the master is reading data from the SiT5541, the SiT5541 expects the ACK from the master at the end of received data, so that the slave releases the SDA line and the master can generate the STOP or repeated START. If there is a NACK signal at the end of the data, then the SiT5541 tries to send the next data. If the first bit of the next data is “0”, then the SiT5541 holds the SDA line to “0”, thereby blocking the master from generating a STOP/(re)START signal.

Parallel Data Format

This I^{2}C slave module supports 7-bit device addressing format. The 8th bit is a read/write bit and “1” indicates a read transaction and a “0” indicates a write transaction. The register addresses are 8-bits long with an address range of 0 to 255 (00h to FFh). Auto address incrementing is supported which allows data to be transferred to contiguous addresses without the need to write each address beyond the first address. Since the maximum register address value is 255, the address will roll from 255 back to 0 when auto address incrementing is used. Obviously, auto address incrementing should only be used for writing to contiguous addresses. The data format is 16-bit (two bytes) with the most significant byte being transferred first. For a read operation, the starting register address must be written first. If that is omitted, reading will start from the last address in the auto-increment counter of the device, which has a startup default of 0x00.

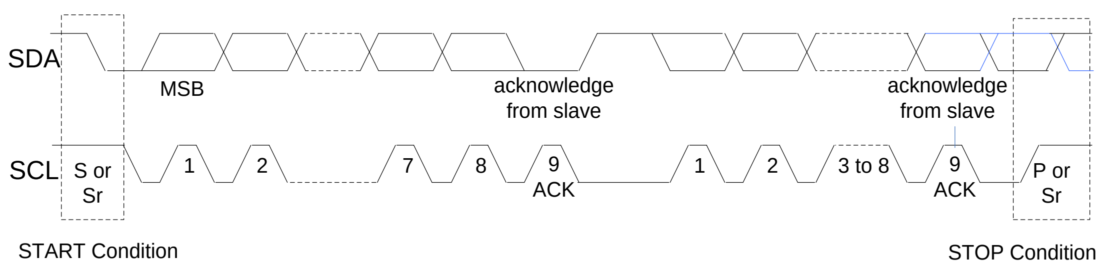

Figure 34. Parallel signaling format

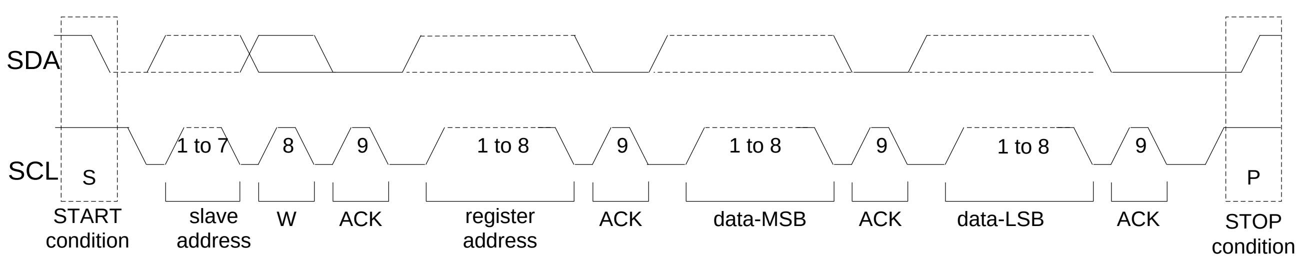

Figure 35. Parallel data byte format, write operation

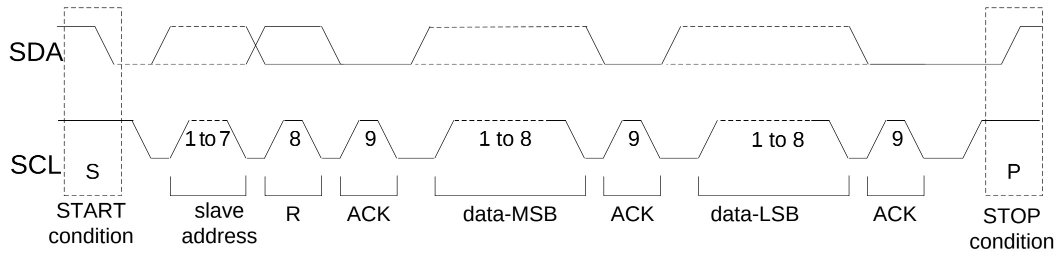

Figure 36. Parallel data byte format, read operation

Figure 37 below shows the I²C sequence for writing the 4-byte control word using auto address incrementing.

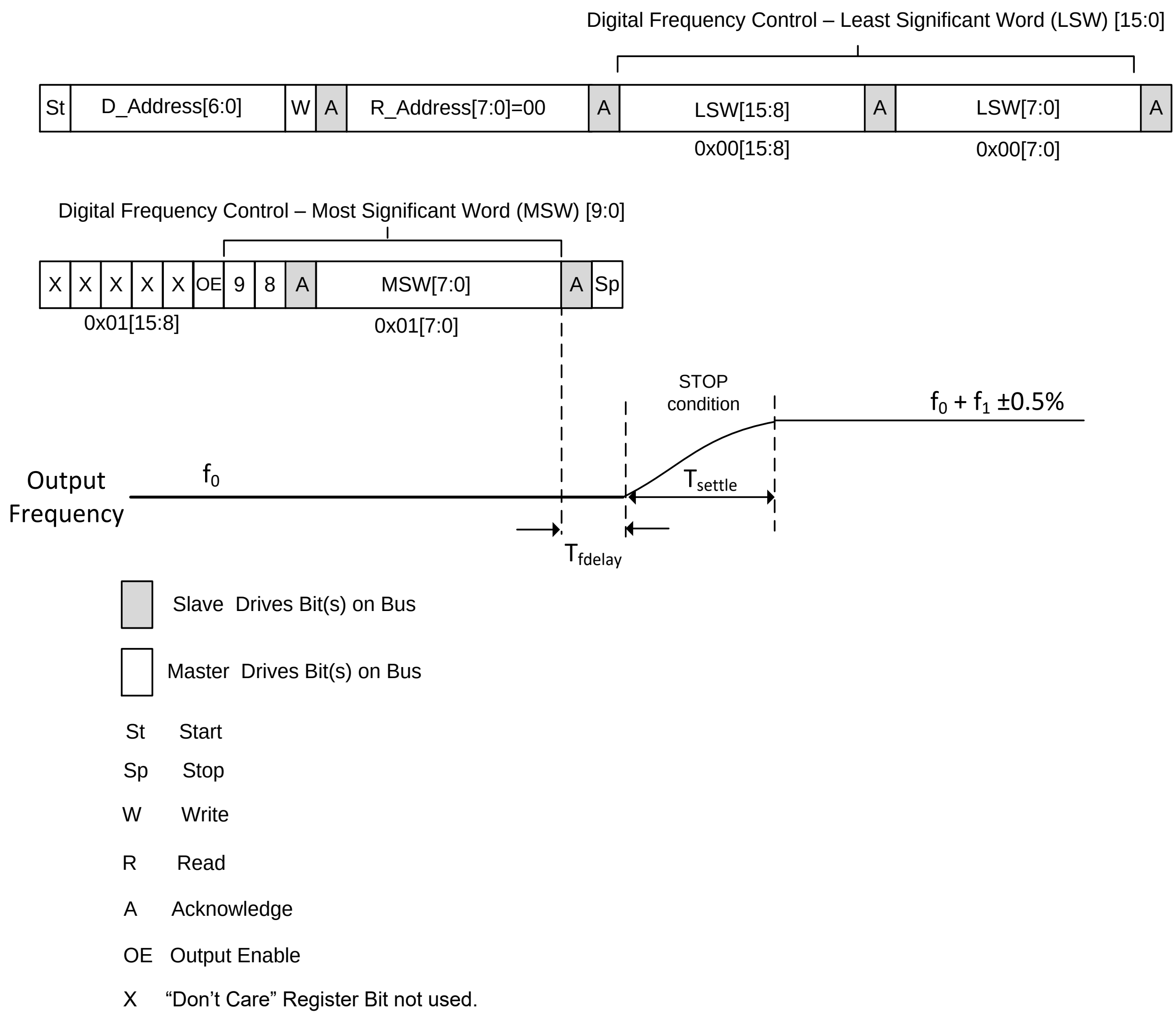

Figure 37. Writing the Frequency Control Word

Table 18. DCTCXO Delay and Settling Time

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency Change Delay	T_{fdelay}	–	103	140	µs	Time from end of 0x01 reg MSW to start of frequency pull, as shown in Figure 37
Frequency Settling Time	T_{settle}	–	16.5	20	µs	Time to settle to 0.5% of frequency offset, as shown in Figure 37

I²C Timing Specification

The below timing diagram and table illustrate the timing relationships for both master and slave.

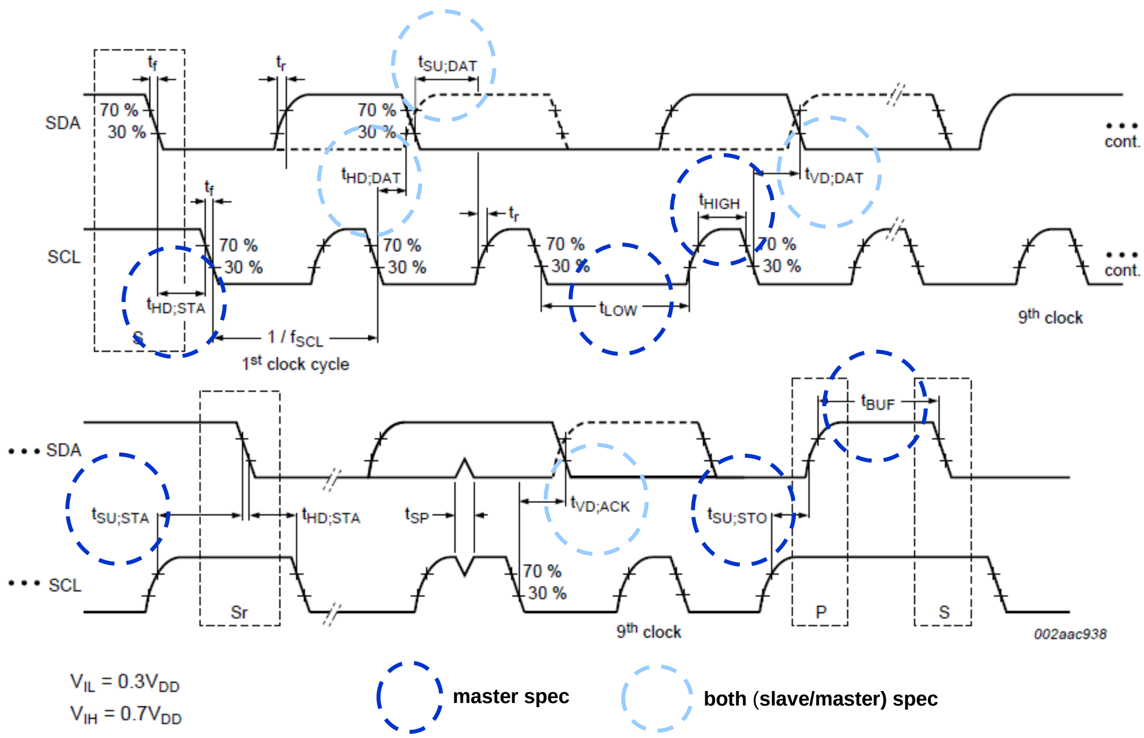

Figure 38. I²C Timing Diagram

Table 19. I²C Timing Requirements

Parameter	Speed Mode	Value	Unit
t_{SETUP}	FM+ (1 MHz)	> 50	nsec
	FM (400 KHz)	> 100	nsec
	SM (100 KHz)	> 250	nsec
t_{HOLD}	FM+ (1 MHz)	> 0	nsec
	FM (400 KHz)	> 0	nsec
	SM (100 KHz)	> 0	nsec
$t_{VD:AWK}$	FM+	> 450	nsec
	FM (400 KHz)	> 900	nsec
	SM (100 KHz)	> 3450	nsec
$t_{VD:DAT}$		NA (s-awk + s-data)/(m-awk/s-data)	

I²C Device Address Modes

There are two I²C address modes:

1) Factory Programmed Mode. The lower 4 bits of the 7-bit device address are set by ordering code as shown in Table 20 below. There are 16 factory programmed addresses available. In this mode, pins 7 and 8 is NC and the A0/A1 I²C address pin control function is not available .

2) A0/A1 Pin Control. This mode allows the user to select between two I²C Device addresses as shown in Table 21.

Table 20. Factory Programmed I²C Address Control[15]

I²C Address Ordering Code	Device I²C Address
0	1100000
1	1100001
2	1100010
3	1100011
4	1100100
5	1100101
6	1100110
7	1100111
8	1101000
9	1101001
A	1101010
B	1101011
C	1101100
D	1101101
E	1101110
F	1101111

Notes:

15. Table 20 is only valid for the DCTCXO device option which supports I²C Control.

Table 21. Pin Selectable I²C Address Control[16]

A1 Pin 8	A0 Pin 7	I²C Address
0	**0**	1100000
0	**1**	1100010
1	**0**	1101000
1	**1**	1101010 (Default)

Notes:

16. Table 21 is only valid for the DCTCXO device option which supports I²C control with A0 and A1 Device Address Control Pins.

Schematic Example

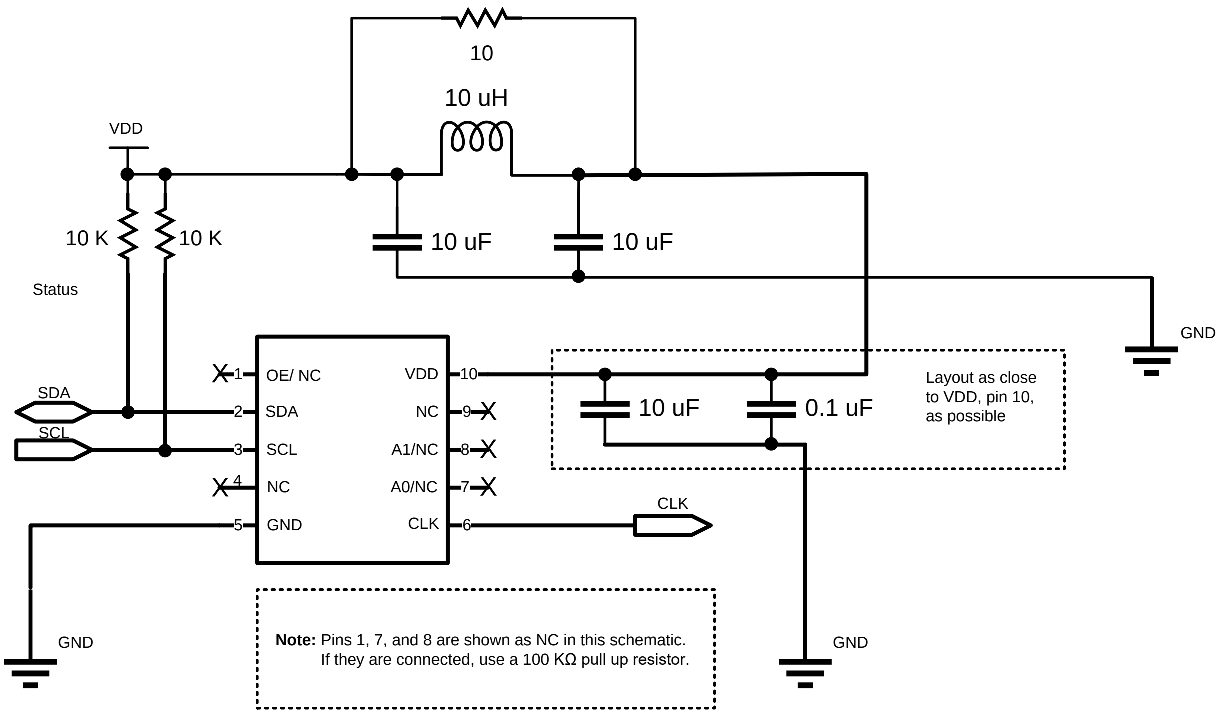

Figure 39. DCTCXO schematic example