SiT5008

Low Power TCXO

Features

- Any frequency between 10 MHz and 60 MHz accurate to 6 decimal places
- 100% pin-to-pin drop-in replacement to quartz-based XO
- ±2 ppm frequency stability (0°C to 80°C)
- Operating temperature from -40°C to 85°C
- Low power consumption of 3.5 mA typical at 1.8 V
- Standby mode for longer battery life
- Fast startup time of 5 ms
- LVCMOS/HCMOS compatible output
- 2 Industry-standard packages: 2.0 x 1.6 mm x mm, 2.5 x 2.0 mm x mm
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

Applications

- Smart meter
- IoT
- Low power wireless
- Connected audio/video

Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

Table 1. Electrical Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	10	–	60	MHz	
Frequency Stability and Aging						
Initial Tolerance	F_init	-3.5	–	+3.5	ppm	At 25°C
Stability over Temperature	F_stab	-2	–	+2	ppm	0°C to 80°C, at rated nominal power supply voltage and load. Referenced to (max frequency + min frequency)/2 over the rated temperature range
		-10	–	+10	ppm	-40°C to 85°C, at rated nominal power supply voltage and load. Referenced to (max frequency + min frequency)/2 over the rated temperature range
First year aging	F_aging	-2	–	+2	ppm	At 25°C
Operating Temperature Range						
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial
Supply Voltage and Current Consumption						
Supply Voltage	Vdd	1.62	1.8	1.98	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd	–	3.9	4.6	mA	No load condition, f = 26 MHz, Vdd = 2.8, 3.3 V
		–	3.6	4.2	mA	No load condition, f = 26 MHz, Vdd = 1.8 Vs
OE Disable Current	I_OD	–	–	4.2	mA	Vdd = 2.8 V, 3.3 V, OE = GND, Output in high-Z state
		–	–	4.0	mA	Vdd = 1.8 V, OE = GND, Output in high-Z state
Standby Current	I_std	–	2.1	4.3	µA	ST = GND, Vdd = 2.8 V, 3.3V. Output is weakly pulled down
		–	0.2	1.3	µA	ST = GND, Vdd = 1.8 V, Output is weakly pulled down
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	All Vdds. See Duty Cycle definition in Figure 3 and Footnote 6
Rise/Fall Time	Tr, Tf	–	1	2	ns	Vdd = 2.8 V, 3.3 V, 20% - 80%
		–	1.3	2.5	ns	Vdd = 1.8 V, 20% - 80%
Output High Voltage	VOH	90%	–	–	Vdd	IOH = -4 mA (Vdd = 3.3 V) IOH = -3 mA (Vdd = 2.8 V) IOH = -2 mA (Vdd = 1.8 V)
Output Low Voltage	VOL	–	–	10%	Vdd	IOL = 4 mA (Vdd = 3.3 V) IOL = 3 mA (Vdd = 2.8 V) IOL = 2 mA (Vdd = 1.8 V)

Table 1. Electrical Characteristics (continued)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics						
Input High Voltage	VIH	70%	–	–	Vdd	Pin 1, OE or ST
Input Low Voltage	VIL	–	–	30%	Vdd	Pin 1, OE or ST
Input Pull-up Impedance	Z_in	50	87	150	kΩ	Pin 1, OE logic high or logic low, or ST logic high
		2	–	–	MΩ	Pin 1, ST logic low
Startup and Resume Timing						
Startup Time	T_start	–	–	5	ms	Measured from the time Vdd reaches its rated minimum value
Enable/Disable Time	T_oe	–	–	150	ns	f =60 MHz. For other frequencies, T_oe = 100 ns + 3*cycles
Resume Time	T_resume	–	–	5	ms	Measured from the time ST pin crosses 50% threshold
Jitter						
RMS Period Jitter	T_jitt	–	1.8	3	ps	f = 26 MHz
Peak-to-peak Period Jitter	T_pk	–	14	30	ps	f = 26 MHz
RMS Phase Jitter (random)	T_phj	–	1.3	2	ps	f = 26 MHz, Integration bandwidth = 12 kHz to 5 MHz
Phase Noise						
10 Hz offset		–	-32	–	dBc/Hz	F_nom = 26 MHz
100 Hz Offset		–	-80	–	dBc/Hz	
1 kHz offset		–	-127	–	dBc/Hz	
10 kHz offset		–	-135	–	dBc/Hz	
100 kHz offset		–	-136	–	dBc/Hz	
1 MHz offset		–	-147	–	dBc/Hz	
5 MHz offset		–	-157	–	dBc/Hz	

Table 2. Pin Description

Pin	Symbol		Functionality
1	OE/$\overline{ST}$/NC	Output Enable	H[1]: specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby	H[1]: specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.
		No Connect	Any voltage between 0 and Vdd or Open[1]: Specified frequency output. Pin 1 has no function.
2	GND	Power	Electrical ground
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage[2]

Top View

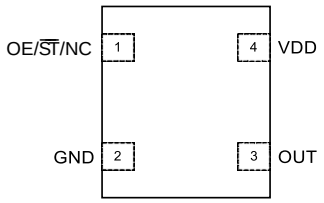


Figure 1. Pin Assignments

Notes:

1. In OE or $\overline{ST}$ mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
2. A capacitor of value 0.1 µF or higher between Vdd and GND is required.

Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Vdd	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Junction Temperature[3]	–	150	°C

Note:

3. Exceeding this temperature for extended period of time may damage the device.

Table 4. Thermal Consideration[4]

Package	θJA, 4 Layer Board (°C/W)	θJA, 2 Layer Board (°C/W)	θJC, Bottom (°C/W)
2520	117	222	26

Note:

4. Refer to JESD51 for θJA and θJC definitions, and reference layout used to determine the θJA and θJC values in the above table.

Table 5. Maximum Operating Junction Temperature[5]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
85°C	95°C

Note:

5. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 6. Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	**MIL-STD-883F, Method 2002**
Mechanical Vibration	**MIL-STD-883F, Method 2007**
Temperature Cycle	**JESD22, Method A104**
Solderability	**MIL-STD-883F, Method 2003**
Moisture Sensitivity Level	**MSL1 @ 260°C**

Test Circuit and Waveform[6]

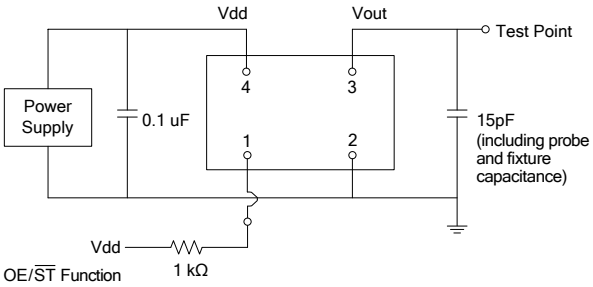


Figure 2. Test Circuit

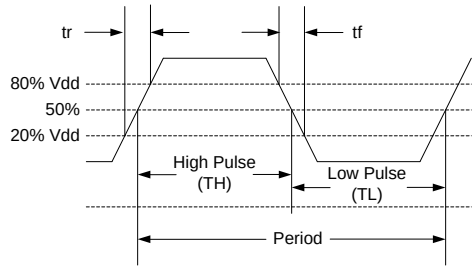


Figure 3. Waveform

Note:

6. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagrams

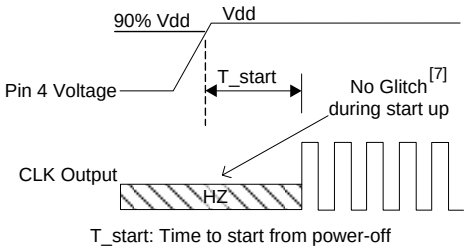


Figure 4. Startup Timing (OE/ST Mode)

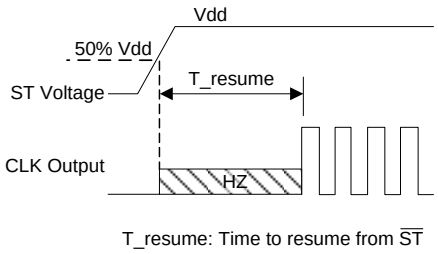


Figure 5. Standby Resume Timing (ST Mode Only)

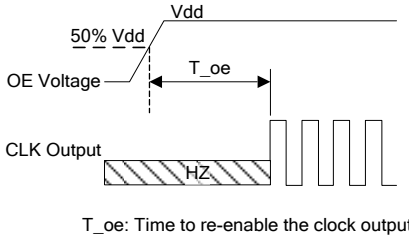


Figure 6. OE Enable Timing (OE Mode Only)

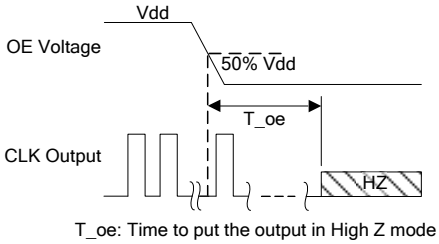


Figure 7. OE Disable Timing (OE Mode Only)

Note:

7. SiT5008 has “no runt” pulses and “no glitch” output during startup or resume.

Programmable Drive Strength

The SiT5008 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time.
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the SiTime Application Notes section.

EMI Reduction by Slowing Rise/Fall Time

Figure 8 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

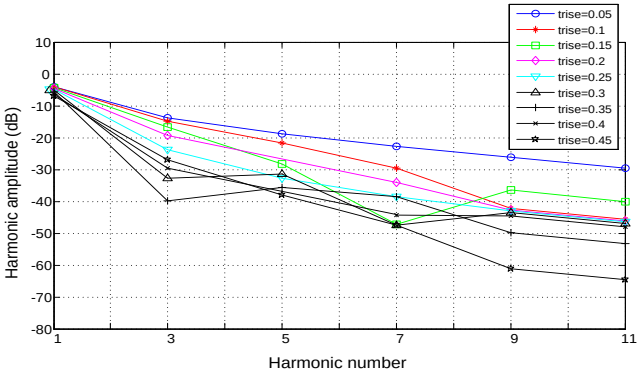


Figure 8. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the down-stream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the Rise/Fall Time Tables (Table 7 to Table 9) to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 2.8 V SiT5008 device with default drive strength setting, the typical rise/fall time is 1 ns for 15 pF output load. The typical rise/fall time slows down to 2.82 ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 2.2 ns by then increasing the drive strength setting on the SiT5008.

The SiT5008 can support up to 60 pF or higher in maximum capacitive loads with drive strength settings. Refer to the Rise/Fall Time Tables (Table 7 to 9) to determine the proper drive strength for the desired combination of output load vs. rise/fall time.

SiT5008 Drive Strength Selection

Tables 7 through 9 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the SiT5008 nominal supply voltage (1.8 V, 2.8 V, 3.3 V)
2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Any given rise/fall time in Table 7 to 9 dictates the maximum frequency under which the oscillator can operate with guaranteed full output swing over the entire operating temperature range. This max frequency can be calculated as the following:

$$\text{Max Frequency} = \frac{1}{5 \times \text{Trf\_20/80}}$$

where Trf_20/80 is the typical value for 20%-80% rise/fall time.

Example 1

Calculate f_{MAX} for the following condition:

- Vdd = 1.8 V (Table 7)
- Capacitive Load: 30 pF
- Desired Tr/f time = 3 ns
  (rise/fall time part number code = E)
- f_{MAX} = 66.666660

Part number for the above example:

SiT5008BI**E**12-18E-66.666660

Drive strength code is inserted here. Default setting is "-"

Rise/Fall Time (20% to 80%) vs C_{LOAD} Tables

Table 7. Vdd = 1.8 V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	6.16	11.61	22.00	31.27	39.91
A	3.19	6.35	11.00	16.01	21.52
R	2.11	4.31	7.65	10.77	14.47
B	1.65	3.23	5.79	8.18	11.08
T	0.93	1.91	3.32	4.66	6.48
E	0.78	1.66	2.94	4.09	5.74
U	0.70	1.48	2.64	3.68	5.09
F or "-": default	0.65	1.30	2.40	3.35	4.56

Table 8. Vdd = 2.8 V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	3.77	7.54	12.28	19.57	25.27
A	1.94	3.90	7.03	10.24	13.34
R	1.29	2.57	4.72	7.01	9.06
B	0.97	2.00	3.54	5.43	6.93
T	0.55	1.12	2.08	3.22	4.08
E or "-": default	0.44	1.00	1.83	2.82	3.67
U	0.34	0.88	1.64	2.52	3.30
F	0.29	0.81	1.48	2.29	2.99

Table 9. Vdd = 3.3 V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	3.39	6.88	11.6	17.5	23.5
A	1.74	3.50	6.38	8.98	12.1
R	1.16	2.33	4.29	6.04	8.34
B	0.81	1.82	3.22	4.52	6.33
T or "-": default	0.46	1.00	1.86	2.60	3.84
E	0.33	0.87	1.64	2.30	3.35
U	0.28	0.79	1.46	2.05	2.93
F	0.25	0.72	1.31	1.83	2.61

Pin 1 Configuration Options (OE, $\overline{ST}$, or NC)

Pin 1 of the SiT5008 can be factory-programmed to support three modes: Output Enable (OE), standby ($\overline{ST}$) or No Connect (NC). These modes can also be programmed with the Time Machine using field programmable devices.

Output Enable (OE) Mode

In the OE mode, applying logic Low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in <1 µs.

Standby ($\overline{ST}$) Mode

In the $\overline{ST}$ mode, a device enters into the standby mode when Pin 1 pulled Low. All internal circuits of the device are turned off. The current is reduced to a standby current, typically in the range of a few µA. When $\overline{ST}$ is pulled High, the device goes through the "resume" process, which can take up to 5 ms.

No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and outputs the specified frequency regardless of the logic level on pin 1.

Table 10 below summarizes the key relevant parameters in the operation of the device in OE, $\overline{ST}$, or NC mode.

Table 10. OE vs. $\overline{ST}$ vs. NC

	OE	$\overline{ST}$	NC
Active current 20 MHz (max, 1.8 V)	4.1 mA	4.1 mA	4.1 mA
OE disable current (max. 1.8 V)	4 mA	N/A	N/A
Standby current (typical 1.8 V)	N/A	0.6 µA	N/A
OE enable time at 77.76 MHz (max)	138 ns	N/A	N/A
Resume time from standby (max, all frequency)	N/A	5 ms	N/A
Output driver in OE disable/standby mode	High Z	weak pull-down	N/A

Output on Startup and Resume

The SiT5008 comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup or resume from the standby mode.

In addition, the SiT5008 features "no runt" pulses and "no glitch" output during startup or resume as shown in the waveform captures in Figure 9 and Figure 10.

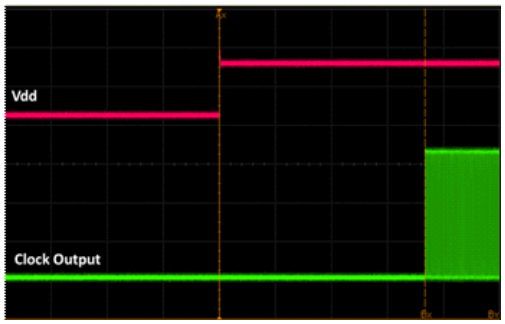


Figure 9. Startup Waveform vs. Vdd

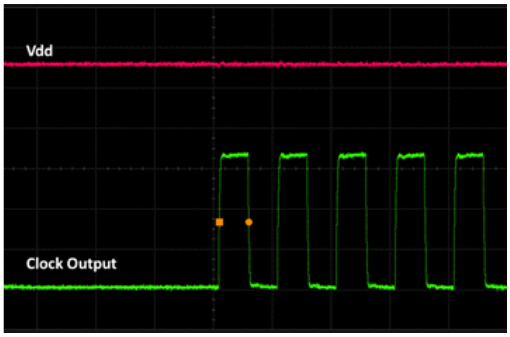
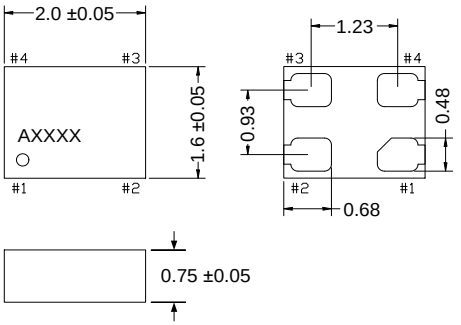
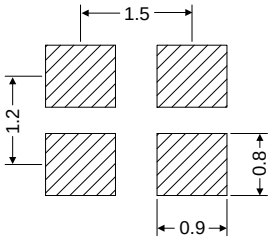
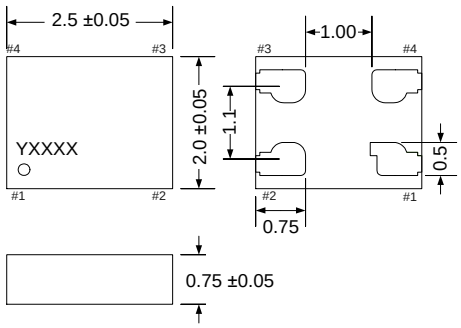
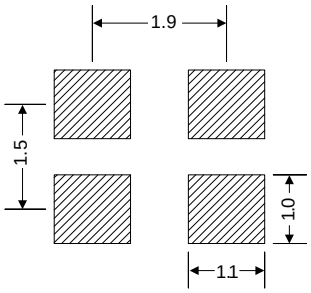


Figure 10. Startup Waveform vs. Vdd (Zoomed-in View of Figure 9)

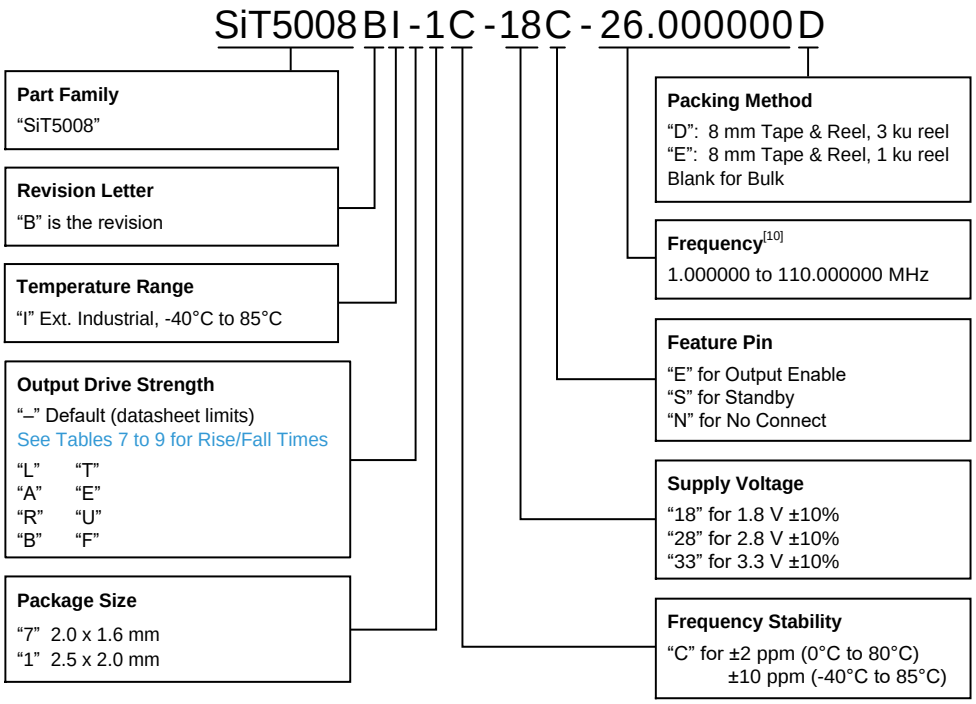
Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[8]	Recommended Land Pattern (Unit: mm)[9]
2.0 x 1.6 x 0.75 mm 	
2.5 x 2.0 x 0.75 mm 	

Notes:

8. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
9. A capacitor of value 0.1 µF or higher between Vdd and GND is required.

Ordering Information



Note:

10. The 26 MHz version of the device in 2.5 x 2.0 mm is in production. Contact SiTime for availability of other configurations.

Table 11. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	16 mm T&R (3 ku)	16 mm T&R (1 ku)	12 mm T&R (3 ku)	12 mm T&R (1 ku)	8 mm T&R (3 ku)	8 mm T&R (1 ku)
2.0 x 1.6	–	–	–	–	D	E
2.5 x 2.0	–	–	–	–	D	E

Table 12. Revision History

Revision	Release Date	Change Summary
0.1	3-Apr-2017	Initial draft
0.90	3-Dec-2020	Updated with detailed stability spec
0.91	4-Dec-2020	Updated stability spec, added phase noise for 26 MHz
0.92	7-Dec-2020	Fixed the ordering code for temp. range
0.93	16-Dec-2020	Fixed the ordering code for drive strength “L” Updated Rise/Fall Time Tables
0.98	8-Feb-2021	Added 3.3 V option
1.0	17-Feb-2021	Final release

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439

Supplemental Information

The Supplemental Information section is not part of the datasheet and is for informational purposes only.

Best Reliability

Silicon is inherently more reliable than quartz. Unlike quartz suppliers, SiTime has in-house MEMS and analog CMOS expertise, which allows SiTime to develop the most reliable products. Figure 1 shows a comparison with quartz technology.

Why is SiTime MEMS Best in Class:

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal™ process, which eliminates foreign particles and improves long term aging and reliability
- World-class MEMS and CMOS design expertise

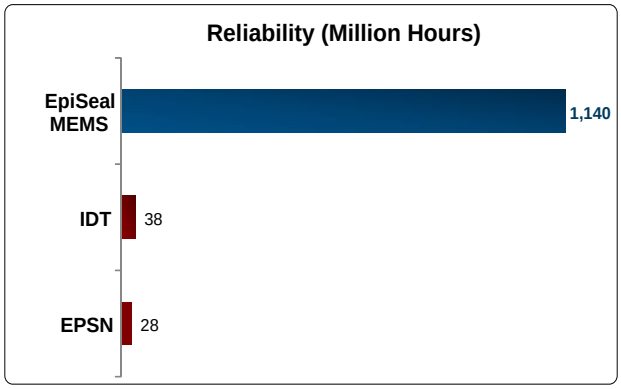


Figure 1. Reliability Comparison[1]

Best Aging

Unlike quartz, MEMS oscillators have excellent long term aging performance which is why every new SiTime product specifies 10-year aging. A comparison is shown in Figure 2.

Why is SiTime Best in Class:

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal™ process, which eliminates foreign particles and improves long term aging and reliability
- Inherently better immunity of electrostatically driven MEMS resonator

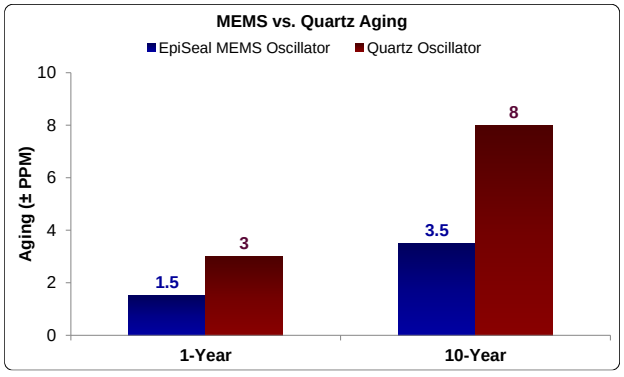


Figure 2. Aging Comparison[2]

Best Electro Magnetic Susceptibility (EMS)

SiTime's oscillators in plastic packages are up to 54 times more immune to external electromagnetic fields than quartz oscillators as shown in Figure 3.

Why is SiTime Best in Class:

- Internal differential architecture for best common mode noise rejection
- Electrostatically driven MEMS resonator is more immune to EMS

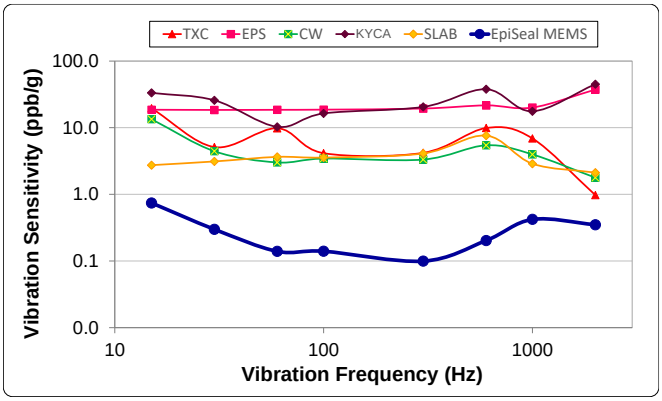


Figure 3. Electro Magnetic Susceptibility (EMS)[3]

Best Power Supply Noise Rejection

SiTime's MEMS oscillators are more resilient against noise on the power supply. A comparison is shown in Figure 4.

Why is SiTime Best in Class:

- On-chip regulators and internal differential architecture for common mode noise rejection
- MEMS resonator is paired with advanced analog CMOS IC

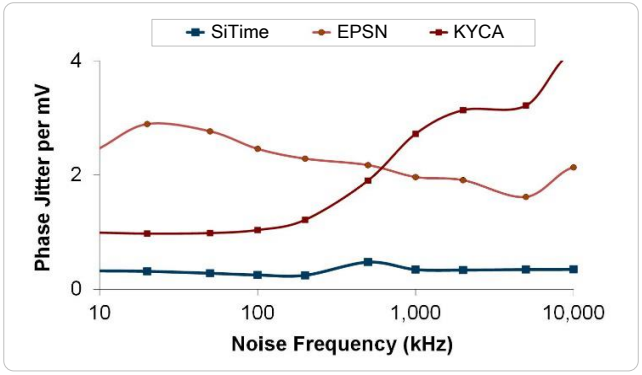


Figure 4. Power Supply Noise Rejection[4]

Best Vibration Robustness

High-vibration environments are all around us. All electronics, from handheld devices to enterprise servers and storage systems are subject to vibration. Figure 5 shows a comparison of vibration robustness.

Why is SiTime Best in Class:

- The moving mass of SiTime's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

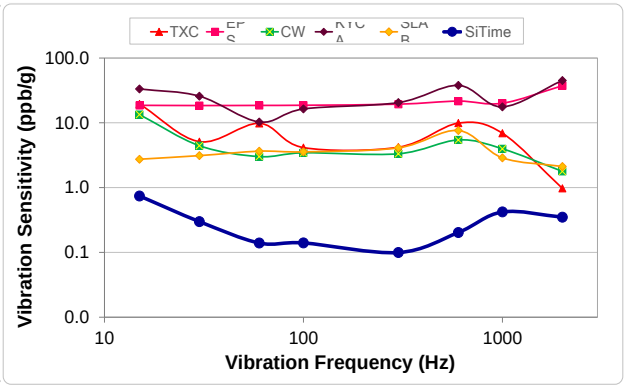


Figure 5. Vibration Robustness[5]

Best Shock Robustness

SiTime's oscillators can withstand at least 50,000 *g* shock. They all maintain their electrical performance in operation during shock events. A comparison with quartz devices is shown in Figure 6.

Why is SiTime Best in Class:

- The moving mass of SiTime's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

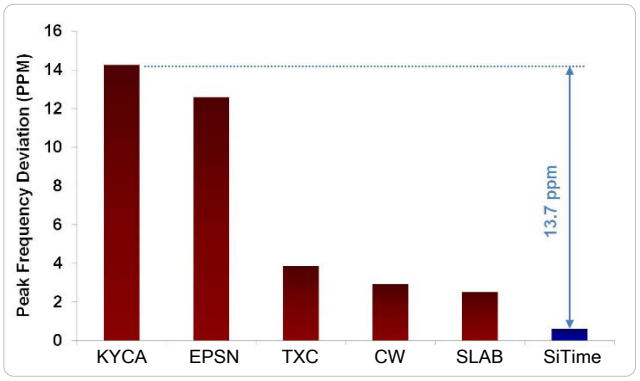


Figure 6. Shock Robustness[6]

Figure labels:

- TXC = TXC
- Epson = EPSN
- Connor Winfield = CW
- Kyocera = KYCA
- SiLabs = SLAB
- SiTime = EpiSeal MEMS

Notes:

1. Data source: Reliability documents of named companies.
2. Data source: SiTime and quartz oscillator devices datasheets.
3. Test conditions for Electro Magnetic Susceptibility (EMS):
   - According to IEC EN61000-4.3 (Electromagnetic compatibility standard)
   - Field strength: 3V/m
   - Radiated signal modulation: AM 1 kHz at 80% depth
   - Carrier frequency scan: 80 MHz – 1 GHz in 1% steps
   - Antenna polarization: Vertical
   - DUT position: Center aligned to antenna

   Devices used in this test:

Label	Manufacturer	Part Number	Technology
EpiSeal MEMS	SiTime	SiT9120AC-1D2-33E156.250000	MEMS + PLL
EPSN	Epson	EG-2102CA156.2500M-PHPAL3	Quartz, SAW
TXC	TXC	BB-156.250MBE-T	Quartz, 3rd Overtone
CW	Conner Winfield	P123-156.25M	Quartz, 3rd Overtone
KYCA	AVX Kyocera	KC7050T156.250P30E00	Quartz, SAW
SLAB	SiLab	590AB-BDG	Quartz, 3rd Overtone + PLL

4. 50 mV pk-pk Sinusoidal voltage.

   Devices used in this test:

Label	Manufacturer	Part Number	Technology
EpiSeal MEMS	SiTime	SiT8208AI-33-33E-25.000000	MEMS + PLL
NDK	NDK	NZ2523SB-25.6M	Quartz
KYCA	AVX Kyocera	KC2016B25M0C1GE00	Quartz
EPSN	Epson	SG-310SCF-25M0-MB3	Quartz

5. Devices used in this test:

   same as EMS test stated in Note 3.
6. Test conditions for shock test:
   - MIL-STD-883F Method 2002
   - Condition A: half sine wave shock pulse, 500-g, 1ms
   - Continuous frequency measurement in 100 µs gate time for 10 seconds

   Devices used in this test:

   same as EMS test stated in Note 3.
7. Additional data, including setup and detailed results, is available upon request to qualified customer. Please contact productsupport@sitime.com.