# SiT3901

Ultra-Small µPower Digitally Controlled Oscillator

## Description

The SiT3901 is the industry's smallest and the lowest power digitally controlled MHz oscillator. With 0.4 mW of active power consumption at 6.78 MHz and 2.6 MHz output frequencies, this µPower oscillator enables longer battery life for consumer, IoT and wearable devices compared to a quartz-based oscillator or resonator.

The device comes in a small 1.5 mm x 0.8 mm package. The unique combination of ultra-low power, ultra-small package and flexible output frequency makes it ideal for power sensitive and space constrained applications.

## Applications

- Tablets
- Fitness bands
- Health and medical monitoring
- Wearables
- Portable audio
- Input devices
- IoT devices

## Features

- Ultra-low current consumption of 105 µA at 2.6 MHz and 220 µA at 6.78 MHz
- ±50,000 ppm - ±150,000 ppm pull range
- Ultra-small 1.5 mm x 0.8 mm package
- 2.6 MHz and 6.78 MHz with 6 decimal places of accuracy
- Operating temperature from -40°C to 85°C
- Frequency stability as low as ±50 ppm
- Programmable output drive strength for best EMI or driving multiple loads
- Ultra-light weight of 1.28 mg
- RoHS and REACH compliant, PFAS-free, Pb-free, Halogen-free and Antimony-free

TempFlat® MEMS

## Electrical Specifications

### Table 1. Electrical Characteristics for 6.78 MHz output

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Frequency Range** | | | | | | |
| **Output Frequency Range** | f | – | 6.78 | – | MHz | Contact SiTime for other frequencies up to 26 MHz |
| **Frequency Stability and Aging** | | | | | | |
| **Initial Tolerance** | f_tol | -6,000 | – | +6,000 | ppm | Frequency offset at 25°C post reflow |
| **Frequency Stability** | f_stab | -100 | – | +100 | ppm | Inclusive of variations over operating temperature -20°C to +70°C or -40°C to +85°C, rated power supply voltage and output load. |
| | | -50 | – | +50 | ppm | Inclusive of variations over operating temperature -20°C to +70°C, rated power supply voltage and output load. |
| **Pull Range** | PR | -50,000 | – | +50,000 | | |
| **First Year Aging** | f_1year | -3 | – | +3 | ppm | At 25°C |
| **Operating Temperature Range** | | | | | | |
| **Operating Temperature Range** | T_use | -20 | – | +70 | °C | Extended Commercial |
| | | -40 | – | +85 | °C | Industrial. Contact SiTime for -40°C to 105°C option. |
| **Supply Voltage and Current Consumption** | | | | | | |
| **Supply Voltage** | VDD | 1.62 | 1.8 | 1.98 | V | |
| | | 2.25 | – | 3.63 | V | Any voltage from 2.25 to 3.63 V |
| **Current Consumption**[1] | IDD | – | 220 | 270 | µA | f = 6.78 MHz, any voltage, no load |

## Table 1. Electrical Characteristics for 6.78 MHz (continued)

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **LVCMOS Output Characteristics** | | | | | | |
| **Duty Cycle** | DC | 45 | – | 55 | % | |
| **Rise/Fall Time**[3] | T_r, T_f | – | 4 | 8 | ns | Vdd = 1.8 V, 20% - 80%. Contact SiTime for other programmable rise/fall options |
| | | – | – | 8 | ns | Vdd = 2.25 V to 3.63 V, 20% - 80%. Contact SiTime for other programmable rise/fall options |
| **Output High Voltage** | VOH | 90% | – | – | VDD | IOL = 0.5 mA (Vdd = 1.8 V)<br>IOL = 1.2 mA (Vdd = 2.25 V to 3.63 V) |
| **Output Low Voltage** | VOL | – | – | 10% | VDD | IOL = 0.5 mA (Vdd = 1.8 V)<br>IOL = 1.2 mA (Vdd = 2.25 V to 3.63 V) |
| **Input Characteristics** | | | | | | |
| **Input High Voltage** | VIH | 80% | – | – | VDD | |
| **Input Low Voltage** | VIL | – | – | 20% | VDD | |
| **Input Slew Rate** | In-slew | 10 | – | – | V/µs | |
| **Input Pull-down Impedance** | Z_in | 300 | – | – | kΩ | Active mode (DP/OE pin = HIGH), Vdd = 1.8 V |
| | | 270 | – | – | kΩ | Active mode (DP/OE pin = HIGH), Vdd = 2.25 V to 3.63 V |
| | | 2.5 | – | – | MΩ | Output disabled (DP/OE pin = LOW), Vdd = 1.8 V |
| | | 1.3 | – | – | MΩ | Output disabled (DP/OE pin = LOW), Vdd = 2.25 V to 3.63 V |
| **Startup, Standby and Resume Timing** | | | | | | |
| **Startup Time** | T_start | – | 75 | 150 | ms | Measured from the time VDD reaches 90% of its final value |
| **Enable Time** | T_disable | – | – | 20 | µs | Measured from the time OE pin crosses 50% threshold |
| **Disable Time** | T_enable | – | 2 | 3 | ms | Measured from the time OE pin crosses 50% threshold |
| **Standby Time** | T_stdby | – | – | 20 | µs | Measured from the time ST pin crosses 50% threshold |
| **Resume Time** | T_resume | – | 2 | 3 | ms | Measured from the time ST pin crosses 50% threshold |
| **Jitter** | | | | | | |
| **RMS Period Jitter** | T_jitt | – | 80 | 130 | ps | f = 6.78 MHz, any voltage |
| **RMS Phase Jitter** | T_phj | – | 1.5 | 2.5 | ns | f = 6.78 MHz, any voltage,<br>Integration bandwidth = 100 Hz to 40 kHz[2] |

**Notes:**

1. Current consumption with load is a function of the output frequency and output load. For any given output frequency, the capacitive loading will increase current consumption equal to C_load*VDD*f(MHz).
2. Max spec inclusive of 25 mV peak-to-peak sinusoidal noise on VDD. Noise frequency 100 Hz to 20 MHz.

## Table 2. Electrical Characteristics for 2.6 MHz

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Frequency Range** | | | | | | |
| **Output Frequency Range** | F_nom | – | 2.6 | – | MHz | Contact SiTime for other frequencies up to 26 MHz |
| **Frequency Stability and Aging** | | | | | | |
| **Initial Tolerance** | f_tol | -3,500 | – | +3,500 | ppm | Frequency offset at 25°C post reflow |
| **Frequency Stability** | f_stab | -100 | – | +100 | ppm | Frequency offset relative to 25°C. Inclusive of variations over all operating temperatures, rated power supply voltage and output load. |
| | | -50 | – | +50 | ppm | Frequency offset relative to 25°C. Inclusive of variations over operating temperature -20°C to +70°C, rated power supply voltage and output load. |
| **Absolute Pull Range** | PR | -150,000 | – | +150,000 | ppm | Relative to F_nom. |
| **First Year Aging** | f_1year | -3 | – | +3 | ppm | At 25°C |
| **Operating Temperature Range** | | | | | | |
| **Operating Temperature Range** | T_use | -20 | – | +70 | °C | Extended Commercial |
| | | -40 | – | +85 | °C | Industrial. Contact SiTime for -40°C to 105°C option. |
| **Supply Voltage and Current Consumption** | | | | | | |
| **Current Consumption**[3] | IDD | – | 105 | 120 | µA | Inclusive of ±150,000 ppm frequency pull range. Measured with no output load. |
| **Supply Voltage** | VDD | 2.25 | – | 3.63 | V | Any voltage from 2.25 to 3.63 V |
| **LVCMOS Output Characteristics** | | | | | | |
| **Duty Cycle** | DC | 45 | – | 55 | % | |
| **Rise/Fall Time**[4] | T_r, T_f | – | – | 8 | ns | Vdd = 2.25 V to 3.63 V, 20% - 80%. Contact SiTime for other programmable rise/fall options |
| **Output High Voltage** | VOH | 90% | – | – | VDD | IOH = -1.2 mA (Vdd = 2.25 V to 3.63 V) |
| **Output Low Voltage** | VOL | – | – | 10% | VDD | IOL = 1.2 mA (Vdd = 2.25 V to 3.63 V) |
| **Input Characteristics** | | | | | | |
| **Input High Voltage** | VIH | 80% | – | – | VDD | |
| **Input Low Voltage** | VIL | – | – | 20% | VDD | |
| **Input Slew Rate** | In-slew | 10 | – | – | V/µs | |
| **Input Pull-down Impedance** | Z_in | 270 | – | – | kΩ | Active mode (ST pin = LOW), Vdd = 2.25 V to 3.63 V |
| | | 1.3 | – | – | MΩ | Standby mode (ST pin = HIGH), Vdd = 2.25 V to 3.63 V |
| **Startup, Standby and Resume Timing** | | | | | | |
| **Startup Time** | T_start | – | 75 | 150 | ms | Measured from the time VDD reaches 90% of its final value |
| **Enable Time** | T_disable | – | – | 20 | µs | Measured from the time OE pin crosses 50% threshold |
| **Disable Time** | T_enable | – | 2 | 3 | ms | Measured from the time OE pin crosses 50% threshold |
| **Standby Time** | T_stdby | – | – | 20 | µs | Measured from the time ST pin crosses 50% threshold |
| **Resume Time** | T_resume | – | 2 | 3 | ms | Measured from the time ST pin crosses 50% threshold |
| **Jitter** | | | | | | |
| **RMS Period Jitter**[5] | T_jitt | – | 260 | 400 | ps | f = 2.6 MHz, Vdd = 2.25 V to 3.63 V, Inclusive of ±150,000 ppm frequency pull range. |
| **RMS Phase Jitter**[5] | T_phj | – | 1.5 | 2.5 | ns | f = 2.6 MHz, Vdd = 2.25 V to 3.63 V, Integration bandwidth = 100 Hz to 40 kHz[2], Inclusive of ±150,000 ppm frequency pull range. |

**Notes:**

3. Current consumption with load is a function of the output frequency and output load. For any given output frequency, the capacitive loading will increase current consumption equal to C_load*VDD*f(MHz).
4. Max spec inclusive of 25 mV peak-to-peak sinusoidal noise on VDD. Noise frequency 100 Hz to 20 MHz.
5. Refer to the performance plot section for typical values at 2.5, 2.8, 3.0 and 3.3 V condition.

### Table 3. Pin Description

| Pin | Symbol | Functionality | |
|---|---|---|---|
| 1 | DP/OE/ST | Data Programming Pin | Tri-Level One Wire Interface: See “Frequency Control Protocol Description” section for programming details |
| | | Output Enable | Active Low:<br>L: Output driver is disabled<br>H: Specified output frequency<br>Active High:<br>H: Output driver is disabled<br>L: Specified output frequency |
| | | Standby | Active Low:<br>L: Output driver is disabled, device is in standby mode<br>H: Specified output frequency<br>Active High:<br>H: Output driver is disabled, device is in standby mode<br>L: Specified output frequency |
| 2 | OUT | Output | LVCMOS clock output |
| 3 | VDD | Power | Supply voltage. Bypass with a 0.01 µF X7R capacitor. |
| 4 | GND | Power | Connect to ground |

**Top View**

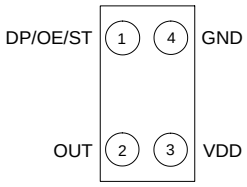



**Figure 1. Pin Assignments**

### Table 4. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Test Condition | Value | Unit |
|---|---|---|---|
| **Continuous Power Supply Voltage Range (VDD)** | | -0.5 to 3.63 | V |
| **Short Duration Maximum Power Supply Voltage (VDD)** | <30 seconds | 4.0 | V |
| **Continuous Maximum Operating Temperature** | | 105 | °C |
| **Short Duration Maximum Operating Temperature** | ≤30 seconds | 125 | °C |
| **Human Body Model (HBM) ESD Protection** | JESD22-A115 | 2000 | V |
| **Charge-Device Model (CDM) ESD Protection** | JESD22-C101 | 750 | V |
| **Machine Model (MM) ESD Protection** | $T_A$ = 25°C | 200 | V |
| **Latch-up Tolerance** | JESD78 Compliant | | |
| **Mechanical Shock Resistance** | MII 883, Method 2002 | 10,000 | *g* |
| **Mechanical Vibration Resistance** | MII 883, Method 2007 | 70 | *g* |
| **1508 CSP Junction Temperature** | | 150 | °C |
| **Storage Temperature** | | -65 to 150 | °C |
| **Soldering Temperature (follow standard Pb free soldering guidelines)** | – | 260 | °C |

## Description

SiT3901 device is a digitally controlled programmable oscillator (DCXO), which allows pulling the frequency around a nominal value dynamically. User can communicate with the device through a 1-pin tri-level serial interface. This device has two DCXO registers, which control the amount of frequency pull. Once the registers are set, the device sets its output frequency to a new value dynamically. The pull range is programmable to a maximum of ±50,000 ppm with a resolution of ±100 ppb. Writing into the DCXO registers does not cause any interruptions of output oscillations; the frequency will switch from one value to the new one smoothly.

### Default Startup Condition

The SiT3901 starts up at its factory programmed frequency. The DCXO registers values are initialized all zeros, effectively setting the frequency to the middle of the control range.

### Frequency Control Protocol Description

The device includes two DCXO registers. Data for each register is written to the device using a data frame.

### Data Frame Format

Each frame consists of 40 bits. A frame has 2 parts:

- Register address, 24 bits
- Pull Frequency (PF) value represented as a 25-bit binary number
- The 25-bit Pull Frequency value is split over the data fields of two frames. One frame carries 9 most significant bits and the other frame carries the remaining 16 bits.

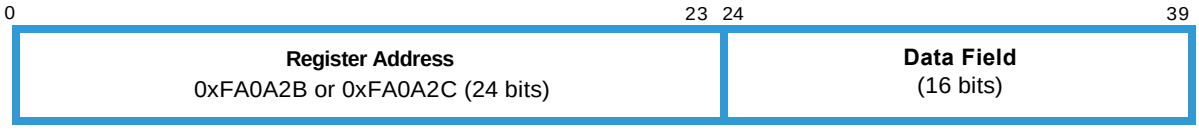



**Figure 2. Data Frame**

To control the output frequency, two frames per frequency update are required, and the frequency is only updated at the end of the second frame. The pull frequency value in this mode is 25 bits. This value is written to the device in two frames as Figure 4. Note that register (address: 0xFA0A2B) carries the most significant 9 bits as indicated by the XXXXXXXXX in Figure 3. The rest of the most significant bits must be set to 0.

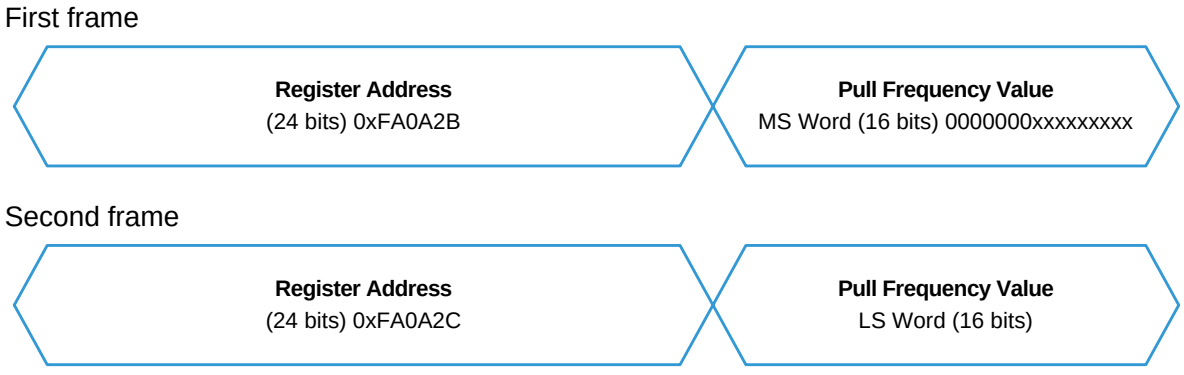



**Figure 3. Frequency Control**

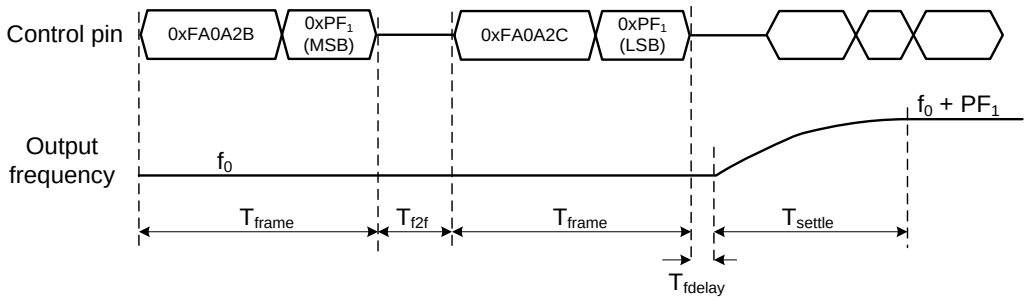



**Figure 4. Frame Timing**

## Frame Timing Parameters

### Table 5. Frame Timing

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Frame Length | $T_{frame}$ | 40 | — | µS |
| Frame to Frame Delay | $T_{f2f}$ | 2 | — | µS |
| Frequency Settling Time | $T_{settle}$ | — | 30 | µS |
| Frame to Frequency Delay | $T_{fdelay}$ | — | 8 | µS |

## Calculating Pull Frequency Values

The frequency pull value (PF) must be encoded as a 25-bit binary number representing the full scale range of the device.

The most significant 9 bits of the frequency pull value are written to the lowest nine bits of the data field at register address 0xFA0A2B. The 7 most significant bits of the data field are written to 0. The least significant 16 bits of the frequency pull value are written to the register address 0xFA0A2C.

Here are the steps to calculate the pull frequency (PF) value:

1. Find the pull frequency value using the equation below where “ppm” is the desired frequency offset from nominal.

Pull Frequency Value

| PF (Pull Frequency Value) |
|---|
| 6.78 MHz: ***PF (±50000 pull range) = 3.2544(1 + ppm/1e6)*** |
| 2.6 MHz: ***PF (±150000 pull range) = 2.49875(1 + ppm/1e6)*** |

2. For any frequency shifts (positive or negative PPM), convert the pull frequency value into a 25-bit binary number.

**Example 1**

This example shows how to shift the frequency by +1000 ppm in a device with ±50000 pull range:

PF = 3.2544(1 + 1000/1e6)

Pull Value Integer = PF*2^23

25 Bit Value = Pull Value Integer XOR (25165824)

MS Data Field = 0000000000100000
LS Data Field = 1111101011010010

Frame for MS Word: 0xFA0A2B [MS Data Field]

Frame for LS Word: 0xFA0A2C [LS Data Field]

**Example 2**

This example shows how to shift the frequency by -25000 ppm in a device with ±50000 pull range:

PF = 3.2544(1 - 25000/1e6)

Pull Value Integer = PF*2^23

25 Bit Value = Pull Value Integer XOR (25165824)

MS Data Field = 0000000000010110
LS Data Field = 0010011000101101

Frame for MS Word: 0xFA0A2B [MS Data Field]

Frame for LS Word: 0xFA0A2C [LS Data Field]

## Physical Interface

The SiTime DCXO uses a serial input interface to adjust the pull frequency value.

The interface uses a one-wire tri-level return-to-middle signaling format. Figure 5 below shows the signal waveform of the interface.

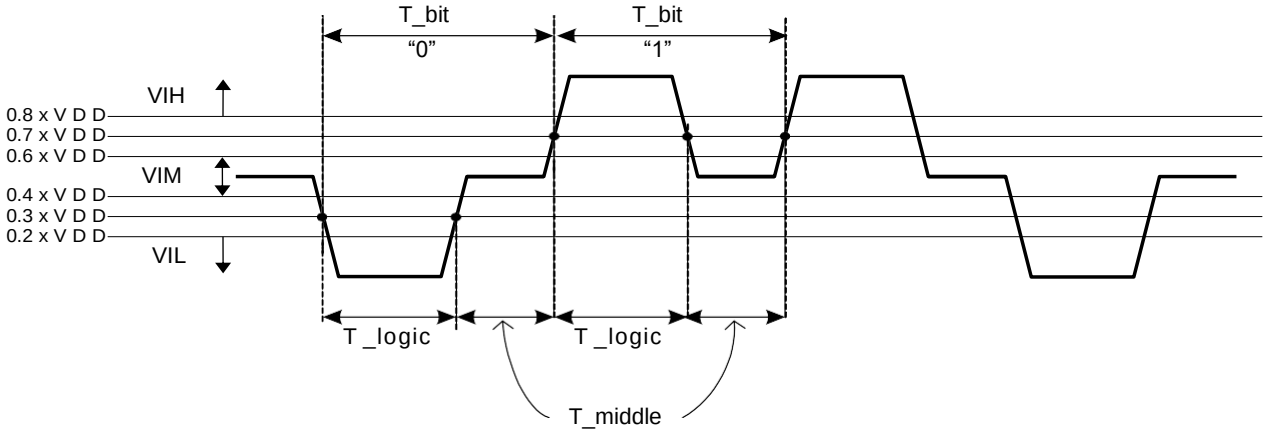



**Figure 5. Serial 1-Wire Tri-Level Signaling**

A logical bit "1" is defined by a high-logic followed by mid-logic. A logical bit "0" is defined by a low-logic followed by mid-logic. The voltage ranges and time durations corresponding to low-logic, high-, and mid-logic are illustrated in Figure 5 and specified in electrical specification table.

The overall baud rate is computed as below:

$$baud\_rate = \frac{1}{T\_bit}$$

Figure 6 shows a simple circuit to generate tri-level circuit with a general purpose IO (GPIO) with tri-state capability. Most FPGAs and micro controllers/processors include such GPIOs. If the GPIO does not support tri-state output, two IOs may be used in combination with external tri-state buffer to generate the tri-level signal; an example of such buffer is the SN74LVC1G126. The waveform at the output of the tri-state buffer is shown in Figure 5. When the GPIO drives Low or High voltage, the rise/fall times are typically fast (sub-5ns range). When the output is set to Hi-Z, the output settles at middle voltage with a RC response. The time constant is determined based on the total capacitance on frequency control pin and the parallel resistance of the pull-up and pull-down resistors. The time constant in most practical situations will be less than 50ns; this necessitate choosing longer T_middle to allow the RC waveform to settle within 5% or so.

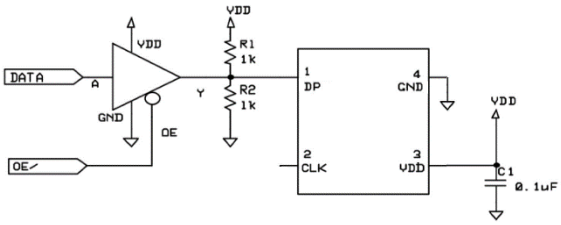



**Figure 6. Circuit Diagram for Generating Tri-Level Signal with Tri-State Buffer**

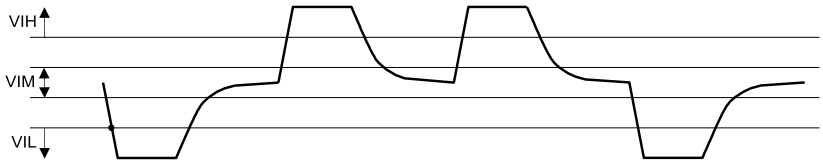



**Figure 7. Tri-State Signal Generated with Tri-State Buffer**

When using a tri-state buffer as shown above, care must be taken if the DATA and OE lines transition at the same time that there are no glitches. A glitch might occur, for example, if the OE line enables the output slightly before the data line has finished its logical transition. One way around this, albeit at the cost of some data overhead, is to use an extra OE cycle on every bit, as shown in Figure 8.

Note that the diagram assumes an SN74LVC125, which has a low-true OE/ line (output is enabled when OE/ is low). For a high-true OE part, such as the SN74LVC126, the polarity of that signal would be reversed.

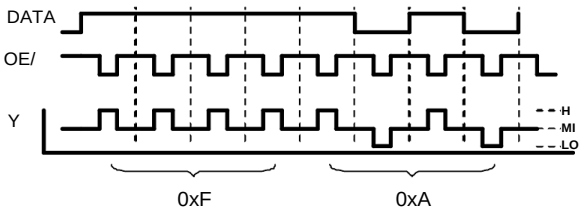



**Figure 8. Signal Polarity**

## Block Diagram

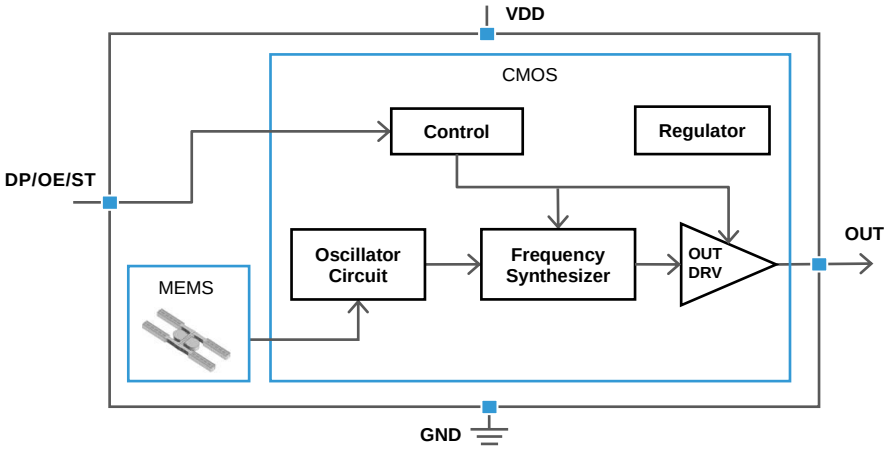



**Figure 9. SiT3901 Block Diagram**

## Changing Device Operating Mode

Upon power cycling, the device defaults to the digital programming mode; pin 1 exhibits DP functionality. Once in output enable (OE) or stand-by (ST) mode, the device must be power cycled to return to digital programming mode. Switching from the digital programming mode to the output enable or stand-by modes is done by writing to two specific separate registers described below. The mode will only change after both registers have been written to. For the both OE and ST modes two polarity options are available: active High and active Low.

The procedure to change to active Low OE mode is the following:

- Write: 0xFA0A00 0040 (clear the DP pin receiver)
- Write: 0xFA0A25 78D3 (switch function from DP to OE)

| Write order | Register address | Data value |
|---|---|---|
| 1 | 0xFA0A00 | 0x0040 |
| 2 | 0xFA0A25 | 0x78D3 |

The procedure to change to active High OE mode is the following:

- Write: 0xFA0A00 0040 (clear the DP pin receiver)
- Write: 0xFA0A25 7853 (switch function from DP to OE)

| Write order | Register address | Data value |
|---|---|---|
| 1 | 0xFA0A00 | 0x0040 |
| 2 | 0xFA0A25 | 0x7853 |

The procedure to change to active Low ST mode is the following:

- Write: 0xFA0A00 0040 (clear the DP pin receiver)
- Write: 0xFA0A25 78B3 (switch function from DP to ST)

| Write order | Register address | Data value |
|---|---|---|
| 1 | 0xFA0A00 | 0x0040 |
| 2 | 0xFA0A25 | 0x78B3 |

The procedure to change to active High ST mode is the following:

- Write: 0xFA0A00 0040 (clear the DP pin receiver)
- Write: 0xFA0A25 7833 (switch function from DP to ST)

| Write order | Register address | Data value |
|---|---|---|
| 1 | 0xFA0A00 | 0x0040 |
| 2 | 0xFA0A25 | 0x7833 |

## Output Enable Mode

Once the device's operation mode has been changed to the output enable mode, a high level on the DP/OE pin will enable the clock output for the active Low OE mode and vice versa for active High OE mode. A low level on the DP/OE pin will disable the output for active Low OE mode and high level will disable it for active high OE as per Table 6.

### Table 6. Operating Modes and Output States

| DP/OE pin | Mode | Output | IDD Example |
|---|---|---|---|
| Active Low | | | |
| LOW | Output Disabled | Hi-Z | 45 µA @ 2.6 MHz |
| HIGH | Output Enabled | Specified frequency | 120 µA @ 2.6 MHz<br>270 µA @ 6.78 MHz |
| Active High | | | |
| HIGH | Output Disabled | Hi-Z | 45 µA @ 2.6 MHz |
| LOW | Output Enabled | Specified frequency | 120 µA @ 2.6 MHz<br>270 µA @ 6.78 MHz |

## Stand-by mode

Once the device's operation mode has been changed to the stand-by mode, a high level on the DP/ST pin will enable the clock output for the active Low ST mode and vice versa for active High ST mode. A low level on the DP/ST pin will disable the output for active Low ST mode and high level will disable it for active high ST as per Table 7.

### Table 7. Operating Modes and Output States

| DP/OE pin | Mode | Output | IDD Example |
|---|---|---|---|
| Active Low | | | |
| LOW | Output Disabled | Weak pull-down | 1.5 µA |
| HIGH | Output Enabled | Specified frequency | 120 µA @ 2.6 MHz<br>270 µA @ 6.78 MHz |
| Active High | | | |
| HIGH | Output Disabled | Weak pull-up | 1.5 µA |
| LOW | Output Enabled | Specified frequency | 120 µA @ 2.6 MHz<br>270 µA @ 6.78 MHz |

## Test Circuit and Waveform

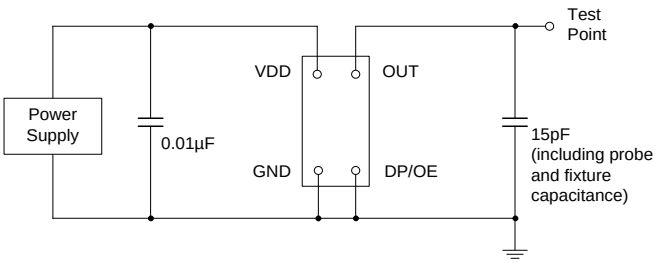



**Figure 10. Test Circuit**

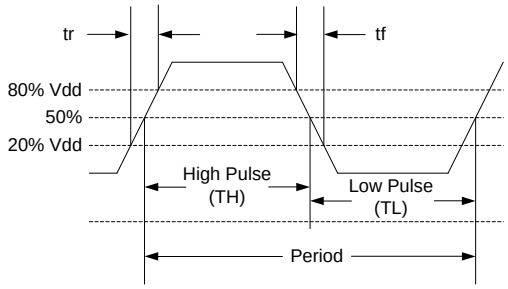
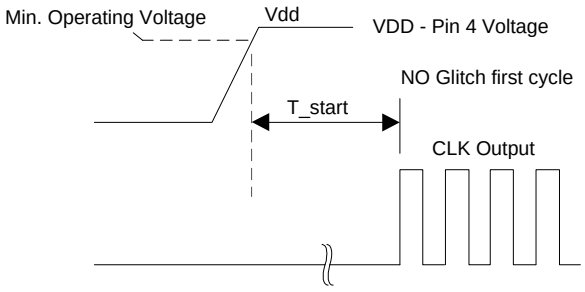



**Figure 11. Waveform[6]**

**Note:**

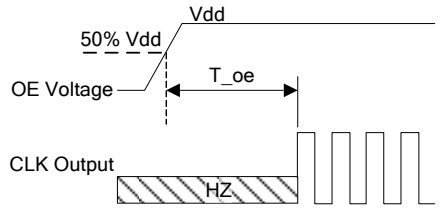
6. Duty Cycle is computed as Duty Cycle = TH/Period.

## Timing Diagram



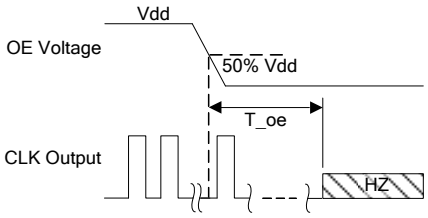

T_start: Time to valid clock output from power on

**Figure 12. Startup Timing[7]**



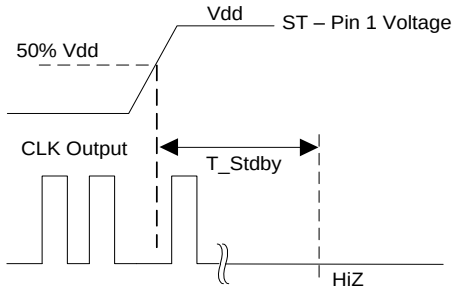

T_oe: Time to re-enable the clock output

**Figure 13. OE Enable Timing (OE Mode Only)**



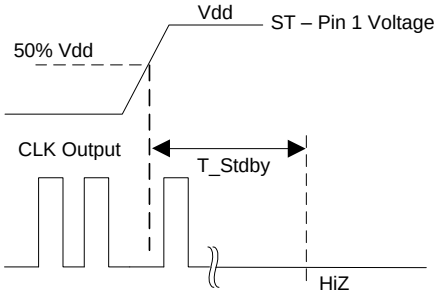

T_oe: Time to put the output in High Z mode

**Figure 14. OE Disable Timing (OE Mode Only)**




T_Stdby: Time for output to go high-Z from the time ST pin crosses 50% threshold

**Figure 15. Resume Timing[7]**




T_Stdby: Time for output to go high-Z from the time ST pin crosses 50% threshold

**Figure 16. Standby Timing[7]**

**Notes:**

7. SiT3901 supports “no runt” pulses and “no glitch” output during startup or resume.

## Performance Plots[8]

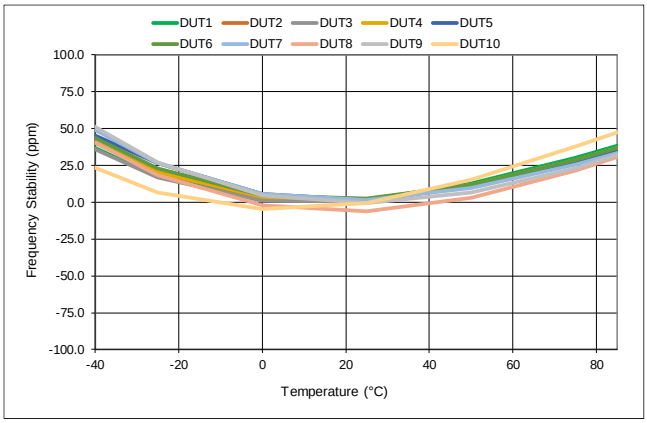



**Figure 17. Frequency vs Temperature**

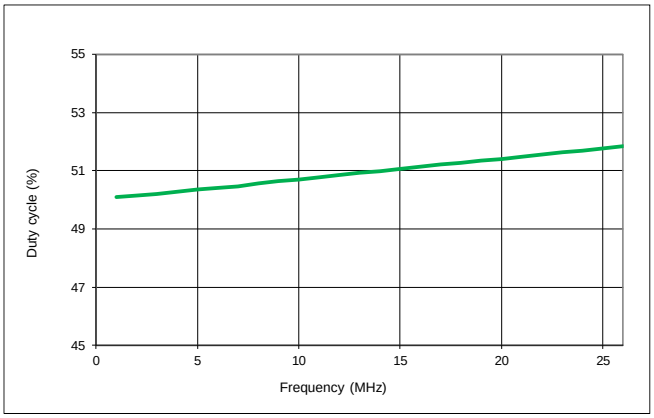



**Figure 18. Duty Cycle vs Frequency**

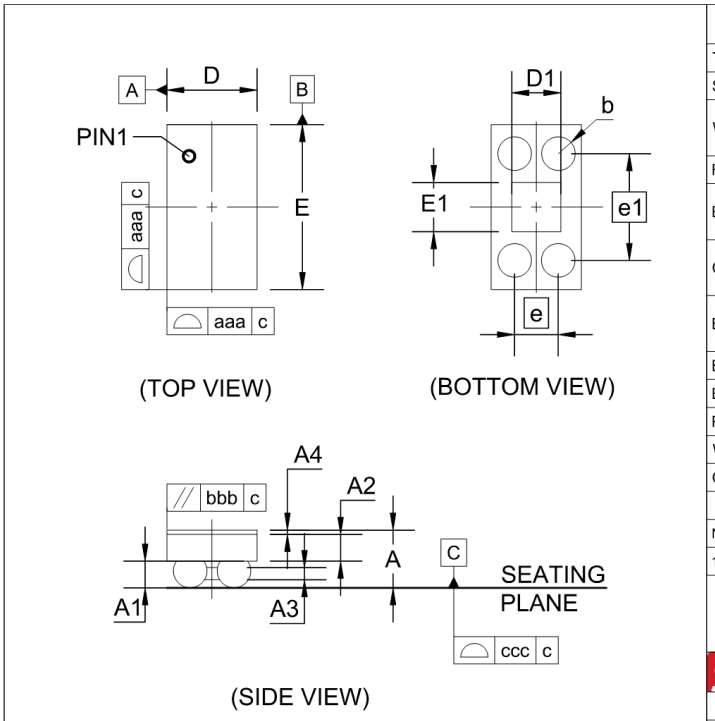
**Notes:**

8. All data is measured at room temperature, unless otherwise stated.

## Dimensions and Patterns

### 1.5 x 0.8 x 0.54 mm

**Package Size – Dimensions (Unit: mm)**



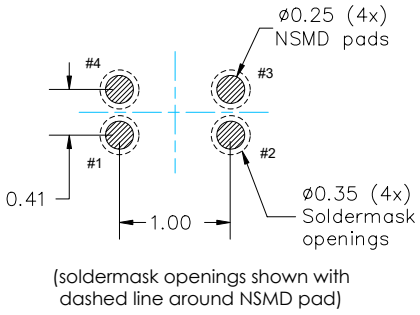

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.481 | 0.540 | 0.599 |
| STAND OFF | | A1 | 0.220 | 0.250 | 0.280 |
| WAFER THICKNESS | | A2 | 0.225 | 0.250 | 0.275 |
| | | A3 | 0.101 | 0.114 | 0.127 |
| FILM THICKNESS | | A4 | 0.036 | 0.040 | 0.044 |
| BODY SIZE | X | D | | 0.845 | |
| | Y | E | | 1.545 | |
| CHILD DIE SIZE | X | D1 | | 0.460 | |
| | Y | E1 | | 0.460 | |
| BALL PITCH | | e | | 0.410 BSC | |
| | | e1 | | 1.000 BSC | |
| BALL SIZE | | | | 0.300 | |
| BALL WIDTH | | b | 0.285 | 0.315 | 0.345 |
| PACKAGE TOLERNCE | | aaa | | 0.030 | |
| WAFER FLATNESS | | bbb | | 0.100 | |
| COPLANARITY | | ccc | | 0.030 | |

NOTE

1. ALL DIMENSION IN MM

| PKG INFO | | DRAWING NO. | |
|---|---|---|---|
| 4L NCSP 0.845x1.545x0.540 mm | | POD-031-NCSP-004-C01508 | |
| | | REV | SHEET |
| DATE | 2020/9/23 | C00 | 01 |

**Recommended Land Pattern (Unit: mm)**

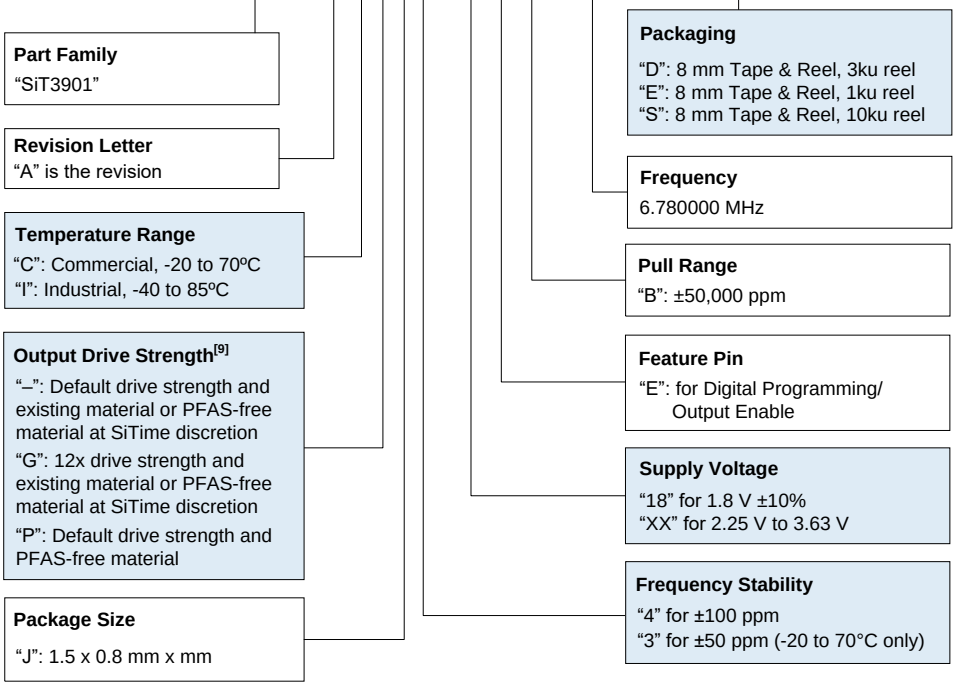



(soldermask openings shown with dashed line around NSMD pad)

**Recommended 4-mil (0.1mm) stencil thickness**

## Ordering Information 6.78 MHz

SiT3901AC-J4-18E B 6.780000 D




**Notes:**

9. Contact SiTime for other drive strength options that result in different rise/fall time for any given output load.

## Ordering Information 2.6 MHz

SiT3901AC-J4-XXE C 2.600000 D

**Part Family**
"SiT3901"

**Revision Letter**
"A" is the revision

**Temperature Range**
"C": Commercial, -20 to 70ºC
"I": Industrial, -40 to 85ºC

**Output Drive Strength**[9]
"–": Default drive strength and existing material or PFAS-free material at SiTime discretion
"P": Default drive strength and PFAS-free material

**Package Size**
"J" 1.5 mm x 0.8 mm CSP

**Packaging**
"D": 8 mm Tape & Reel, 3ku reel
"E": 8 mm Tape & Reel, 1ku reel
"S": 8 mm Tape & Reel, 10ku reel

**Frequency**
2.600000 MHz

**Pull Range**
"C": ±150,000 ppm

**Feature Pin**
"E": for Digital Programming/ Output Enable

**Supply Voltage**
"XX" for 2.25 V to 3.63 V

**Frequency Stability**
"4" for ±100 ppm
"3" for ±50 ppm (-20 to 70°C only)

## Table 8. Revision History

| Version | Release Date | Change Summary |
|---|---|---|
| 0.15 | 20-May-2020 | Preliminary release |
| 0.16 | 20-May-2020 | Title updated<br>Features section updated<br>Table 2 updated |
| 0.18 | 10-Jun-2020 | Updated with programming information<br>Fixed formatting |
| 0.21 | 10-Sep-2020 | Added pull range to ordering information<br>Revised pull frequency equation and examples |
| 0.23 | 22-Sep-2020 | Removed IDD for unrelated output frequencies |
| 0.25 | 8-Dec-2020 | Updated output voltage high |
| 0.27 | 8-Jul-2021 | Added pull range to electrical specifications table, various updates to frequency control registers, and updated frequency stability condition, updated initial tolerance specification |
| 0.29 | 29-Nov-2021 | Added “G” ordering code option for 12x drive strength<br>Resolved formatting errors in the input characteristics section of electrical specifications table |
| 1.01 | 20-May-2022 | Updated current consumption, phase jitter, and period jitter based on characterization data at 6.78 MHz<br>Removed performance plots corresponding to current consumption, phase jitter, and period jitter<br>Updated product description and features section |
| 1.2 | 8-Nov-2024 | Added option for 2.6 MHz. Updated with OE and ST mode. PFAS free ordering code update. |

**SiTime Corporation**, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439