SiT1580

1.2 mm^2 Ultra-small, µPower, Low Jitter, 32.768 kHz TCXO

Features

- 32.768 kHz ±5 ppm all-inclusive frequency stability
- World's smallest TCXO footprint: 1.2 mm^2
  - 1.5 mm x 0.8 mm CSP
- LVCMOS output drives multiple loads
- Low integrated phase jitter (IPJ): 2.5 ns$_{RMS}$
- Ultra-low power: 4.5 µA
- Supply voltage: 1.8 V ±10%
- Operating temperature ranges: -40°C to +85°C
- Pb-free, RoHS and REACH compliant
- Hermetically sealed against gas intrusion to exceed test conditions such as MIL-STD-883G Method 1014.12

Applications

- Smart watches, health and wellness monitors
- Ultra-accurate RTC reference clock
- Smart utility meters, E-meters
- Embedded IoT modules

TempFlat MEMS™ AstroMEMS™

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Electrical Characteristics

Table 1. Electrical Characteristics

Conditions: Min/Max limits are over temperature, Vdd = 1.8 V ±10%, unless otherwise stated. Typicals are at 25°C and Vdd = 1.8 V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Output Frequency	Fout		32.768		kHz	
Total Frequency Stability	F_stab	-5		5	ppm	All inclusive. Includes initial tolerance and stability over temperature, voltage, and load variations
Allan Deviation	AD		1e-8	4e-8	–	1 second averaging time
First Year Frequency Aging	F_aging		±1		ppm	T_A = 25°C, Vdd = 1.8 V
Humidity Sensitivity			±0.1		ppm/%RH	Humidity effect on Frequency stability
Jitter						
Integrated Phase Jitter	IPJ		1.8	2.5	ns$_{RMS}$	Integration bandwidth = 100 Hz to 16.384 kHz. Inclusive of 50 mV peak-to-peak sinusoidal noise on Vdd. Noise frequency 100 Hz to 20 MHz
RMS Period Jitter	PJ$_{RMS}$		2.5	4	ns$_{RMS}$	10,000 samples, per JEDEC standard 65B
Peak-to-Peak Period Jitter	PJ$_{p-p}$		20	30	ns$_{p-p}$	
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.62	1.8	1.98	V	
Supply Current	Idd		4.5	5.3	µA	No Load
Start-up Time at Power-up	t_start			300	ms	Measured when supply reaches 90% of final Vdd to the first output pulse
Operating Temperature Range						
Operating Temperature Range	Vdd	-20		70	°C	"C" ordering code
		-40		85	°C	"I" ordering code
LVCMOS Output						
Output Rise/Fall Time	tr, tf		9	20	ns	10-90% (Vdd), 15 pF Load
Output Clock Duty Cycle	DC	45		55	%	
Output Voltage High	VOH	90%			Vdd	I_{OH} = -1 µA
Output Voltage Low	VOL			10%	Vdd	I_{OL} = 1 µA

Note:

1. Tested with Agilent 53132A frequency counter. Measured with 100 ms gate time for accurate frequency measurement.

Table 2. Pin Configuration

CSP Pin	Symbol	I/O	Functionality
1	NC	Internal Test	Leave pin floating. Do not connect to GND.
2	CLK Out	OUT	Oscillator clock output, LVCMOS compatible. Output driver will sink/source sufficient current to drive multiple loads without signal degradation.
3	Vdd	Power Supply	SiT1580 includes on-chip filtering capacitance. If your power supply cannot deliver fast response for the rise/fall time, we recommend a 10-100 nF bypass capacitor.
4	GND	Power Supply Ground	Connect to ground.

CSP Package (Top View)

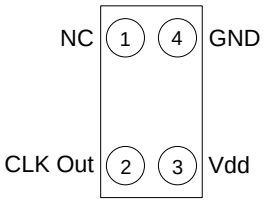


Figure 1. Pin Assignment

Table 3. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameters	Test Conditions	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 4.0	V
Continuous Maximum Operating Temperature Range		105	°C
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Charge-Device Model (CDM) ESD Protection	JESD22-C101	750	V
Machine Model (MM) ESD Protection	JESD22-A115	200	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	20,000	*g*
Mechanical Vibration Resistance	Mil 883, Method 2007	70	*g*
Maximum Junction Temperature		150	°C
Storage Temperature		-65 to 150	°C

System Block Diagram

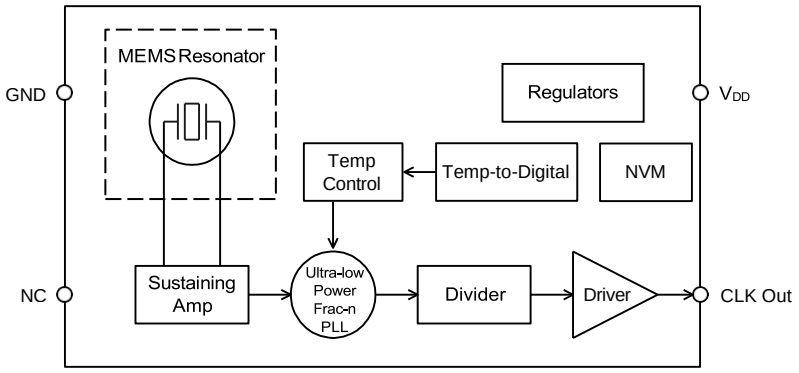


Figure 2. SiT1580 Block Diagram

Description

SiT1580 is an ultra-small, µPower 32.768 kHz TCXO optimized for battery-powered applications. SiTime's silicon MEMS technology enables the first 32 kHz TCXO in the world's smallest footprint and chip-scale packaging (CSP). Typical supply current is 4.5 µA under no load condition.

SiTime's MEMS oscillator consists of a MEMS resonator and a programmable analog circuit. SiT1580 MEMS resonator is built with SiTime's unique MEMS First™ process. A key manufacturing step is EpiSeal™ during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, SiTime's MEMS resonator die can be used like any other semiconductor die. One unique result of SiTime's MEMS First and EpiSeal manufacturing processes is the capability to integrate SiTime's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

TCXO Frequency Stability

SiT1580 is factory calibrated (trimmed) over multiple temperature points to guarantee extremely tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point with a -0.04 ppm/C^2 temperature coefficient, the SiT1580 temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is a 32 kHz TCXO with extremely tight frequency variation over the -40°C to +85°C temperature range.

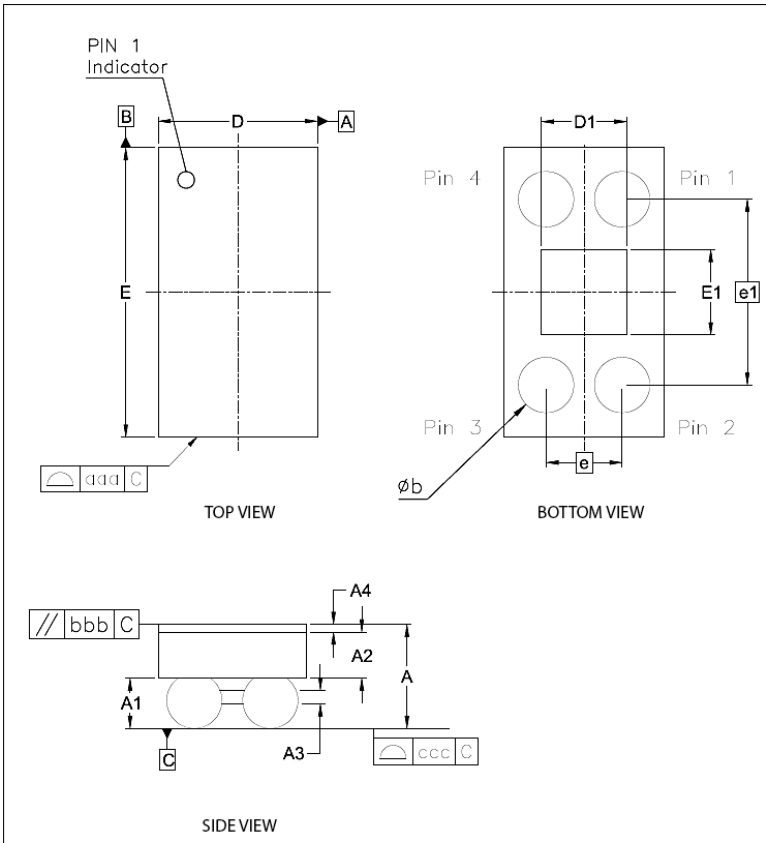
When measuring the output frequency of SiT1580 with a frequency counter, it is important to make sure the counter's gate time is $\geq$100 ms. Shorter gate times may lead to inaccurate measurements.

Post Stress Frequency Stability

The SiT1580 is designed to be robust and maintain frequency accuracy in the presence of the smallest molecular gases that may be encountered either in manufacturing, qualification stress or general usage. In such cases, the SiT1580 is designed to withstand external influences and stay within the ±5 ppm all-inclusive frequency stability.

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)

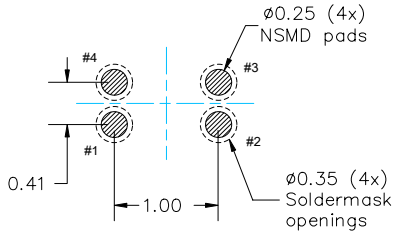


		SYMBOL	MIN	NOM	MAX
PACKAGE THICKNESS		A	0.481	0.540	0.599
STAND OFF		A1	0.220	0.250	0.280
WAFER THICKNESS		A2	0.225	0.250	0.275
		A3	0.101	0.114	0.127
FILM THICKNESS		A4	0.036	0.040	0.044
BODY SIZE	X	D		0.845	
	Y	E		1.545	
CHILD DIE SIZE	X	D1		0.460	
	Y	E1		0.492	
BALL PITCH		e		0.410 BSC	
		e1		1.000 BSC	
BALL SIZE				0.300	
BALL DIAMETER/WIDTH		b	0.285	0.315	0.345
PACKAGE TOLERANCE		aaa		0.030	
WAFER FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.030	

NOTES
1. Dimensioning and tolerance conform to ASME Y14.5-2009
2. All dimensions are in millimeters.

TITLE	4L NCSP	SiTime	
		DWG NO.	
		POD-032-NCSP-004-C01508	
0.845x1.545x0.54 mm		REV.	SHEET
DATE	10-MAR-2019	B03	1 OF 2

Recommended Land Pattern (Unit: mm)



(soldermask openings shown with dashed line around NSMD pad)

Recommended 4-mil (0.1mm) stencil thickness

Manufacturing Guidelines

1) No Ultrasonic or Megasonic cleaning: Do not subject the SiT1580 to an ultrasonic or megasonic cleaning environment. Permanent damage or long term reliability issues may occur.
2) Reflow profile, per JESD22-A113D.
3) The SiT1580 CSP includes a protective, opaque polymer top-coat. If the SiT1580 is exposed to intense light, especially in the 1.0-1.2 µm IR spectrum, we recommend a protective “glob-top” epoxy or other cover to keep the light from negatively impacting the frequency stability.
4) For additional manufacturing guidelines and marking/tape-reel instructions, refer to SiTime Manufacturing Notes.

Ordering Information

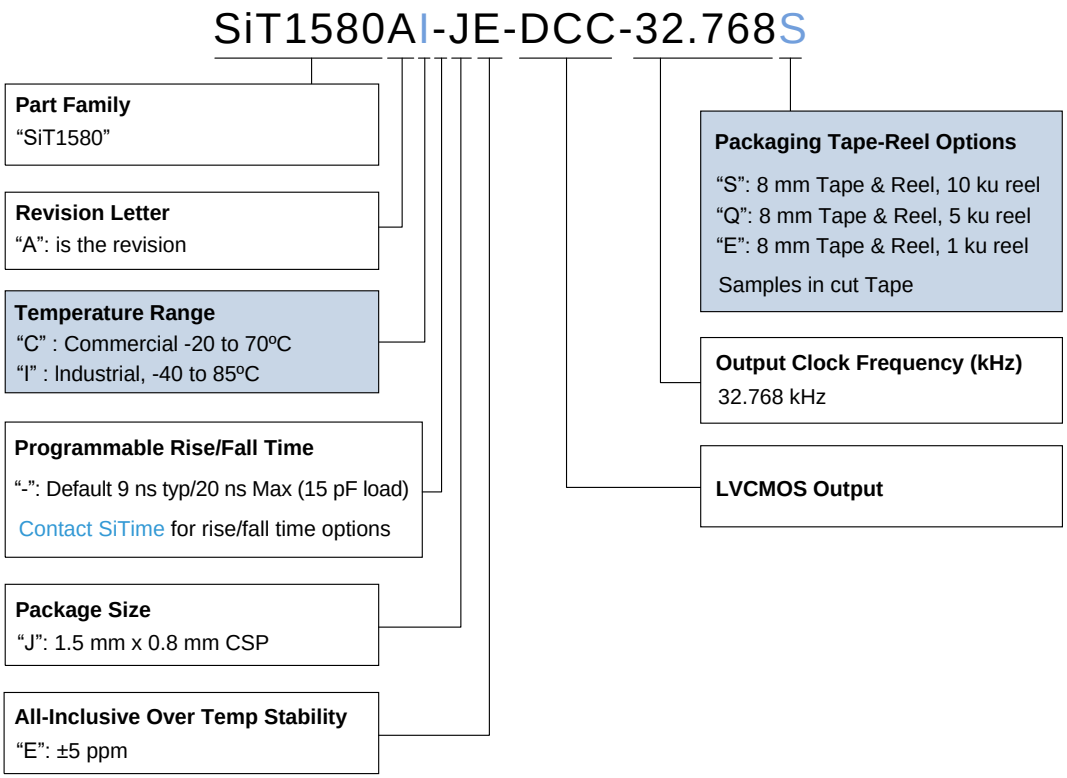


Table 4. Revision History

Version	Release Date	Change Summary
0.92	10/01/2018	Preliminary Datasheet Release
1.0	04/29/2020	Final Release
1.01	5/21/2020	Added Figure 2: System Block Diagram

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