How to Measure Clock Jitter – Part I
Principle and Practice

April 8-9, 2013
Agenda

- Jitter definitions and terminology
- Who cares about jitter
- How to measure clock jitter
What is Clock Jitter

• Jitter is, “The deviation of an event timing relative to its ideal value”
  • Event? - defined by specific type of jitter
  • Ideal value? - event timing on an ideal clock, often estimated from average value of the event

• Jitter definitions:
  • Period Jitter
    • Deviation of the clock period from averaged value
  • Cycle-to-Cycle Jitter
    • Deviation of the difference of periods of two consecutive clock cycles
  • Long Term or Multi-Cycle Jitter
    • Deviation of the durations of multiple cycles from the averaged value
    • Also known as long term jitter or accumulated jitter
  • Timing Interval Error (TIE) Jitter and Phase jitter
    • Error in edge location relative to an ideal clock
Who Cares About Clock Jitter

• Digital applications (Time Domain)
  • Computers
  • Data Servers
  • Network Interface Cards (NICs)
  • Telecom Equipment
  • Embedded Systems
    • Industrial and appliance controllers
• Graphics and Video Displays
• Consumer Electronics
  • Digital cameras, camcorders, game console, smart phones, many more.
• RF & GPS do Not Care About Time Domain
  • They care about phase noise (future topic)
Jitter Definitions and Terminology

Period Jitter (PerJ)

- Period jitter: variation of period from ideal period (typically average period)
  - Event: Two consecutive rising or falling edges
  - Ideal value = average period

\[
PerJit(k) = T_k - T_c \quad \text{PerJit}_{RMS} = STDEV(T_k)
\]
Clocks in High Speed Digital Systems

- CPU
- Parallel Interface
- Serial Transmit
- Serial Receive
- Peripheral
- CPU
- GPU
- Memory etc.
- CLOCK

SiTime
State Machine (Processor) Clocking

- Processors, microcontrollers
- Application Processors (graphics, network, etc)
- State-Machines, DSP

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Application Requirements</th>
<th>MEMS Timing Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range</td>
<td>1 MHz to 600 MHz</td>
<td>1 MHz to 800 MHz</td>
</tr>
<tr>
<td>Frequency Stability</td>
<td>25 ppm to 50 ppm</td>
<td>5 ppm to 50 ppm</td>
</tr>
<tr>
<td>Period Jitter</td>
<td>4 ps to 100 ps (RMS)</td>
<td>1 ps to 5 ps</td>
</tr>
<tr>
<td>Cycle-to-cycle (C2C) Jitter</td>
<td>20 ps to 500 ps</td>
<td>8 ps to 50 ps</td>
</tr>
<tr>
<td>IDD</td>
<td>10 mA to 200 mA</td>
<td>3 mA to 70 mA</td>
</tr>
<tr>
<td>Start-up time</td>
<td>5 ms to 50 ms</td>
<td>3 ms to 10 ms</td>
</tr>
<tr>
<td>Spread Spectrum clocking (for EMI reduction)</td>
<td>Down-spread, Center-spread 0.5%, 1%, 2%, 4%</td>
<td>All option readily available</td>
</tr>
</tbody>
</table>
Jitter Measurement

• Jitter can be measured with the following equipment
  • **Real-time oscilloscope**
    • Equivalent-time oscilloscope
    • Time interval analyzer (TIA)
    • Bit error rate tester
    • Specialized, under-sampling instrument (often used in automatic test equipment)
    • Phase noise analyzer (for phase noise and integrated phase jitter)

• Real-time oscilloscope are most commonly used
Jitter Measurement with Real-Time Sampling Oscilloscope

- Uses interpolation to estimate the threshold crossing time of the edges
Real-Time Scope Measurement Errors

1. **Voltage Noise Converted to Jitter ($J_{VJC}$):**
   - Oscilloscope front-end amplifier
   - Quantization error due to 8-bit to 10-bit ADC resolution

2. **Timing Error ($J_{TBJ}$):**
   - Noise due to low sampling rate
   - Time base jitter
   - Trigger error: Can be ignored for scope with deep memory supporting single capture measurements
Voltage Noise to Jitter Conversion

- Minimize voltage noise to jitter conversion
  - Sharpen the edges $\rightarrow$ Increase SlewRate
  - Reduce scope noise $\rightarrow$ Decrease $V_n$

$T_n = V_n / \text{SlewRate}$

Faster rise/fall time reduces voltage noise impact on jitter
Reduce Voltage Noise to Jitter Conversion (Decrease Scope Noise)

- Select the right front-end bandwidth
  - Amplifier noise is proportional to its bandwidth
  - Optimal bandwidth to reduce the scope amplifier noise while avoiding slowing down the signal edge
  - Example: $T_{\text{rise}} = 1\text{ns} \rightarrow Amp_{\text{BW}} \sim 1\text{GHz}$

$$Amp_{\text{BW}} \approx \frac{1}{\min(t_{\text{rise}20/80}, t_{\text{fall}20/80})}$$  \hspace{1cm} \text{Amp}_{\text{noise}} \propto \sqrt{Amp_{\text{BW}}}

By reducing acquisition bandwidth from 8GHz to 2GHz, measured period jitter changed from 3.58 to 1.72 ps rms.
Reduce Voltage Noise to Jitter Conversion
(Increase Sampling rate)

- Select maximum sampling rate
  - The higher the sampling rate, the more accurate edge interpolation
  - Minimum sampling rate required 10 times higher than the inverse of rise/fall time

\[
\text{Sampling rate}_{\text{min}} \approx \frac{5}{\min(t_{\text{rise} \_20/80}, t_{\text{fall} \_20/80})}
\]

By increasing sampling rate from 5Gsps to 40Gsps, measured period jitter changed from 2.1 to 0.92 ps rms.
Reduce Voltage Noise to Jitter Conversion (Increase Signal Slew Rate)

- Choose smaller vertical setting (volt/div)
  - Smaller setting may cause the signal to go outside the screen. This is OK on most scopes
  - Vertical zoom reduces the scope quantization noise
  - 50mV/div is sufficient for most LVCMOS clocks

By reducing the vertical setting from 500mV/Div. to 50mV/Div., measured period jitter changed from 3.58 to 0.91 ps rms.
Oscilloscope Time Base Jitter

- **Time-base jitter**
  - The oscilloscope time-base jitter directly impacts the jitter measurement.
  - Ensure the scope time-base jitter is less than **0.5ps RMS** for accurate jitter measurements in the range of 1ps or higher.

![Jitter Measurement Error Due To Time Base Jitter](chart)

**Measurement Error (% of J_{SUT})**

- **J_{TBJ} [1 ps rms]**
- **J_{TBJ} [0.5 ps rms]**
- **J_{TBJ} [0.25 ps rms]**

**Jitter of Signal Under Test, J_{SUT} (ps rms)**

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Consistent Period Jitter Measurements Across Different Instruments

Other Jitter Error Sources:

- **Test Probe:**
  - Do not use active probes for jitter measurement. The probe amplifier adds to the instrument jitter floor significantly.

- **Test Fixture:**
  - Use good lab power supplies to reduce *POWER SUPPLY NOISE*
  - Use recommend *POWER SUPPLY BYPASS* for SiTime devices
  - Solder down the DUT to eliminate *PARASITIC INDUCTANCE OR CAPACITANCE* from socket
  - Proper *TERMINATION* for oscillator output
    - Probe Termination App Note to be released by April 12.
Recommended Period Jitter Measurement Setup

Setup 1:
Connection to scope through comparator. Maintains 15pF loading to the oscillator.

SiTime jitter characterization setup

Setup 2:
Direct connection to oscilloscope. Causes 50Ω loading to the oscillator output.
Summary

• Jitter is the result of edge uncertainty in clock signals

• Using default oscilloscope auto-setups is not optimal for accurate and consistent jitter measurement

• Tips for measuring period jitter with real-time digital oscilloscope:
  • Use oscilloscope with low time base jitter (less than 0.5ps RMS)
  • Use high sampling rate (at least 20 Gsps)
  • Choose proper vertical settings (maximize slew rate)
  • Select the scope bandwidth optimally (minimize scope noise contribution)
Contact Information

• For Questions, contact SiTime Technical Support
  Technicalsupport@sitime.com

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