

SiT6098EBB Evaluation Board User Manual
for 1-Hz to 2.5-MHz Oscillators and TCXOs in 1508 CSP:
SiT1532/34, SiT1552, SiT1566/68/69, SiT1572/76/79

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The SiT6098EBB evaluation board supports 1-Hz to 2.5-MHz oscillators in a 1.5 x 0.8 mm CSP package including the following products:

Base Part Number	Type	Output Frequency	Package
SiT1532	μPower Oscillator	32.768 kHz	1.5 x 0.8 CSP
SiT1572	Low-Jitter Oscillator	32.768 kHz	1.5 x 0.8 CSP
SiT1552	±5 to ±20-ppm TCXO	32.768 kHz	1.5 x 0.8 CSP
SiT1566	±3 to ±5-ppm TCXO	32.768 kHz	1.5 x 0.8 CSP
SiT1568	±5-ppm TCXO with calibration	32.768 kHz	1.5 x 0.8 CSP
SiT1534	μPower Oscillator	1 Hz to 32.768 kHz	1.5 x 0.8 CSP*
SiT1569	Low-Power Oscillator	1 Hz to 462.5 kHz	1.5 x 0.8 CSP
SiT1576	Low-Jitter TCXO	1 Hz to 2.5 MHz	1.5 x 0.8 CSP
SiT1579	Low-Jitter Oscillator	1 Hz to 2.5 MHz	1.5 x 0.8 CSP

*SiT1534 is also available in a 2.0 x 1.2 package. See SiT6096EBB for 2012 support.

1 Introduction

The SiT6098EBB evaluation board (EVB) provides the ability to evaluate the functionality of SiTime’s 32-kHz 1508 oscillators and TCXOs on a simple board that makes it easy to power up the oscillator and observe the output buffered through an operational amplifier. The analog buffer isolates the device from the significant loading, which is important for performing the best waveform and current measurements.

2 Board Information

A PCB view of the SiT6098EBB board with component reference designator call-outs is shown in [Figure A2 \(SiT6098EBB layout\)](#).

3 Connectors

Table 1. Connector’s Overview: Digi-Key p/n

Designator	Purpose	Digi-Key P/N for Mating Connector
J2	DUT power	WM2613-ND
J3	Buffer power	WM2626-ND
J4	DUT consumption current measurement	WM2613-ND
Crimps for J2, J3, J4		WM6685CT-ND, 7pcs
J6	Direct output	H2011-ND
Crimps for J6		H9999-ND, 2pcs
J1	Buffer output	A97594-ND

Note: Pin-1 orientation of the chip is defined by a chamfer and dot in the silkscreen pattern.

3.1 DUT Power

Evaluation boards have input two-pin connector J2 for power supply. Pins polarities are identified on the silkscreen pattern near connector.

3.2 Buffered Clock Output

This EVB uses an operational amplifier to buffer the oscillator clock output to make it easy to connect to test and measurement equipment through SMA cables without loading the ultra-low power clock output driver. The ADA4817-1 FET operational amplifier is used in a unity-gain buffer configuration. It is a unity-gain stable, ultra-high speed, voltage feedback amplifier with FET inputs.

The three-pin connector J3 is intended for supplying the VDD power to the on-board operational amplifier. Pin polarities are identified on the silkscreen pattern near connector J3. The operational amplifier requires a dual power supply and should be -3V for negative power rail (V-) and +8V for the positive supply (V+).

Table 2. Buffer supply voltage:

Power Rail Name	Voltage
V+	+8V (max)
V-	-3V (min)

3.3 Clock Output (Direct)

The oscillator output is best observed through the buffered output path using a test probe placed on the test point TP2 or through the SMA connector J1. The buffer can be bypassed and the output can be directly observed thru J6 2mm pitch pin header connector or using test point TP1 (see [Figure A1 – Figure A2](#) of Appendix A for test points arrangement on the board).

[Section 4.1](#) shows recommended measurement configurations. When probing the oscillator output directly, the probe loading can affect the output waveform and power consumption of the device. SiTime recommends active probes with 10-M Ω and 1-pF impedance.

3.4 DUT Current Consumption Measurement

Two-pin connector J4 enables measuring the current consumption. To measure the current properly, remove zero-ohm resistor R3, and connect the DMM or other current measuring device across this connector.

4 Application Notes

4.1 Configurations

The SiT6098EBB board supports multiple configurations for evaluating AC and DC coupled output modes of the SiTime oscillator. In addition, this EVB provides the ability to add additional load capacitance and to bypass the output buffer. [Figure A1](#) in Appendix A shows the schematic of SiT6098EBB. Components labeled “DNP” are not assembled. Components which are common to all listed below configurations have nominal values assigned to them.

4.2 General Configuration

[Figure 1](#) shows general shipment configuration.

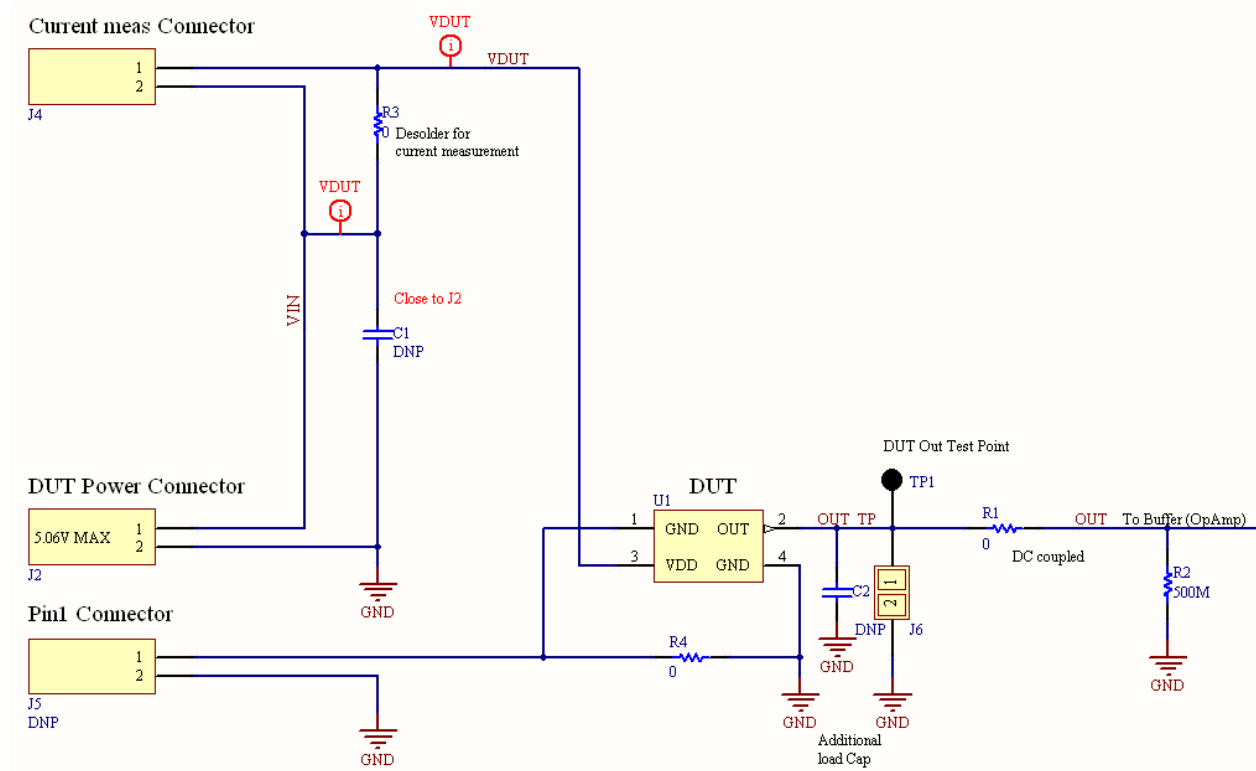


Figure 1. General EVB configuration

4.2.1 Configuration 1: DC-Coupled Output

This configuration is intended for observing a DC coupled output through an oscilloscope through the buffered output at SMA (J1) connector or test point (TP2) (see [Figure A1](#) – [Figure A2](#) of Appendix A for test point locations on the board). [Figure 2](#) shows the circuit for this configuration.

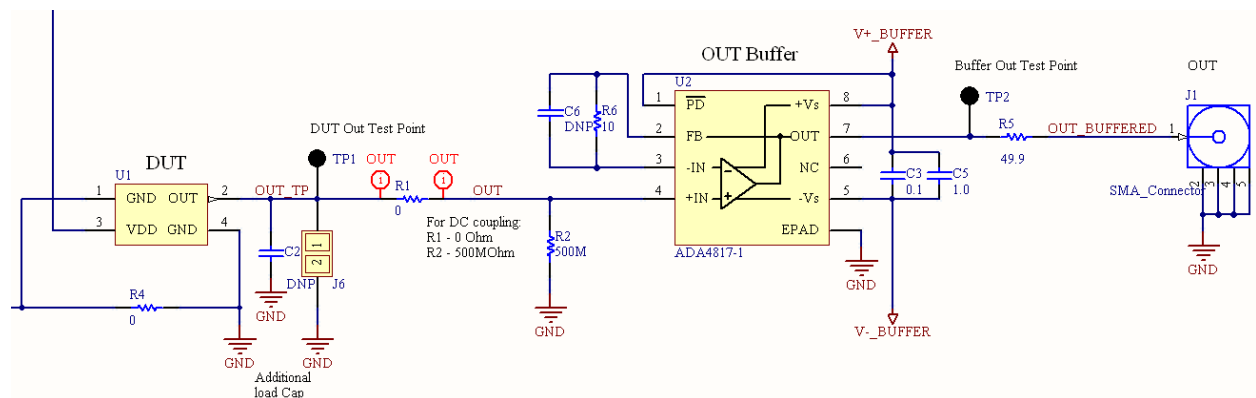


Figure 2. DC-coupled output configuration

4.2.2 Configuration 2: AC-Coupled Output

This configuration is intended for observing an AC-coupled output through an oscilloscope through the buffered output at SMA (J1) connector or buffer output test point (TP2) (see [Figure A1 – Figure A2](#) of Appendix A for test point locations on the board). A 0.1- μF capacitor is placed in the clock output signal path. [Figure 3](#) shows the circuit for this configuration.

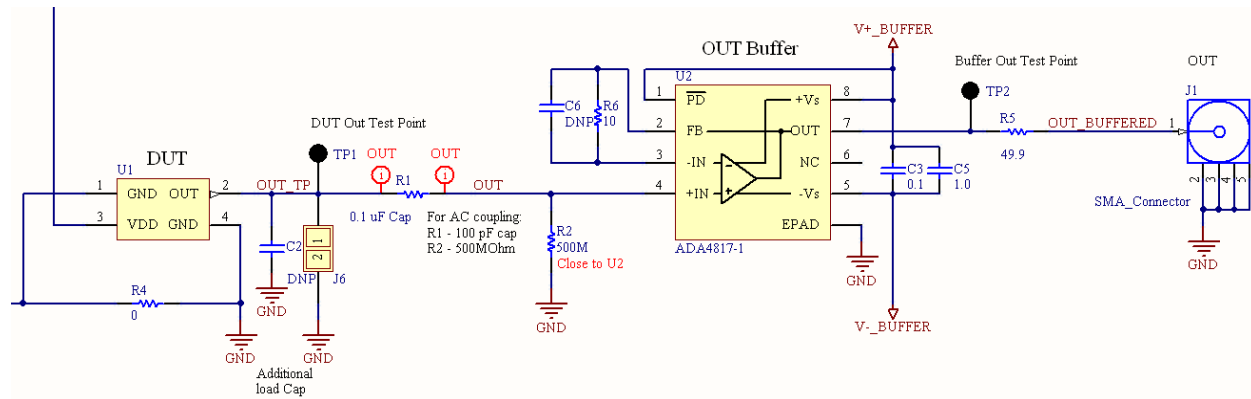


Figure 3. AC-coupled output configuration

4.2.3 Configuration 4: Direct Output with Additional Load Capacitor

This configuration is intended for observing direct oscillator output with a passive high input impedance ($> 1 \text{ M}\Omega$ || $< 1 \text{ pf}$) scope probe at test point TP1 (see [Figure A1 – Figure A2](#) of Appendix A for test points on the board) or to connect the oscillator output to the end user system using 2-mm pitch header connector J6 with an optional user defined load capacitor C2. [Figure 4](#) shows the circuit for this configuration.

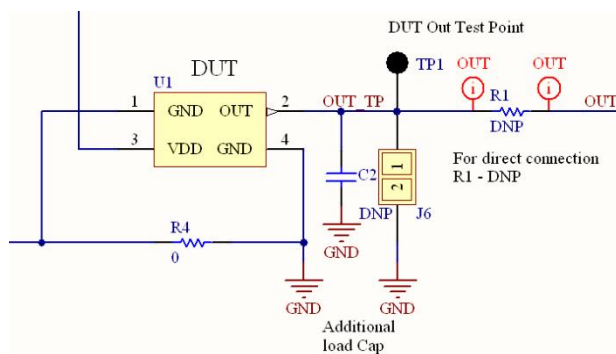


Figure 4. Circuit for observing direct oscillator output

4.2.4 Configuration 5: DUT Power Supply Filter

This configuration is intended for providing power-supply filtering for the oscillator by soldering user-defined capacitor C1. Figure 5 shows the circuit for this configuration. Power-supply filtering for the device under test (DUT) is not required in common use cases. It should be used only if power supply noise is significant or to cancel parasitic inductance effect of long wires from the power supply to EVB.

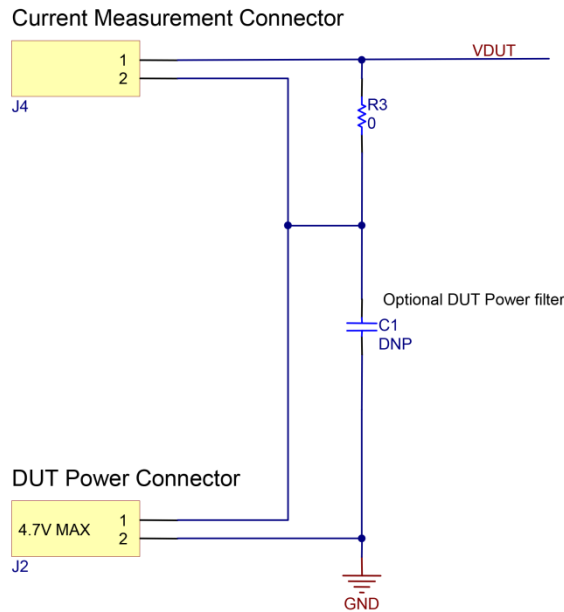


Figure 5. Circuit for providing DUT power filter

4.2.5 Measuring Current Consumption

When measuring supply current, simply remove jumper resistor R3 across 2-pin connector J4. Figure 6 shows the circuit for this configuration and connection of a precision DMM, e.g. Agilent U1242A to connector J4. Figure 7 shows the setup for measuring supply current.

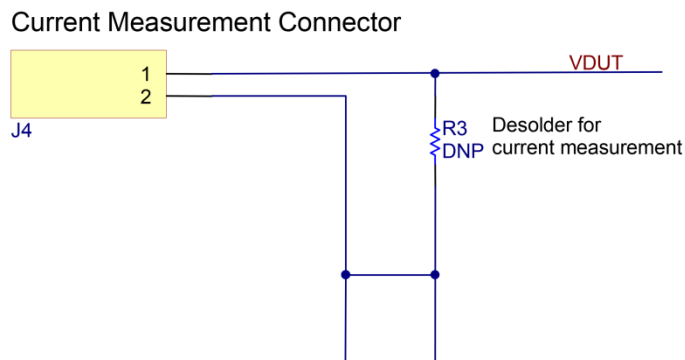


Figure 6. DUT supply current measurement

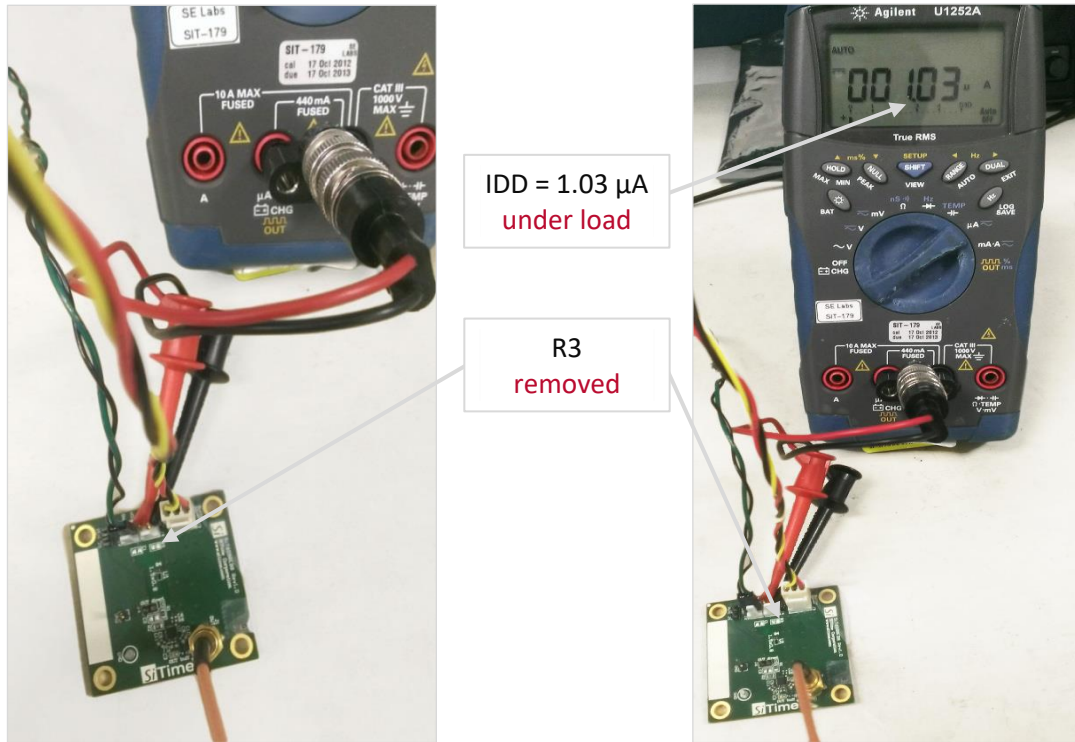


Figure 7. Setup for measuring IDD

Appendix A

A1: Board Schematic

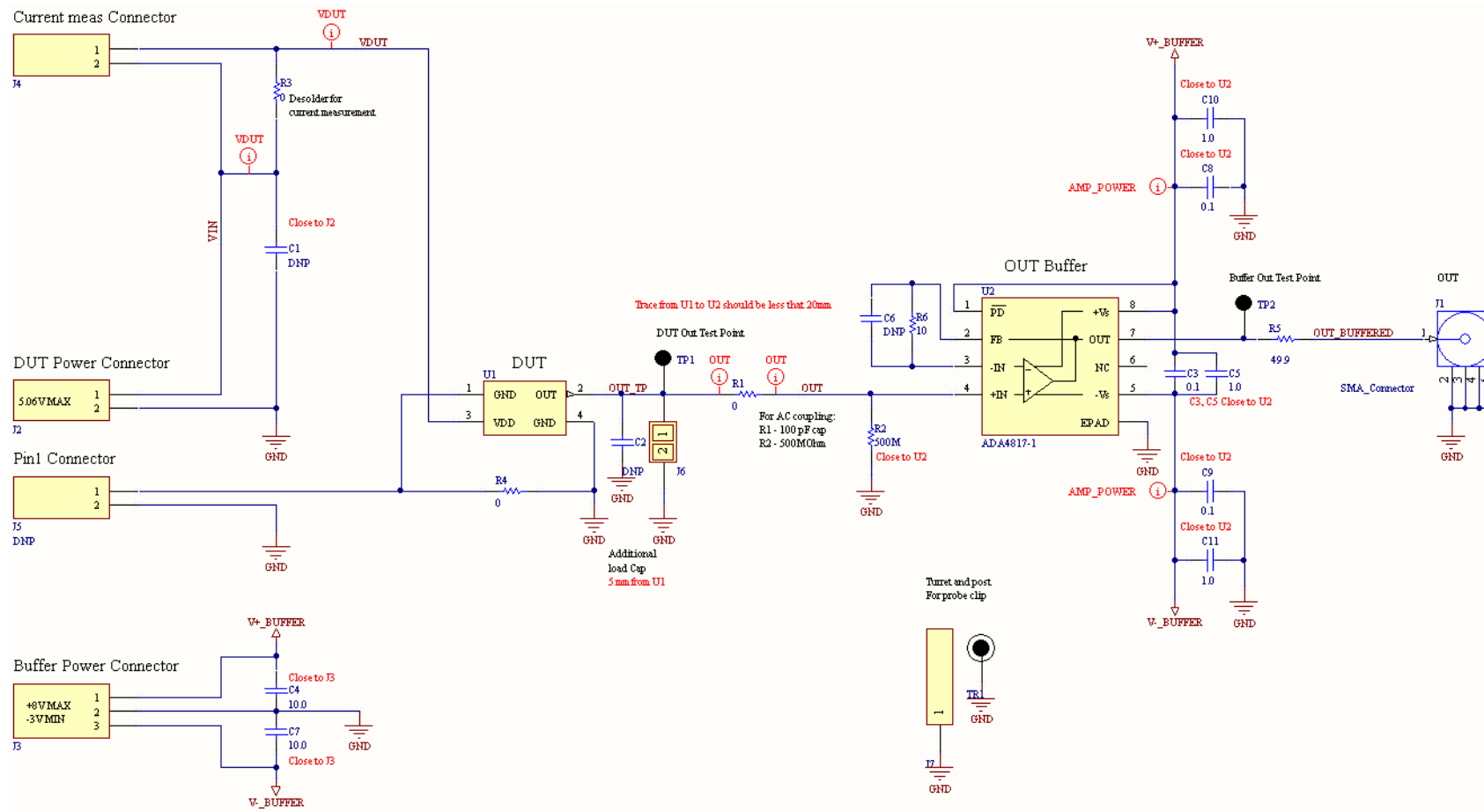


Figure A1. SiT6098EBB schematic

A2: Board Layout

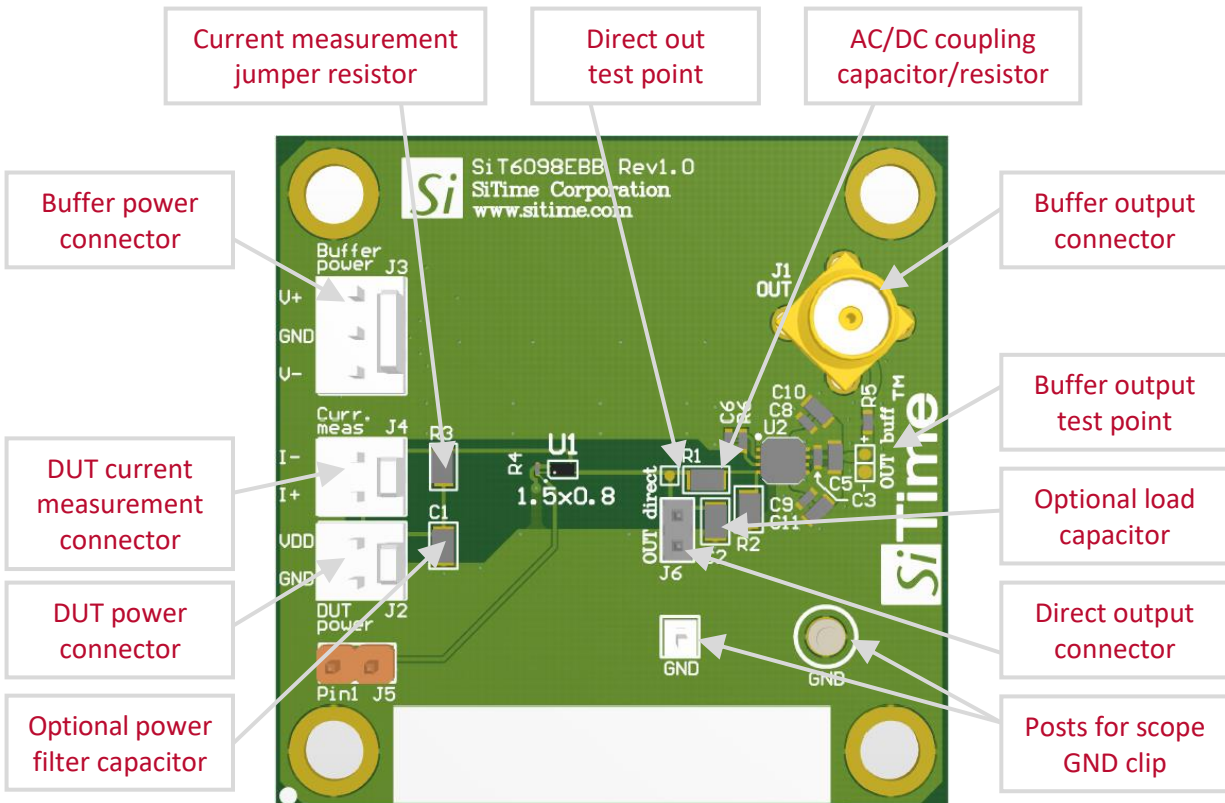


Figure A2. SiT6098EBB layout

Table 3. Revision History

Version	Release Date	Change Summary
1.2	09/11/2019	Addition of SiT1566/68/69, SiT1572/76/79. Edits for clarity.

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