Performance report for SiT9386 - 74.25 MHz, LVDS

Conditions:

- Frequency 74.25 MHz
- VDD: 2.5 V, 3.3 V
- Room temperature
- Termination:
  - 100 Ω between both outputs.

Equipment:

Model	Measurement / Purpose
Keysight DSA90604A (6 GHz, 20 Gsps)	Period jitter, differential voltage swing, rise/fall time, duty cycle
Keysight 5052B Signal Source Analyzer	Phase noise, integrated phase jitter
Keysight 34980A	Power supply current
Keysight E3631A	Power supply
Keysight 53230A	Frequency

Test setup:

For waveform parameters measurement (rise/fall time, differential swing, duty cycle), both DUT outputs are terminated with 100 Ω differential. Output signals are measured using Keysight 1134B active probe with Keysight N5425B probe head. All measurements are applied to the differential waveform. Figure 1 shows test setup diagram for waveform parameters measurement.

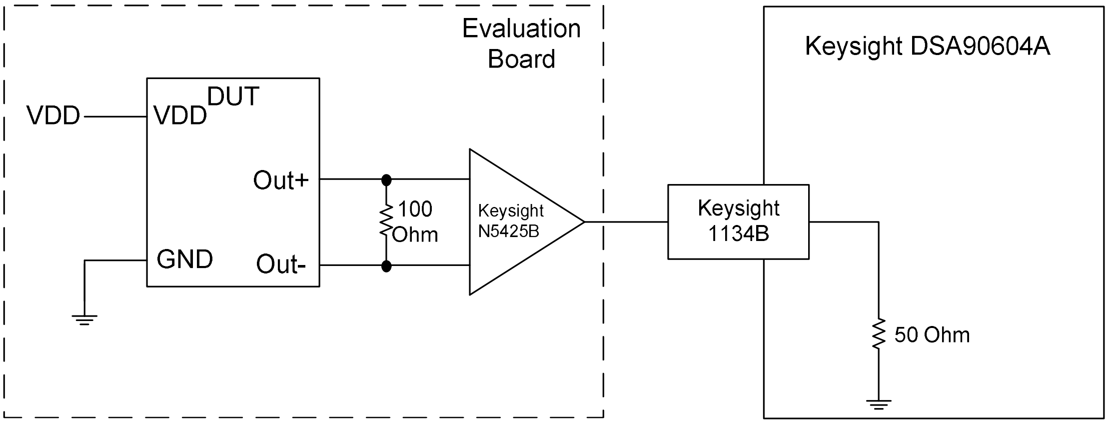

Figure 1: Test setup for measuring waveform parameters (rise/fall time, differential swing, duty cycle)

For period jitter measurement outputs are connected through AC-coupling capacitors to the oscilloscope channels. Signals are subtracted inside the oscilloscope. All measurements applied to differential waveform. Figure 2 shows test setup diagram for period jitter measurement.

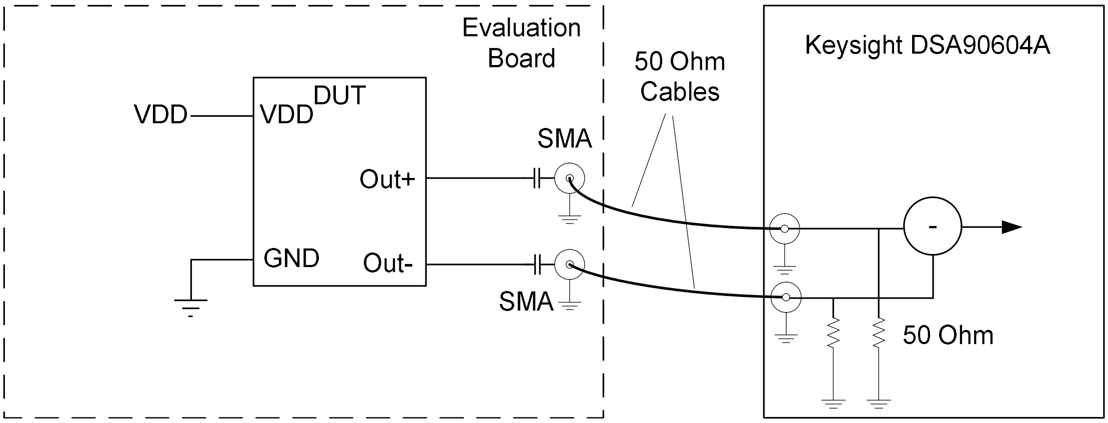

Figure 2: Test setup for measuring period jitter

For phase noise measurements, differential signal is converted to single-ended using impedance matching transformer. Transformer's output is connected to measurement instrument. Figure 3 shows test setup diagram for phase noise measurement.

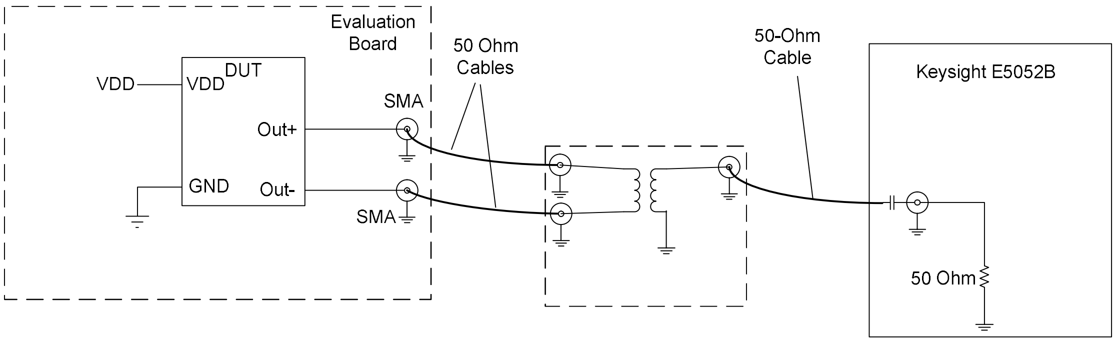

Figure 3: Test setup for measuring phase noise.

For IDD measurement device output is floating. For frequency measurement differential-to-single-ended converter is used.

Data:

- Phase noise
- Integrated phase jitter
- RMS period jitter
- Peak-to-peak period jitter
- Rise/fall time
- Duty cycle
- Differential output swing
- IDD
- Frequency stability over temperature

Table 1: Summary performance data

Parameter	Units	Voltage	
		2.5 V	3.3 V
Integrated Phase jitter (1.875 MHz - 20 MHz)	fs, rms	207	210
Integrated Phase jitter (12 kHz - 20 MHz)	fs, rms	283	285
Period jitter	ps, rms	0.85	0.81
Period jitter (10,000 cycles)	ps, pk-pk	6.44	6.34
Duty cycle	%	49.9	49.9
Rise time (20% - 80%)	ps	331	328
Fall time (80% - 20%)	ps	326	325
Differential voltage swing	V	0.67	0.68
Current consumption (no load, output enabled)	mA	67.1	67.6
Current consumption (no load, output disabled)	mA	51.3	51.8

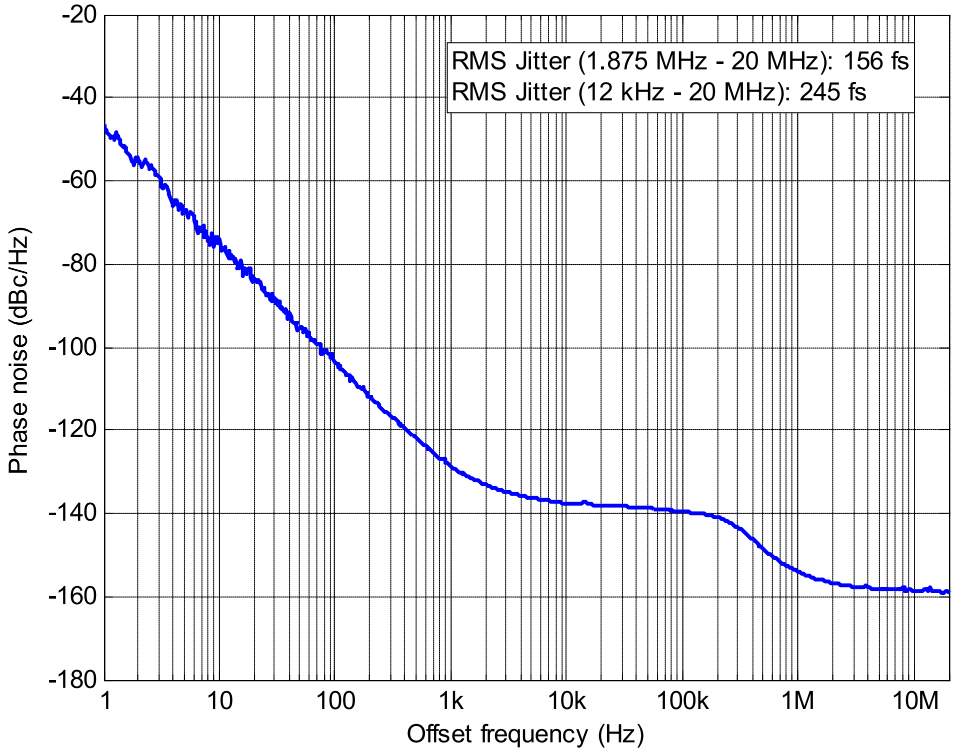

Figure 4: Phase noise, 2.5 V

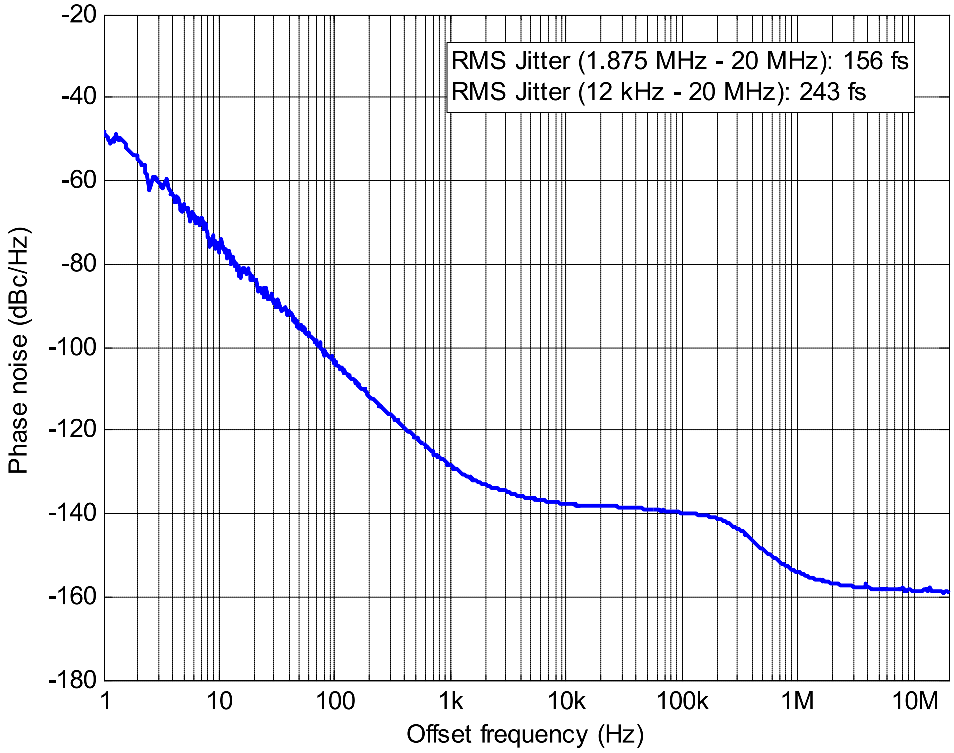

Figure 5: Phase noise, 3.3 V

Figure 6: Output waveform, 2.5 V

Figure 7: Output waveform, 3.3 V

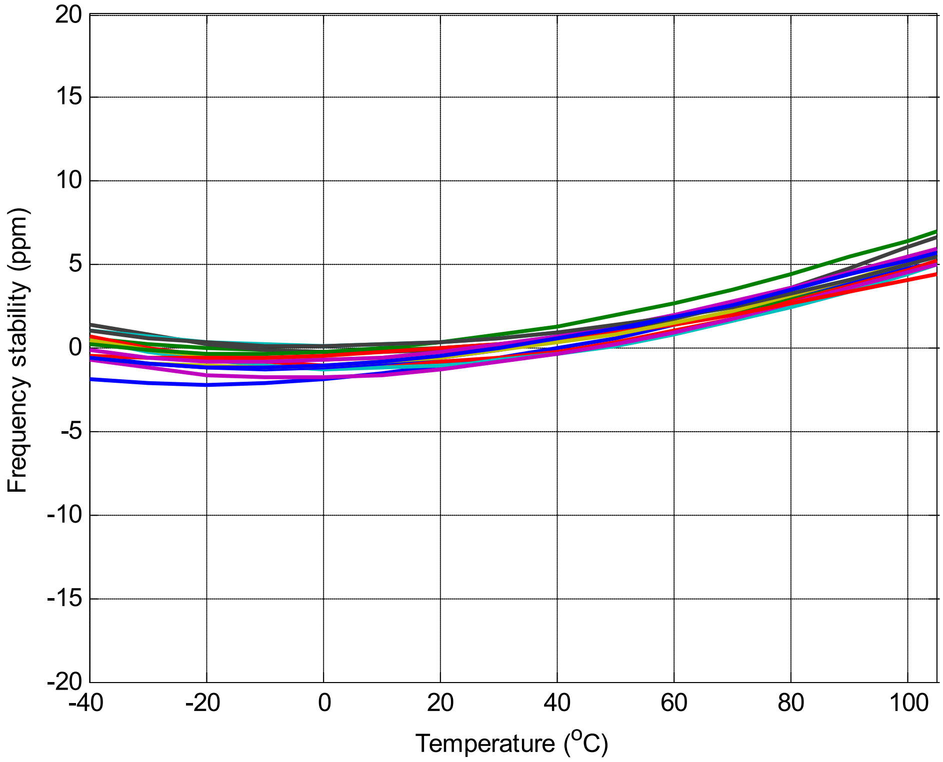

Figure 8: Frequency stability* over temperature, 2.5 V

*SiT9386 frequency stability is independent of output frequency.

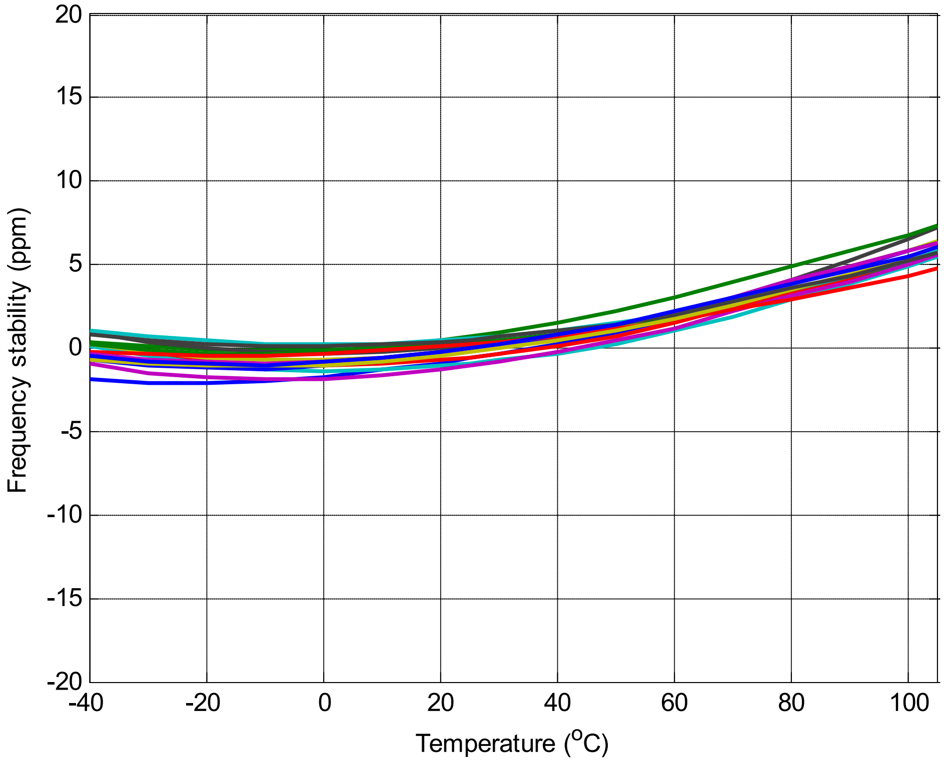

Figure 9: Frequency stability over temperature, 3.3 V