# Improved System Performance with Digital Frequency Tuning in Precision Super-TCXOs

## Contents



## 1 Introduction

Historically, frequency tuning has been achieved through pulling the frequency using a voltage input. This type of frequency control device is called a VCXO (voltage controlled oscillator). A large number of TCXO (temperature compensated oscillator) applications use a voltage control function for frequency tuning during operation. These devices are often called VCTCXOs or TCVCXOs. An alternative method for tuning frequency is by use of a digital input.

Several SiTime Elite Platform™ Super-TCXO™ families, listed in Table 1, offer both voltage control and digital control for frequency tuning. This application note provides information on the DCO mode (digitally controlled oscillator mode) of these precision Super-TCXO families which support digital input through an $I^2C$ digital interface. Using the DCO mode, the output frequency can be continuously pulled within the specified pull range. The pull range can be changed in-system to one of 16 available pull range options, from ±6.25 to ±3200. Additionally, DCO mode allows users to control the output enable (OE) state of the device through the writes to the device's registers (corresponding part number option has to be selected).

**Table 1: SiTime Super-TCXO devices with digital control**

| Family | Frequency Range (MHz) | Freq. Stability (ppm) | Output Signal Type(s) |
|---|---|---|---|
| SiT5155 | 10 std. frequencies | ±0.5, ±1.0, ±2.5 | LVCMOS, clipped sinewave |
| SiT5156 | 1 to 60 | ±0.5, ±1.0, ±2.5 | |
| SiT5157 | 60.000001 to 220 | ±0.5, ±1.0, ±2.5 | LVCMOS |
| SiT5356 | 1 to 60 | ±0.1, ±0.2, ±0.25 | LVCMOS, clipped sinewave |
| SiT5357 | 60.000001 to 220 | ±0.1, ±0.2, ±0.25 | LVCMOS |
| SiT5358 | 1 to 60 | ±0.05 | LVCMOS, clipped sinewave |
| SiT5359 | 60.000001 to 220 | ±0.05 | LVCMOS |
| SiT5186* | 1 to 60 | ±0.5, ±1.0, ±2.5 | LVCMOS, clipped sinewave |
| SiT5187* | 60.000001 to 220 | ±0.5, ±1.0, ±2.5 | LVCMOS |
| SiT5386* | 1 to 60 | ±0.1, ±0.2, ±0.25 | LVCMOS, clipped sinewave |
| SiT5387* | 60.000001 to 220 | ±0.1, ±0.2, ±0.25 | LVCMOS |

* AEC-Q100 Compliant

DCO mode offers multiple advantages compared to voltage control including reduced BOM cost by eliminating the DAC (digital-to-analog converter) and shrinking the PCB area (if an external DAC is used), simplified design, greater flexibility, increased noise immunity, and improved system performance.

1. **Frequency control resolution as low as 5E-12** – This high resolution minimizes accumulated time error in synchronization applications.
2. **Lower system cost** – Traditional VCXOs require a DAC to drive the control voltage input. In a DCO, the frequency control is achieved digitally by writing to the control registers using a serial interface, eliminating the need for a DAC.
3. **Better noise immunity** – The analog signal that is used to drive the voltage pin of a VCXO can be sensitive to noise and the trace over which the signal is routed can be susceptible to noise coupling from the system. Because frequency control for the DCOs is performed over a digital interface, they do not suffer from analog noise coupling.
4. **No frequency pull non-linearity** – The frequency pulling is achieved via a fractional feedback divider of the PLL, eliminating any pull non-linearity that is sometimes associated with quartz-based VCXOs. Better pull range linearity improves the dynamic performance in closed loop operations.
5. **Programmable wide pull range** – Because the pulling mechanism is achieved via a fractional feedback divider, it is not constrained by resonator pullability as it is in quartz-based solutions. SiTime digitally controlled oscillators have 16 frequency pull range options from ±6.25 ppm to ±3200 ppm, offering system designers greater flexibility.

## 2 Theory of Operation

Figure 1 shows a high-level block diagram of the DCO.

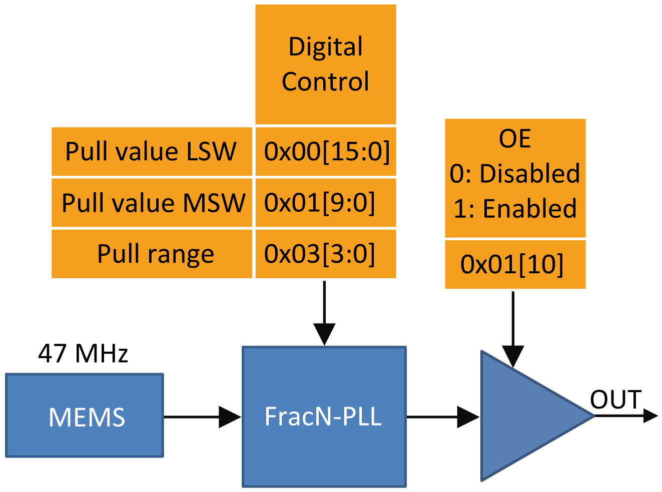


**Figure 1: Digitally Controlled Oscillator High-Level Block Diagram**

### 2.1 Digital Control

The device powers up at the nominal operating frequency and pull range specified by the ordering code. After power-up, both the pull range and output frequency can be controlled via digital interface writes to the respective control registers. The maximum output frequency change is constrained by the pull range limits. Pull ranges are specified in the form of half of the peak-to-peak deviation (e.g. ±100 ppm which is 200 ppm peak-to-peak).

The pull range is specified by the value loaded to the digital pull range control register (Reg2[3:0]). The 16 pull range choices are documented in the control register and range from ±6.25 ppm to ±3200 ppm. Table below shows the frequency resolution vs. pull range programmed value along with the corresponding programming codes.

**Table 2: Frequency Resolution vs. Pull Range**

| Reg2[3:0] | Programmed Pull Range | Frequency Resolution |
|---|---|---|
| 0000b | ±6.25 ppm | 5x10-12 |
| 0001b | ±10 ppm | 5x10-12 |
| 0010b | ±12.5 ppm | 5x10-12 |
| 0011b | ±25 ppm | 5x10-12 |
| 0100b | ±50 ppm | 5x10-12 |
| 0101b | ±80 ppm | 5x10-12 |
| 0110b | ±100 ppm | 5x10-12 |
| 0111b | ±125 ppm | 5x10-12 |
| 1000b | ±150 ppm | 5x10-12 |
| 1001b | ±200 ppm | 5x10-12 |
| 1010b | ±400 ppm | 1x10-11 |
| 1011b | ±600 ppm | 1.4x10-11 |
| 1100b | ±800 ppm | 2.1x10-11 |
| 1101b | ±1200 ppm | 3.2x10-11 |
| 1110b | ±1600 ppm | 4.7x10-11 |
| 1111b | ±3200 ppm | 9.4x10-11 |

The frequency offset (in ppm) is specified by the 26-bit DCO frequency control register in two's complement format. The power-up default value is 00000000000000000000000000b which sets the output frequency at its nominal value (0 ppm). To change the output frequency, a frequency control word is written to Reg0[15:0] (least significant word, LSW) and Reg1[9:0] (most significant word, MSW). The LSW value should be written first followed by the MSW value; the frequency change is initiated after the MSW value is written.

After the MSW pull value is written, control logic changes the feedback divider value during Tdelay timeframe to accommodate the new frequency. Then the output frequency starts to change and settles to 1% of the final frequency value within the Tsettle timeframe (see Figure 2).

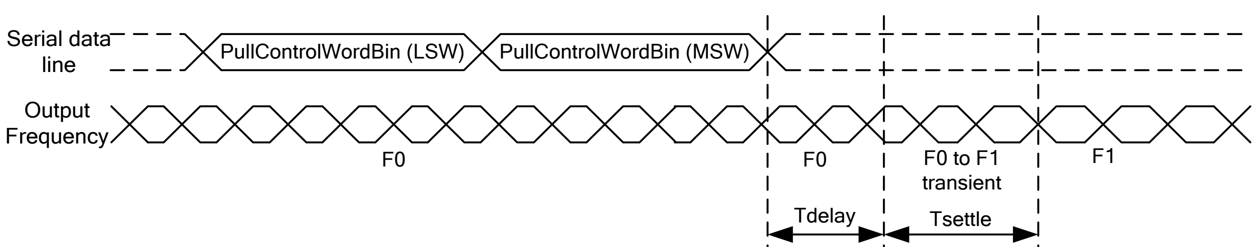


**Figure 2: Frequency Pulling Timing Diagram**

The device output is not disabled during frequency change. Therefore if the software output enable (OE) control function is enabled, the user can disable output manually for frequency change period.

**Important note:** Maximum digital control update rate is 38 kHz regardless of digital interface bus speed.

### 2.2 Additional Functions

Output is enabled/disabled within the Tenable/Tdisable time after the control word containing OE bit is written to the device.

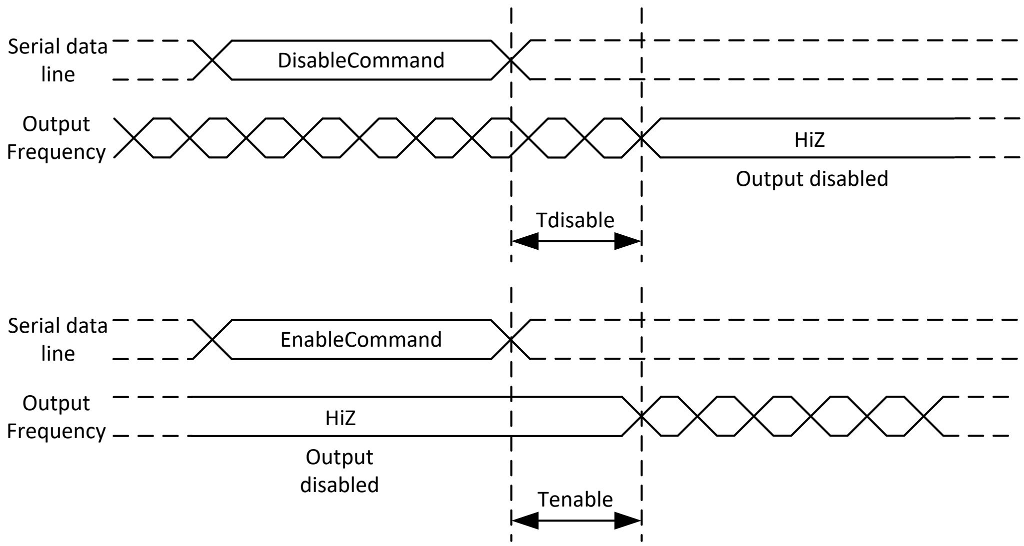


**Figure 3: Output Enable/Disable Timing Diagram**

## 3 Frequency Pulling

Following is the procedure for frequency pulling of SiTime digitally controlled oscillators:

1. Calculate the fraction of the target pull value (*targetPull*) relative to the pull range (*pullRange*):

$$fractionPull = \frac{targetPull}{pullRange} \quad \text{Eq. 1}$$

2. Multiply the fraction of the target pull value by the full half scale word value and round to the nearest whole number:

$$pullControlWordDec = round(fractionPull * 2^{25} - 1) \quad \text{Eq. 2}$$

3. Convert the result of step 2 to two's complement binary (*pullControlWordBin*).
4. Read Reg1 value from the device as it may include control bits for other settings.
5. Form the register content for writing:
    a. Reg0[16:0] – *pullControlWordBin[15:0] (LSW)*
    b. Reg1[9:0] – *pullControlWordBin[25:16] (MSW)*
    c. Reg1[15:10] – Do not change
6. Write registers with the sequence as follows:
    a. Reg0
    b. Reg1

# 4 Additional Functions

The output driver can be enabled or disabled through control registers. (The corresponding part number option should be selected to enable this function. Refer to the datasheet of the selected product family). To enable the output driver, Reg1[10] (address 0x01) should be set to 1; to disable set it to 0.

> **Important note:** By default (at startup) output is disabled in this mode and should be enabled by appropriate write operation after start-up.

# 5 Evaluation Tools

The SiT6722EB evaluation board (EVB) is designed for use with SiTime TCXOs. It supports the 5.0 x 3.2 mm 10-pin ceramic package. This EVB enables users to evaluate all aspects of the TCXO devices including signal integrity, phase noise, phase jitter, and output frequency digital control via $I^2C$ interface.

EVB Features:

- Support for all three Super-TCXO configuration modes: TCXO, VCTCXO, and DCTCXO
- Probing points for frequency measurements
- Connector access for controlling the output frequency via $I^2C$ interface
- Connector for current measurement

SiTime typically ships the EVB with the Super-TCXO mounted using SiTime-recommended reflow profile. The Super-TCXO device should only be evaluated in its original soldered down state for best signal integrity and frequency stability. The device performance is not guaranteed if it is de-soldered and then re-soldered either manually or via reflow process.

More details can be found in the SiT6722EB EVB user manual.

# Appendix A: Frequency Pulling Examples

## Example 1

**Pull range:** ±200 ppm (*pullRange*)

**Default output frequency:** 156.25 MHz

**Desired output frequency:** 156.2640625 MHz (*targetPull* = +90 ppm)

Follow this frequency pulling procedure:

1. *fractionPull = +90 / 200 = 0.45*
2. *pullControlWordDec = round(0.45 * $2^{25}$-1) = round(15,099,493.95) = 15,099,494*
3. *pullControlWordBin = 111001100110011001100110b = 0xE66666*

| 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **0** |

4. Register content for the writing is:

| | *pullControlWordBin[15:0]* | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Reg0** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **0** |

| | *Don't care* | | | | | *OEcontrol[0]* | *pullControlWordBin[25:16]* | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Reg1** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | **0** | **0** | **0** | **0** | **0** | **Do not change** | **0** | **0** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **0** |

### Example 2

**Pull range:** ±200 ppm (*pullRange*)

**Default output frequency:** 122.88 MHz

**Desired output frequency:** 122.873856 MHz (*targetPull* = -50 ppm)

Follow this frequency pulling procedure:

1. *fractionPull = -50 / 200 = -0.25*
2. *pullControlWordDec = round(-0.25 * $2^{25}$-1) = round(-8,388,607.75) = -8,388,608*
3. *pullControlWordBin = 11100000000000000000000000b = 0x3800000*

| 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

4. Register content for the writing is:

| **Reg0** | ***pullControlWordBin[15:0]*** | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| **Reg1** | ***Don't care*** | | | | | ***OEControl[0]*** | ***pullControlWordBin[25:16]*** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | **0** | **0** | **0** | **0** | **0** | **x** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

**Table 1: Revision History**

| Version | Release Date | Change Summary |
|---|---|---|
| 1.0 | 01/29/2019 | Initial release |

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