12.9 A 1.55×0.85mm² 3ppm 1.0µA 32.768kHz MEMS-Based Oscillator

Samira Zali Asl[1,2], Shouvik Mukherjee[1], Will Chen[1], Kimo Joo[1], Rajkumar Palwai[1], Niveditha Arumugam[1], Preston Galle[1], Meghan Phadke[1], Charles Grosjean[1], Jim Salvia[1], Haechang Lee[1], Sudhakar Pamarti[3], Terri Fiez[2], Kofi Makinwa[4], Aaron Partridge[1], Vinod Menon[1]

[1]SiTime, Sunnyvale, CA,
[2]Oregon State University, Corvallis, OR,
[3]University of California, Los Angeles, CA,
[4]Delft University of Technology, Delft, The Netherlands

Mobile time-keeping applications require small form-factor, tight frequency stability, and micro-power 32.768kHz clock references. Today's 32kHz quartz resonators and oscillators are facing challenges in size reduction [1,2]. Previously described MEMS-based oscillators can achieve tight accuracy but operate at high frequency with power unsuitable for mobile applications [3]. This paper introduces a 32kHz MEMS-based oscillator. Based on a comparison table of recent oscillators shown in Fig. 12.9.6, it offers the smallest size, 1.55×0.85mm², with the best frequency stability, 100ppm (XO) and 3ppm (TCXO) over the industrial temperature range of -40 to 85°C. Supply current is 0.9 and 1.0µA for XO and TCXO, respectively, at supply voltages from 1.5 to 3.6V.

A simplified block diagram of the MEMS-based oscillator is shown in Fig. 12.9.1. A 524kHz MEMS resonator and sustaining amplifier provide a frequency reference to a programmable fractional-N synthesizer, which in turn generates an accurate 32kHz output. The oscillator can be configured in either XO or TCXO mode. In XO mode, the fractional-N synthesizer compensates for the frequency inaccuracy due to process variations through a 2nd-order digital Delta-Sigma Modulator (DSM). In TCXO mode, a temperature-to-digital converter (TDC) and a 3rd-order polynomial additionally compensate frequency variation over temperature.

The capacitively transduced 524kHz MEMS resonator, shown in Fig. 12.9.2, has the following electrical characteristics: nominal quality factor (Q) of 52,000, nominal motional impedance (R_m) of 40kΩ, and resonant frequency variation of <100ppm over -40 to +85°C. The resonator is biased using a Charge Pump (CP) that triples a 1.2V regulated supply. A Pierce sustaining circuit maintains oscillation with a sub-threshold inverter. An Automatic Gain Control (AGC) [1] adjusts the g_m of this inverter at start up and over PVT variations. A series drive capacitor (C_{Drive}) is trimmed to compensate R_m variation over production. The total current consumption of the MEMS sustaining circuit and the CP is 240nA. Figure 12.9.3 shows the block diagram of the PLL and temperature-compensation path. The MEMS frequency is divided down to 32kHz by DSM controlled pre-divider. The PLL bandwidth is set to 1kHz to minimize the noise contribution from the pre-divider and the VCO. The VCO is a current-controlled ring oscillator with a nominal frequency of 262kHz. The current consumption of the PLL, including DSM, is 290nA.

In low-power mode, shown in Fig. 12.9.3, the PLL can be disabled and the output derived from the DSM controlled pre-divider. This introduces additional output jitter, but is not detrimental in applications that count pulses, e.g., 32,768 pulses to define one second. This low power XO mode (LPM) reduces chip current to 0.6µA for 1Hz rail-to-rail output clock with no external load.

The TDC shown in Fig. 12.9.3 employs a BJT-based temperature-sensing element [4]. This produces a PTAT voltage $\Delta V_{BE}=V_{BE2}-V_{BE1}$, using two equally sized BJTs biased with different currents I_2 and I_1 with a ratio of ρ. A 2nd-order ΔΣ modulator provides a digital bitstream whose average value is proportional to $(\alpha.\Delta V_{BE})/V_{BG}$, where $V_{BG}=V_{BE1}+\alpha.\Delta V_{BE}$. α and ρ are chosen to create a temperature-independent V_{BG}. To improve its accuracy and robustness, the TDC employs dynamic element matching in the BJT current sources, correlated double sampling in the first integrator, and chopping at the system level.

The TDC operates at a sampling frequency of 262kHz with an over-sampling ratio of 192. Each conversion takes 6ms with a current consumption of 4.5µA. This current consumption includes that of the decimation filter, digital filter, and clock generator. The resolution of the stand-alone TDC is 25mK/Conversion leading to a figure of merit (Energy/Conversion x Resolution²) of 24pJ°C² [5]. The TDC update rate is reduced by duty-cycling, but still guarantees <1ppm error during a 1°C/s temperature ramp. Clock gating in the digital circuitry is used to save power when the TDC is inactive. Figure 12.9.4 shows the current profile of the temperature-compensation engine. It takes 1ms for the BJT core and modulator to initialize, 6ms for two back-to-back conversions at 25°C, and 2ms to evaluate the polynomial. Two conversions are necessary for the system-level chopping. Duty cycling reduces TDC conversion rate to 3S/s and the average current to 100nA.

Replica biasing is employed in the digital regulator to guarantee timing closure over process and temperature. The replica structure in Fig. 12.9.3 consists of a series stack of NMOS and PMOS that matches the gates used in the standard cells. Driving a constant current into this series stack generates a voltage (VGS_{ref}) that results in a constant slew rate, and hence speed, in the digital gates. A resistor (R_{set}) adds output voltage margin to this replica structure. VDD_{dig} is generated using an open-loop unity gain buffer that ensures stability over all load conditions.

There are two options for the output driver: a rail-to-rail CMOS and a low-swing driver. With a low-swing driver, the CVF current can be reduced by V_{swing}/V_{DD}. As shown in Fig. 12.9.3, the driver has two regulators which together control its output swing. CMOS transmission gates are used to alternate between independently programmable V_{top} and V_{bottom}. Capacitive charge sharing generates fast output transitions followed by slow single pole settling from the regulators. To further reduce the output driver power consumption, the output frequency can be divided down to 1Hz in powers of 2.

Shown in Fig. 12.9.5, measured frequency stability over temperature (-40 to +85°C) is less than 100ppm for 85 XO devices and less than 3ppm for 45 TCXO devices. TCXOs are trimmed individually at several temperature points. Figure 12.9.5 also shows the hysteresis measured over 14 temperature cycles and tracking performance in the presence of a temperature transient as fast as 1.7°C/s on a TCXO device.

System performance is tabulated in Fig. 12.9.6 and compared to that of existing XO and TCXO devices. As shown, frequency stability over industrial temperature range is improved compared to other works. The total current consumption of this oscillator is 0.9µA and 1.0µA in XO and TCXO mode, respectively. The low-swing driver can be enabled to save power when driving external load capacitance. The low-power mode, with XO with PLL disabled, reduces the supply current further to 0.6µA. Figure 12.9.7 shows the 0.18µm CMOS die with area of 1.2mm² and MEMS die with area of 0.17mm². The MEMS resonator is flipped-chip bonded to the CMOS die in a 1.55×0.85mm² chip-scale package (CSP).

References:

[1] E. Vittoz, *et al.*, "High-Performance Crystal Oscillator Circuits: Theory and Application," *IEEE, J. Solid State Circuits*, vol. 23, no.3, pp. 774-783, June 1988.
[2] S. Dalla Piazza, "Quartz Tuning Forks: A High-Volume, Low-Cost, High-Tech MEMS Product," [Online].
Available: http://www.go4time.eu/publications/37-general.html.
[3] M. Perrott, *et al.*, "A Temperature-To-Digital Converter for a MEMS-based Programmable Oscillator with < ±0.5-ppm Frequency Stability and < 1-ps Integrated Jitter," *IEEE J. Solid-State Circuits,* vol. 48, no.1, pp. 276 - 291, Jan. 2013.
[4] M. A. P. Pertijs, *et al.*, "A CMOS Temperature Sensor with a 3σ Inaccuracy of 0.1°C from 55°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, Dec. 2005.
[5] K. Souri, *et al.*, "A CMOS Temperature Sensor with a Voltage-Calibrated Inaccuracy of ±0.15°C (3σ) from –55 to 125°C," *IEEE J. Solid-State Circuits,* vol. 48, no.1, pp. 292-301, Jan. 2013.

 978-1-4799-0920-9/14/$31.00

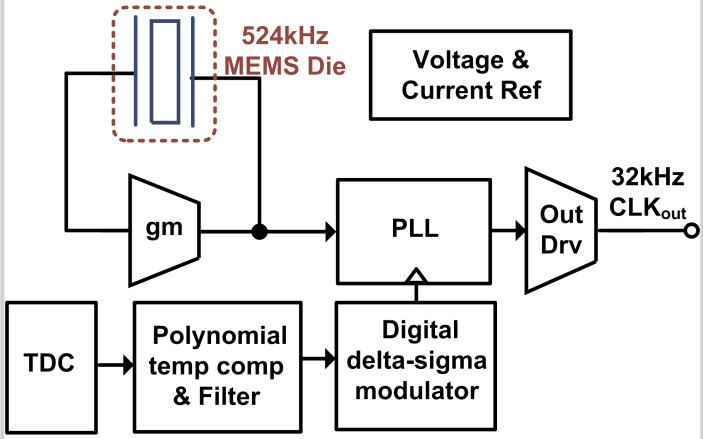

Figure 12.9.1: Simplified block diagram of MEMS-based TCXO. In XO mode, TDC and polynomial temperature compensation blocks are disabled.

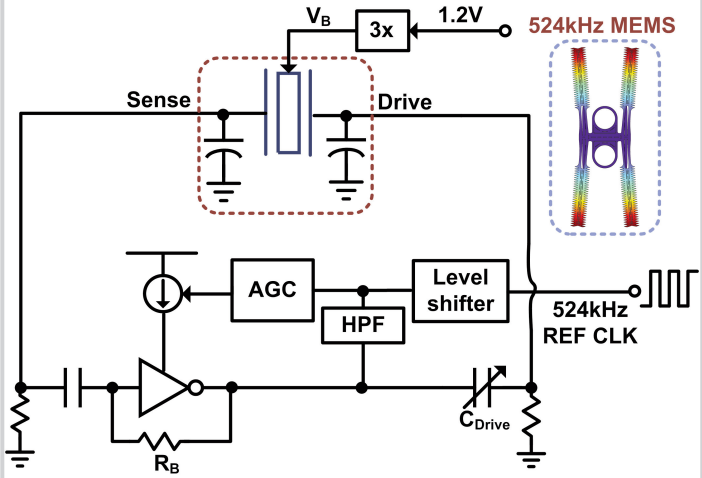

Figure 12.9.2: MEMS resonator, its bias (VB) and 524kHz sustaining oscillator block diagram. RB is replica-biased transistor operating in sub-threshold.

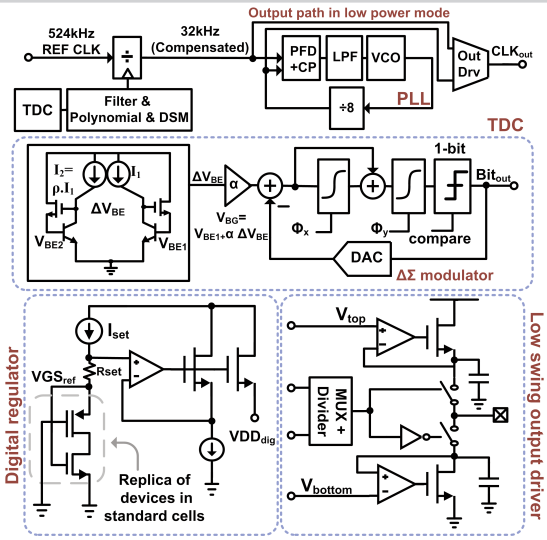

Figure 12.9.3: The Fractional-N synthesizer including temperature-compensation path, TDC, digital regulator, and low-swing driver.

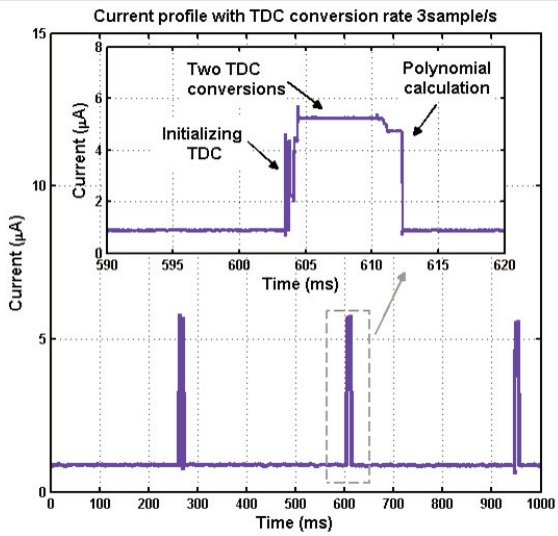

Figure 12.9.4: Supply current profile in TCXO mode. TDC conversion rate is 3S/s.

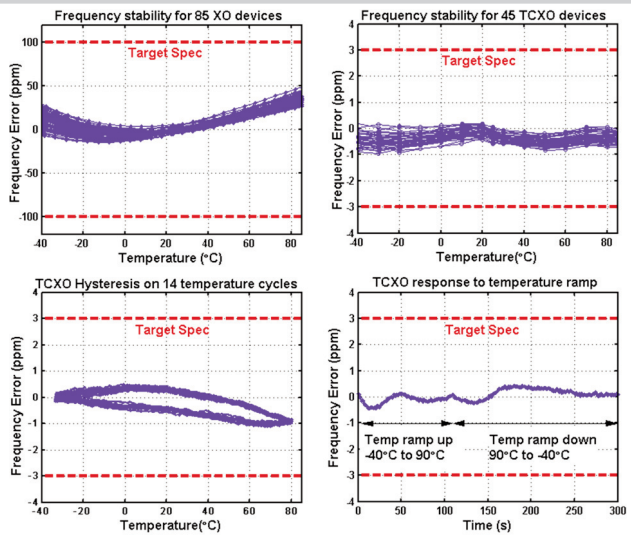

Figure 12.9.5: Frequency stability vs. temperature for XO and TCXO, TCXO Hysteresis, and its response to temperature ramp.

	XO			TCXO			
Parameter	This work	Epson SG-3050	Micro crystal OV-7604	This work	Maxim DS32KHz	Epson TG-3530	Kyocera KT3225T
Supply Voltage (V)	**1.2 to 3.63**	1.2 to 5.5	1.2 to 5.5	**1.5 to 3.63**	2.7 to 5.5	2.2 to 5.5	2 to 5.5
Temperature Range (°C)	**-40 to 85**	-20 to 70	-40 to 85	**-40 to 85**	-40 to 85	-20 to 70	-40 to 85
Frequency Stability vs. Temp (ppm)	**100 max**	120 max	160 max	**±3**	±7.5	±5	±5
Supply sensitivity (ppm/V)	**±0.25**	±3	±1.5	**±0.25**	2.5	±1	±1
OSC Start up (s)	**0.2**	1	0.5	**0.5**	1	3	3
Current (μA) Clock enabled, no load	**0.9 typ 1.4 max 0.6 LPM**	-Typ 2 max	0.5 typ 0.7 max	**1 typ 1.5 max**	1.85 typ 4 max	1.7 typ 4 max	1.5 typ 4 max
Package size (mm²)	**1.55x0.85**	2.2x1.4	3.2x1.5	**1.55x0.85**	18.5x6.35	5x10.1	3.2x2.5

Figure 12.9.6: Performance comparison with previous low-power 32kHz XOs and TCXOs.

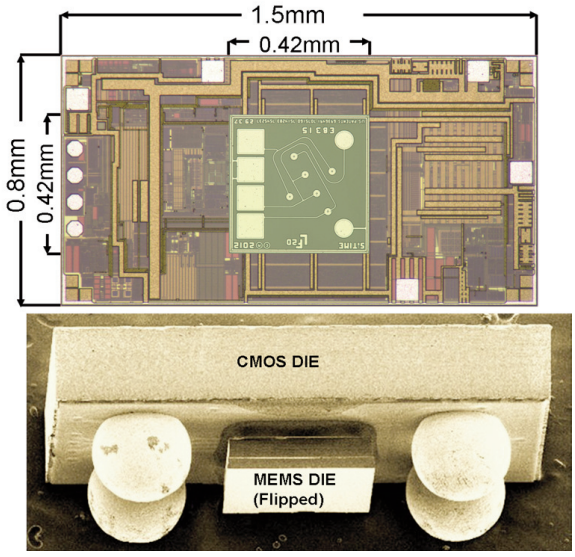

Figure 12.9.7: Micrograph of MEMS and CMOS dies and final CSP package.

978-1-4799-0920-9/14/$31.00