
Decoupling, Bypassing, and Layout Recommendations for SiTime Oscillators

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1 Introduction

Proper decoupling, bypassing, and power supply noise reduction is important in many applications to ensure optimal performance for oscillators. A common strategy is to place capacitors near high speed devices on a Printed Circuit Board (PCB). Such capacitors serve two important functions:

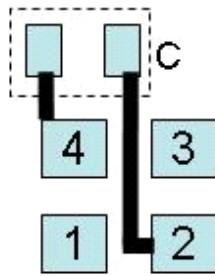
- Provide instantaneous current to the component
- Reduce noise propagation through the system
- Shunt the power supply noise to GND

Following sections describe decoupling, bypassing, and noise rejection recommendations for SiTime single-ended and differential devices.

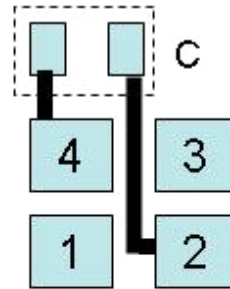
2 Decoupling

Fast switching devices such as clock oscillators place a significant demand on the power source. The high clock rate coupled with the fast rise time (typically in the 1 ns range) makes it very difficult for the power supply to source the required current in a timely manner. As a result, the supply voltage level at the device will sag. To ensure that an adequate amount of charge is always available to the device, a decoupling capacitor is installed to act as a local reservoir.

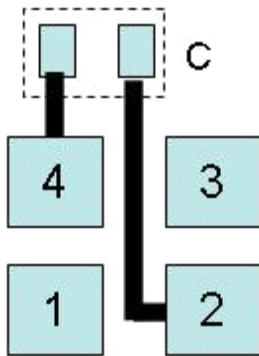
SiTime recommends using a 0.1uF ceramic decoupling capacitor between the VDD pin of the oscillator and the ground plane for both single-ended and differential devices. Figure 1 and Figure 2 show a sample layout for the SiTime 4-pin oscillator with a 0603-size, 0.1uF decoupling capacitor C. All traces shown on Fig.1 and Fig.2 need to be covered with solder mask. Pin 1 of the clock may be used to support functions such as Output Enable, Standby, Spread Disable, or VCMO control.



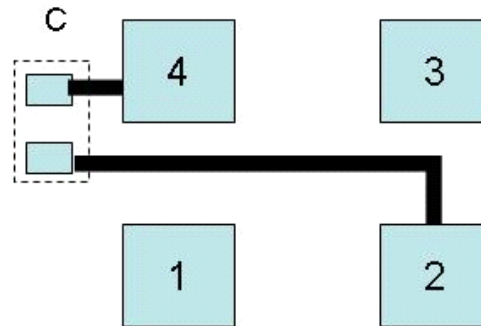
(a) 2.5mm x 2.0mm package



(b) 3.2mm x 2.5mm package

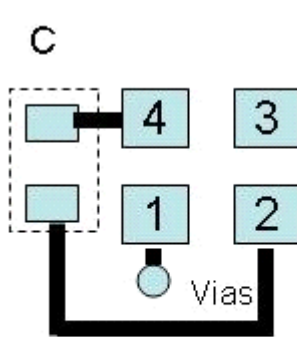


(c) 5.0mm x 3.2mm package

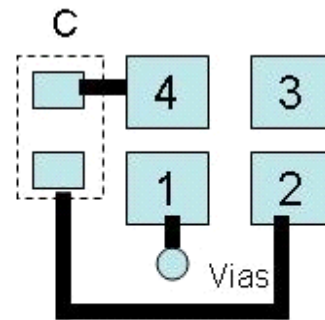


(d) 7.0mm x 5.0mm package

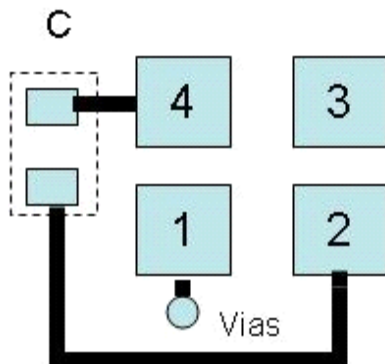
Figure 1: Layout Example for 4-pin SiTime device with decoupling capacitor for case when board fabrication technology allows trace routing between oscillators pins



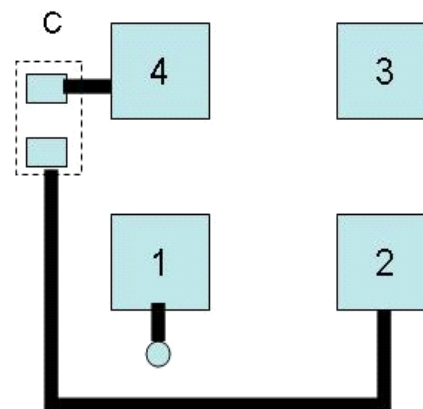
(a) 2.5mm x 2.0mm package



(b) 3.2mm x 2.5mm package



(c) 5.0mm x 3.2mm package



(d) 7.0mm x 5.0mm package

Figure 2: Layout Example for a SiTime Device with a Decoupling Capacitor for case when board production technology doesn't allow traces between oscillators pins.

3 Bypassing

With today's high processor speeds and data rates, there is a considerable amount of noise in the system. The nearly square waveforms produced by the clock oscillators contain the fundamental frequency of the unit as well as the higher harmonic components of the signal. To limit the amount of noise propagating through the system, bypass capacitors are needed to provide low-impedance paths to shunt this transient energy to ground.

In most applications, the 0.1uF decoupling capacitor provides sufficient bypass capability for all SiTime devices. No additional bypass capacitors are required.

The user may consider using an additional 1nF or 10nF bypass for SiTime oscillators with differential outputs operating at high frequencies (above 150 MHz) to suppress the higher clock harmonics on the power supply network.

4 Power Supply Noise Reduction

In most applications, a single 0.1 μ F capacitor between VDD and GND shunts much of the noise that may exist on the power supply to GND. SiTime devices use internal regulator to reduce the impact of the power supply noise. However, to minimize any residual power supply noise impact on the oscillator output jitter even further, the user may consider RC or LC power supply filtering strategies. SiTime recommends using such filtering for high-speed applications, such as serial interfaces with greater than 6Gbps baud rates (e.g., 8.5Gbps Fibre Channel and Serial 10Gbit Ethernet).

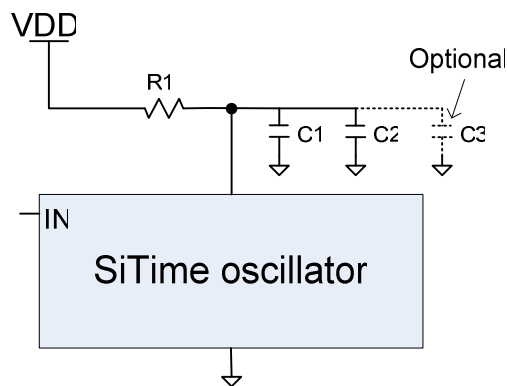


Figure 3: RC power supply filter

The RC filtering, shown in Figure 3, is simple to use. The R needs to be selected such that the nominal voltage drop on the resistor is in the range of 5% of nominal power supply voltage. Table 1 shows the values for different SiTime oscillators.

Table 1: Recommended component values for RC power supply filter

Device	R1 (Ω)	C1 (μ F)	C2 (μ F)	C3 (μ F)
SiT8102, SiT9001	3	10	0.1	0.01
SiT8103, SiT3701, SiT8033, SiT9003, SiT8003	5	1	0.1	N/A

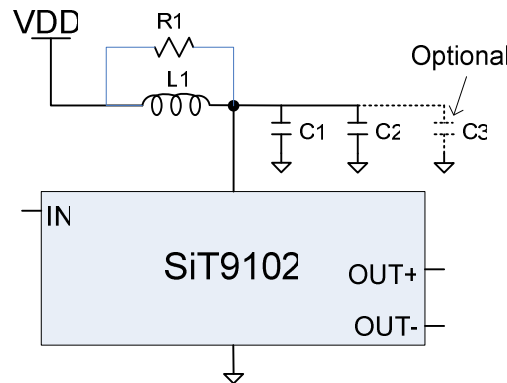


Figure 4: LC power supply filter

The LC filtering, shown in Figure 4, is especially suitable for devices with higher current consumption, such as differential oscillators. The inductor low series resistance (typically less than 1Ω) delivers the DC supply voltage to the device with less than 50mV drop. The LC filter had the added advantage of minimizing potential oscillator switching noise from the power network. The resistor in parallel with inductor is intended to reduce the peaking at the resonance frequency of the LC circuit. Table 2 lists the recommended component values for LC power supply filter for 9102 devices. The same filter can also be used with other SiTime differential or single-ended oscillators (with and without spread spectrum feature), and VCMOs.

Table 2: Recommended component values for LC power supply filter

Components	L1	C1	C2	C3	R
SiT9102, SiT9002	1uH to 10uH I _{max} >140mA	10 μF	0.1 μF	0.01 μF	50 Ω

5 Layout Recommendations for SiTime Clocks

Some common guidelines for PCB designs are:

- Decoupling capacitors between VDD and ground of the clock source are essential to reduce noise that may be transmitted to the clock signal. These capacitors must be placed as close to the VDD pin as possible – 1-2 mm.
- Physically locate the clock source chip as close to the load
- Limit the trace lengths for clock signals.
- Do not route clock signal close to the board edge.
- Do not route power traces or other high frequency signals below the oscillator PCB area. A Ground layer below the oscillator is highly recommended
- Avoid using vias in clock signal routings if possible. Vias change the trace impedance causing, which may cause reflections.

- Do not route clock traces on the power and ground layer.
- Avoid right angle bends in a trace and if possible keep trace routings straight. If a bend is necessary make it with two 45 deg. corners or by using round bend.
- When routing differential signals, ensure the electrical length of the traces within one pair match.



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