

Decoupling, Bypassing, and Layout Recommendations for SiTime Clocks

1 Decoupling and Bypassing

Capacitors placed near high speed devices on a Printed Circuit Board (PCB) serve two important functions:

- Provide instantaneous current to the component
- Reduce noise propagation through the system

1.1 Decoupling

Fast switching devices such as clock oscillators place a significant demand on the power source. The high clock rate coupled with the fast rise time (typically in the 1 ns range) makes it very difficult for the power supply to source the required current in a timely manner. As a result, the supply voltage level at the device will sag. This phenomenon is sometimes referred to as the “voltage droop”. To ensure that an adequate amount of charge is always available to the device, a decoupling capacitor is installed to act as a local reservoir.

SiTime recommends using a 0.1uF ceramic decoupling capacitor between the VDD pin of the oscillator and the ground plane. If space permits, adding a second ground via is recommended to reduce the inductance to the ground plane. Figure 1 shows a sample layout for the SiTime SiT8102 clock oscillator with a 0603-size, 0.1uF decoupling capacitor.

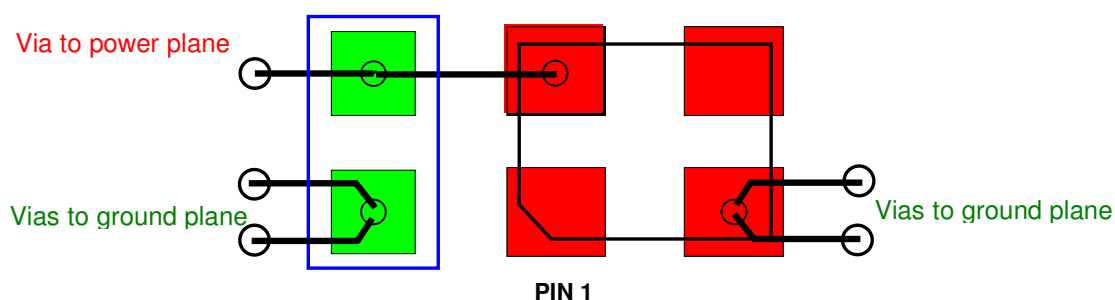


Figure 1. Layout Example for a SiTime Device with a Decoupling Capacitor

This layout assumes that pin 1 of the clock is used to support functions such as Output Enable or Standby. Therefore, space is provided to allow a trace to be routed in the top layer of the PCB to pin1.

1.2 Bypassing

With today's high processor speeds and data rates, there is a considerable amount of noise in the system. The nearly square waveforms produced by the clock oscillators contain the fundamental frequency of the unit as well as the higher harmonic components of the signal. To limit the amount of noise propagating through the system, bypass capacitors are needed to provide low-impedance paths to shunt this transient energy to ground.

In most applications, the 0.1uF decoupling capacitor provides sufficient bypass capability for all SiTime devices. No additional bypass capacitors are required.

For SiTime oscillators with differential outputs operating at higher frequencies (above 200 MHz), the user may consider using an additional 1nF bypass capacitor to suppress the higher harmonics.

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