

# SiT9102AC for Ethernet

LVPECL oscillator for Gb-Ethernet and 10Gb-Ethernet



## ■ Features

- Low rms phase jitter (random) of 0.5 ps
- 125MHz, 156.25MHz, and 161.1328 MHz output frequencies
- Extended commercial temperature range, -20 to 70°C
- High frequency stability of  $\pm 25$  PPM
- Available in two industry standard packages: 5.0 x 3.2 x 0.75 mm and 7.0 x 5.0 x 0.90 mm
- All-silicon device with outstanding reliability of 2 FIT, 10x improvement over quartz-based devices, enhancing system MTBF
- Ultra short lead time
- Please refer to SiT9102 datasheet for other frequencies (up to 800 MHz) and signaling levels (LVDS, HCSL, CML)
- Custom frequencies, such as 156.25391 or 125.00625 MHz that improve throughput or eliminate bit errors are also available. Contact your local SiTime Sales Representative for more information.

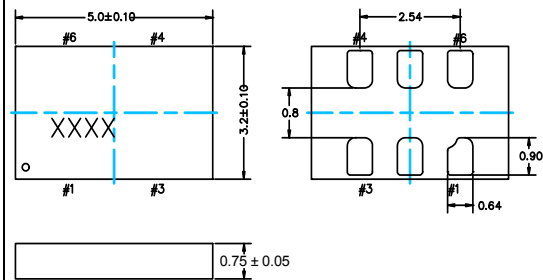


## ■ Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	–	125	–	MHz	
		–	156.25	–	MHz	
		–	161.1328	–	MHz	
Frequency Tolerance	F_tol	-25	–	+25	PPM	Inclusive of: Initial tolerance, operating temperature, rated power, supply voltage change, load change, aging (1st yr @25°C), shock and vibration.
Aging	Ag	-1.0	–	1.0	PPM	1st year at 25°C
Storage Temperature Range		-55	–	+125	°C	
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Please contact SiTime
Supply Voltage	Vdd	2.25	2.5	2.75	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd		75	84	mA	Vcc = 3.3V or 2.5V. Excluding load termination current
Standby Current	I_std	–	–	10	μA	
Duty Cycle	DC	45	50	55	%	
Rise/Fall Time	Tr, Tf	100	150	300	ps	Vdd = 3.3V, 20% - 80% Vdd level
		100	150	300	ps	Vdd = 2.5 V, 20% - 80% Vdd level
Output High Voltage	VOH	Vdd - 1.1	–	Vdd - 0.7	V	50 Ohm termination to GND, see figure 1 and 2.
Output Low Voltage	VOL	Vdd - 2.0	–	Vdd - 1.4	V	
Pk-Pk Output Voltage Swing	Vsw	600	800	1000	mV	
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE
Startup Time	T_osc	–	–	10	ms	Measured from the time Vdd reaches its rated minimum value
RMS Phase Jitter (random)	T_jitt	–	0.5	–	ps	f = 156.25 or 161.1328 MHz, BW: 1.875 MHz to 20 MHz
RMS Period Jitter	P_jitt	–	1.3	1.8	ps	f = 156.25 or 161.1328 MHz, BW: 1.875 MHz to 20 MHz

■ Dimensions, Pin Description and Land Pattern

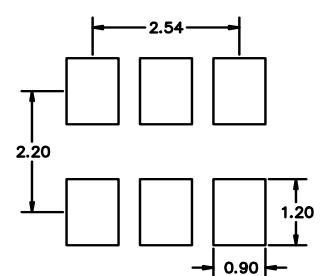
Dimensions (Unit: mm)<sup>[1]</sup>  
**5.0 x 3.2 x 0.75 mm**



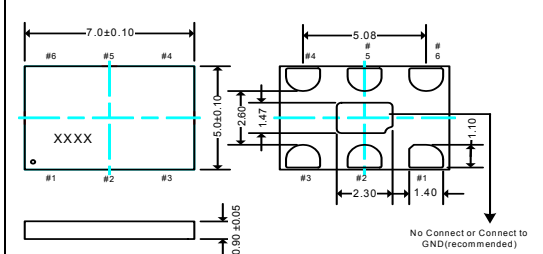
Pin Map	
Pin	Connection
1	OE
2	No Connect
3	GND
4	OUT+
5	OUT-
6	Vdd

Pin #1 Functionality	
OE	
H or Open	specified frequency output
L	output is high impedance

Recommended Land Pattern (Unit: mm)<sup>[2]</sup>



Dimensions (Unit: mm)<sup>[1]</sup>  
**7.0 x 5.0 x 0.90 mm**



Recommended Land Pattern (Unit: mm)<sup>[2]</sup>

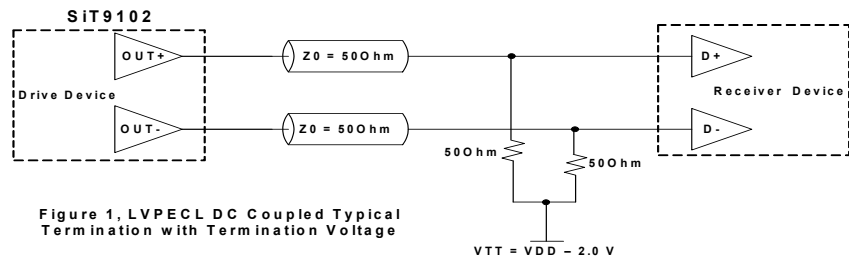
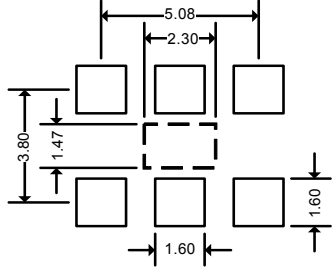


Figure 1, LVPECL DC Coupled Typical Termination with Termination Voltage

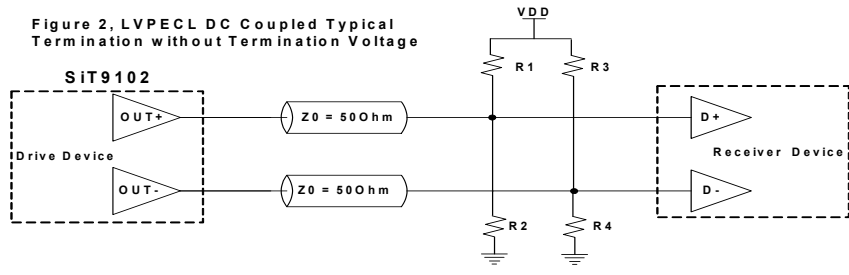


Figure 2, LVPECL DC Coupled Typical Termination without Termination Voltage

<b>VDD = 3.3V</b>
R1 = R3 = 133 Ohm
R2 = R4 = 82 Ohm
<b>VDD = 2.5V</b>
R1 = R3 = 250 Ohm
R2 = R4 = 62.5 Ohm

Notes:

- XXXX top marking denotes manufacturing lot number.
- A capacitor of value 0.1 μF between Vdd and GND is recommended.

Ordering Part number	Frequency (MHz)	Package size (mm)	Vdd (V)	Feature Pin
SiT9102AC-142N33E125.00000T	125	7.0 x 5.0 x 0.90	3.3	OE
SiT9102AC-132N33E125.00000T	125	5.0 x 3.2 x 0.75	3.3	OE
SiT9102AC-142N25E125.00000T	125	7.0 x 5.0 x 0.90	2.5	OE
SiT9102AC-132N25E125.00000T	125	5.0 x 3.2 x 0.75	2.5	OE
SiT9102AC-142N33E156.25000T	156.25	7.0 x 5.0 x 0.90	3.3	OE
SiT9102AC-132N33E156.25000T	156.25	5.0 x 3.2 x 0.75	3.3	OE
SiT9102AC-142N25E156.25000T	156.25	7.0 x 5.0 x 0.90	2.5	OE
SiT9102AC-132N25E156.25000T	156.25	5.0 x 3.2 x 0.75	2.5	OE
SiT9102AC-142N33E161.13280T	161.1328	7.0 x 5.0 x 0.90	3.3	OE
SiT9102AC-132N33E161.13280T	161.1328	5.0 x 3.2 x 0.75	3.3	OE
SiT9102AC-142N25E161.13280T	161.1328	7.0 x 5.0 x 0.90	2.5	OE
SiT9102AC-132N25E161.13280T	161.1328	5.0 x 3.2 x 0.75	2.5	OE

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