Termination Recommendations for SiTime Single-ended Oscillators

Printed Circuit Boards (PCB) are the most common transmission medium used for mounting oscillators and routing clock signals in a system level board design. PCB land patterns above a certain frequency however stop acting like simple wire connections and start behaving like complex transmission lines. The consequence of this behavior results in the distortion of the clock signal. Typical manifestations of this distortion are ringing, overshoot, and undershoot of the clock signal. The length of the PCB trace in relation to the highest frequency component of the clock signal determines when a land pattern stops behaving as a simple connection and starts behaving like a complex transmission line. A square wave contains energy at the fundamental clock frequency and also at the higher harmonics. It is this energy contained in the higher harmonics that must be examined. To accurately reproduce a clock signal at the input to the receiving circuitry without distortion, the connecting PCB land pattern must pass all of the energy contained in the original clock signal without distortion. A 10 MHz clock pulse with a 1ns Rise Time is just as prone to exhibiting poor signal integrity as a 125 MHz clock signal with a 1ns Rise Time.

A basic rule of thumb is that when the propagation delay (T_{PD}) of the clock signal traveling through the trace starts to approach the Rise Time (T_R) of the clock signal then the length of the line is critical and the PCB trace will begin to behave like a transmission line. This is expressed in Equation 1.

$$L_{MAX} < \left(\frac{T_R}{2T_{PD}} \right)$$

Equation 1

L = Line (trace) Length
T_R = Rise Time
T_{PD} = Propagation Delay per unit length

The longer the PCB trace the more likely that it will behave like a transmission line. Reflections occur on a transmission line when there is a mismatch between the characteristic impedance of the line and the source and load impedance. It is these signal (voltage) reflections that add and subtract to the original (incident) wave that cause distortion in the clock signal normally seen as ringing, overshoot, and undershoot. There is debate in the literature as to when the line length presents a

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problem with signal integrity. PCB design and signal integrity simulation software should be employed to analyze and solve this problem.

SiTime recommends that the trace length be kept short so that transmission line effects do not occur and distort the signal integrity of the clock signal. On a system level board PCB traces and ground planes typically take the form of Microstrip Transmission Lines (Figure 2), and Stripline Transmission Lines (Figure 3). Both of these transmission line structures are unbalanced lines; when a scope probe is connected to the signal and ground lands of these lines then both sides of the scope probe connections should be kept as short as possible. Do not use a long *pig tail* ground connection for the probe as this will add length to the line and reflections will occur resulting in ringing, overshoot, and undershoot.

If longer traces have to be employed then the transmission line Application circuit (Figure 1), can be employed.

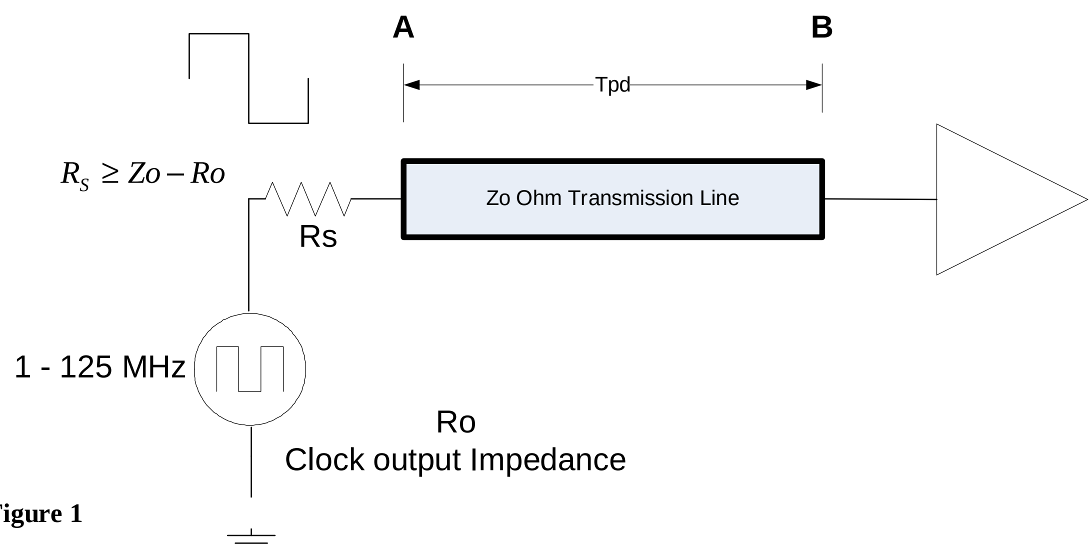

Figure 1

The output impedance of most CMOS clock oscillators is low therefore a resistor installed as close to the output PIN as possible can be used to match the output impedance of the clock generator to the transmission line. The typical output impedance for the SiTime SiT8002 clock generator is 30 Ω. Therefore a customer driving a transmission line with characteristic impedance Zo of 50 Ω would place a 20 Ω high quality SMD resistor on the output of the clock generator as close to the output PIN as physically possible. It is also desirable but not always practical to

match the load impedance to the line impedance. Typical load impedances are usually high resulting in a reflected wave that is sent back to the source where the subsequent use of a series termination resistor will prevent the reflection of the wave that was reflected back from the load. The addition of the series termination resistor is a "compromise solution" and will result in a degradation of the Rise Time and absolute voltage levels. This technique is not recommended for driving multiple loads. A fan-out buffer should be used for driving multiple loads and the input to the buffer should be placed as close to the clock oscillator as possible.

(1) $$t_{pd} = 1.017\sqrt{0.45e_r + 0.67}$$

(2) $$Zo = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98}{0.8w + t}\right)$$

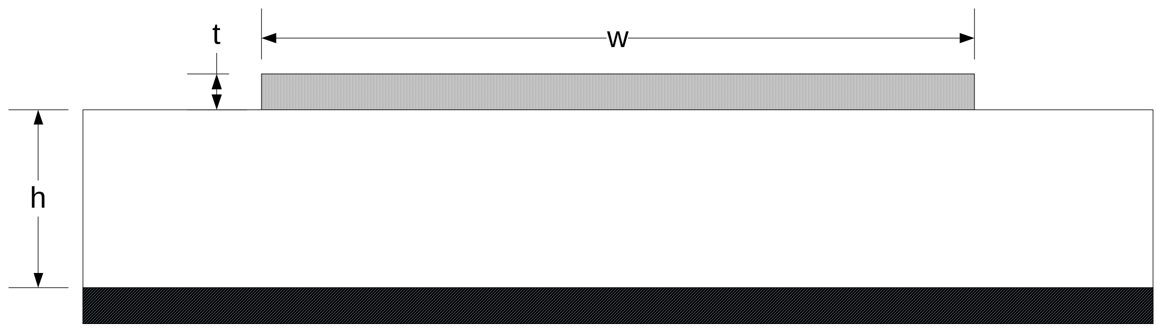

Figure 2 Microstrip

(3) $$t_{pd} = 1.017\sqrt{e_r} \text{ (ns/ft)}$$

(4) $$Zo = \frac{60}{\sqrt{e_r}} \ln\left[\frac{4b}{0.67\pi(0.8w + t)}\right]$$

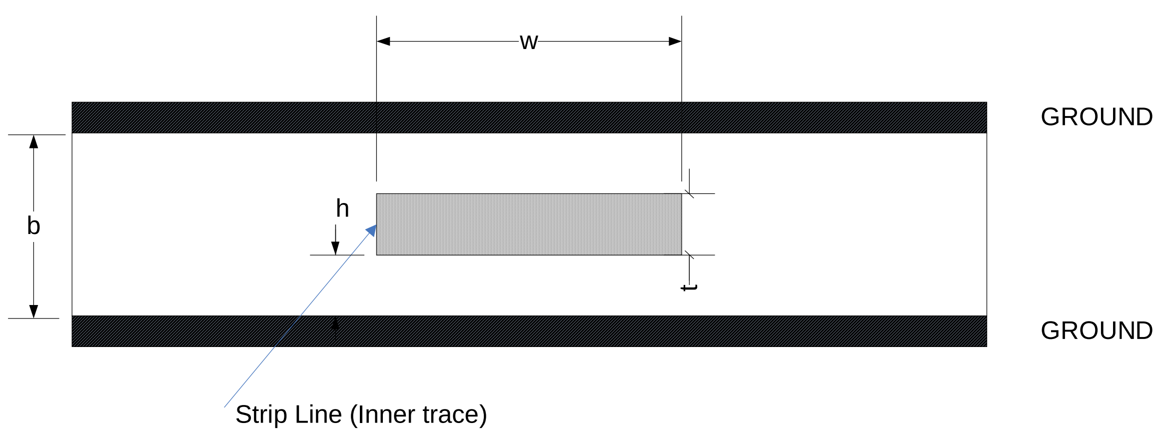

Figure 3 Stripline

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Conclusion

The exact value of the series termination resistor should be found initially by simulation and finally arrived at through empirical trial and error by testing on the prototype system board. SiTime does not recommend the use of vias and or internal traces to route clock signals.

Proper measuring techniques should be employed. Land patterns and traces should be kept as short as possible. A 0.1µF decoupling capacitor should be placed as close as physically possible to the SiT8002 and should be connected between the PIN 4 VDD (power supply) and PIN 2 (ground) to ensure data sheet performance.

References

1. Johnson, Howard & Graham, Martin "High-Speed Digital Design" Prentice Hall, 1993

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