11.1 Dual-MEMS-Resonator Temperature-to-Digital Converter with 40μK Resolution and FOM of 0.12pJK²

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Precision MEMS oscillators require a temperature-to-digital converter (TDC) that adjusts the multiplication factor of a fractional-N PLL in order to compensate for the MEMS resonator's frequency variation over temperature [1]. This compensation, however, provides a path for the TDC's noise to propagate to the oscillator's output as phase noise (PN). Previous work has sought to minimize this noise, by using high-resolution TDCs, e.g., the MEMS-thermistor based TDC described in [1]. This paper presents a TDC based on dual-MEMS resonators [2-3] that has no significant impact on oscillator PN. In a 130Hz bandwidth (BW), the sensor achieves a thermal-noise-limited resolution of 40μK, leading to a resolution FOM (Energy/Conversion × Resolution²) of 0.12pJK², 5× better than the state of the art [4].

Telecom applications require clocks with an Allan Deviation (ADEV) of better than 10^{-10} in a 1s integration time, or a PN less than -59dBc at 1Hz offset frequency for a 48MHz clock, decreasing by 30dB/decade. Such applications also require ±0.1ppm frequency stability from -40 to 85°C, which has to be maintained during temperature ramps of 1°C/s and thermal transients, usually within a 100Hz BW. The MEMS oscillator described in this work meets the PN requirement with no temperature compensation (XO). However, to meet the stability requirements, temperature compensation (TCXO) is essential.

The best reported TDC resolution is 100μK (rms) at 10S/s with an FOM of 13pJK² [1]. In this work, the MEMS frequency varies by up to 1ppm/K. To avoid degrading the TCXOs PN, a TDC resolution of at least 50μK at 200S/s is needed. Scaling the architecture in [1] to meet this requirement would necessitate a power consumption of 1W. The sensor in [4] achieves what appears to be the best energy-efficiency to date, with an FOM of 0.52pJK², but at 10mK (rms), its resolution is far insufficient. In addition, both of these optimal examples are thermistor-based and are unlikely to meet the ±0.1ppm stability requirement (including hysteresis) over lifetime. Other TDC types, e.g., BJT-based sensors, have not yet achieved the required resolution and energy efficiency [5]. The presented dual-MEMS resonator TDC in this work enables us to simultaneously achieve the target resolution, BW, FOM and the stability.

Figure 11.1.1 depicts the programmable oscillator with two MEMS resonators on one die, attached to a CMOS die that includes two oscillator sustaining circuits, a frequency ratio engine and a frequency synthesizer. In this architecture, the temperature information is obtained from the ratio of the two MEMS frequencies [6]: a temp-sense frequency f_{TS} (45MHz) and a temp-flat frequency f_{TF} (47MHz), with temperature coefficients of -7ppm/K and 1ppm/K, respectively. Their ratio thus has a temperature coefficient of about -8ppm/K.

Figure 11.1.2 shows the frequency ratio engine, which consists of one PLL nested within another. A digital PLL (DPLL) locks the f_{TS} to a scaled value of f_{TF} that is provided by the nested analog fractional-N PLL (APLL) and serves as the digitally controlled oscillator (DCO) of the DPLL. The fractional divide value of the APLL is the scaled ratio of the two frequencies. The DCO's output frequency is divided by 10 to optimize power and performance in the process used. The fractional divide value is applied to the TDC datapath composed of a 7th-order polynomial and an elliptic low-pass filter. The filtered result is then used to stabilize the reference frequency f_{TF} by modifying the programmable frequency multiplier (PFM) value of the frequency synthesizer [1], thus resulting in a stable frequency at the synthesizer's output.

The DCO is a 3rd-order fractional-N PLL, designed for 2MHz BW and composed of an XOR-based PFD, a 2nd-order loop filter and a 9-stage ring oscillator. As shown in the simplified block diagram of Fig. 11.1.3, the DPLL includes a digital phase quantizer and a loop filter. The digital PFD employs a coarse quantizer made of a 4b counter that counts every rising edge of the VCO output, and a fine quantizer that consists of 9 arbiters that sample all phases of the ring oscillator. Each rising edge of Clk_{TS} latches the coarse and fine quantizer outputs. Since only rising edges of the ring oscillator's internal nodes are used, the quantization step is 1/9th of a VCO period. The total phase travelled by the VCO in a period of Clk_{TS} is measured by summing the difference of two consecutively latched quantizer outputs, while the coarse value is multiplied by 9. This value is subtracted from a digital constant (STEP=90) that represents the desired VCO phase increment in the locked condition at every sample. It is then fed to an integrator and 5kHz BW digital loop. The loop filter's output contains temperature information, which is used to control the DCO frequency and modify the PFM value after being processed in the TDC datapath.

Since the TDC output should exactly compensate for Clk_{TF} variations across temperature, its static gain must be about -1ppm/K. Figure 11.1.4 shows that at 1s integration time, the ADEV of the oscillator frequency is about 8×10^{-11}. Given that the oscillator ADEV is not dominated by the TDC, the TDC noise ADEV must be less than 80μK. Because the TDC's resolution is at the tens of μK level, directly measuring it is challenging due to the various sources of on and off-chip thermal drift present in the measurement setup and the climate chamber. Therefore, the resolution was instead estimated from the measured noise contribution of the TDC to the output clock PN. In the TCXO mode, TDC noise does not significantly impact the PN over the full frequency spectrum. However, turning off the elliptic filter in the TDC data path results in a PN bump in the frequency range of about 300Hz to 8kHz, as shown in Fig. 11.1.4. In order to measure the TDC's contribution on PN, the TDC datapath is gained up by 26dB. This can be verified by measuring the amount of PN increment of the bump. This method increases the TDC noise contribution to the output clock PN to a measurable value. The exact relationship between the TDC output and temperature was determined by ramping the temperature over a small range and observing the resulting oscillator drift with the gained up TDC, as shown in Fig. 11.1.4. Based on this calibration, the TDC's resolution was found to be less than 40μK (rms) in a 130Hz BW.

As plotted in Fig. 11.1.5, TCXO devices have <±100ppb output clock frequency stability over the temperature range from -40 to +85°C, while varying under 100ppm for the XO parts. Figure 11.1.5 also includes the hysteresis measurement over 9 temperature cycles. The hysteresis window is <30ppb and is mainly dominated by about 15°C temperature offset between the up and down temperature ramps, due to the measurement setup.

The TDC's performance is tabulated in Fig. 11.1.6 and compared with previously reported high-resolution TDCs. As shown, the described TDC improves the state-of-the-art resolution by over 2×, but in a 25× shorter conversion time. The resulting resolution FOM is 0.12pJK², about 5× better than the state of the art [4]. Figure 11.1.7 shows the chip micrograph of the prototype sensor in which the MEMS resonators die is flipped and attached to the 0.18μm CMOS die. The overall chip current (at 20MHz output frequency, no-load) was measured to be about 48mA. At 1.6V supply, the TDC (including analog and digital circuits) along with the sustaining circuits for both oscillators consumes about 12mA, of which 1.5mA and 2mA is estimated for the TDC analog and digital portion, respectively.

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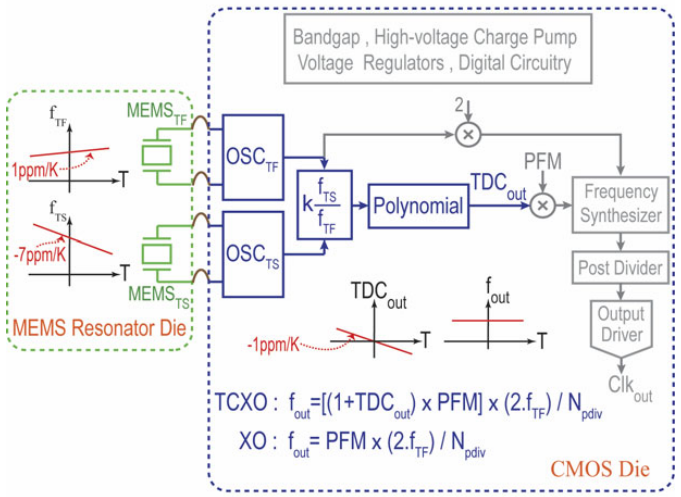

Figure 11.1.1: The MEMS resonator die is attached to the CMOS die consisting of sustaining circuits, the frequency ratio engine and the frequency synthesizer.

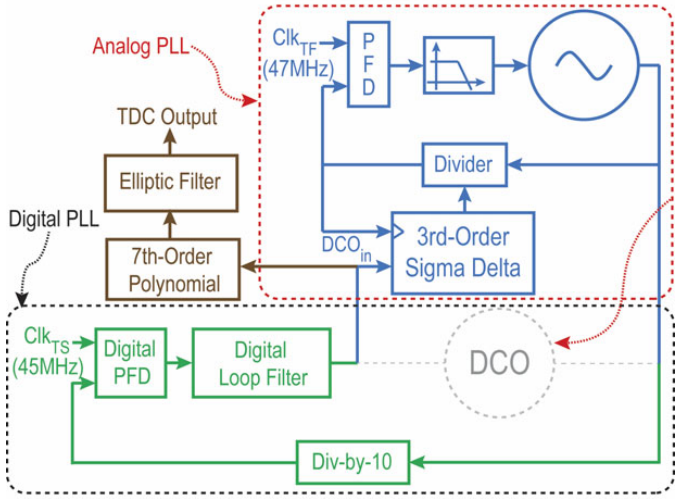

Figure 11.1.2: Simplified block diagram of the frequency ratio engine of the dual-resonator TDC, composed of the digital PLL, the analog PLL and the TDC datapath.

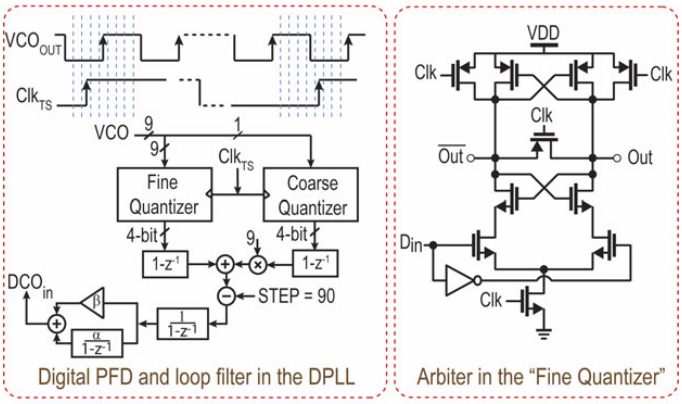

Figure 11.1.3: Simplified block diagram of the digital PFD, the digital loop filter as well as the arbiter circuit, connected to each phase of the ring oscillator, used in the fine quantizer.

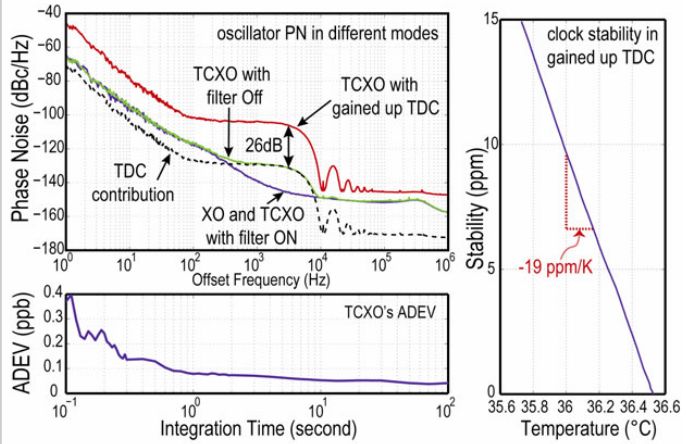

Figure 11.1.4: Measured PN for a 20MHz clock for different operation modes, TCXO's ADEV and oscillator frequency drift vs temperature for the gained up TDC.

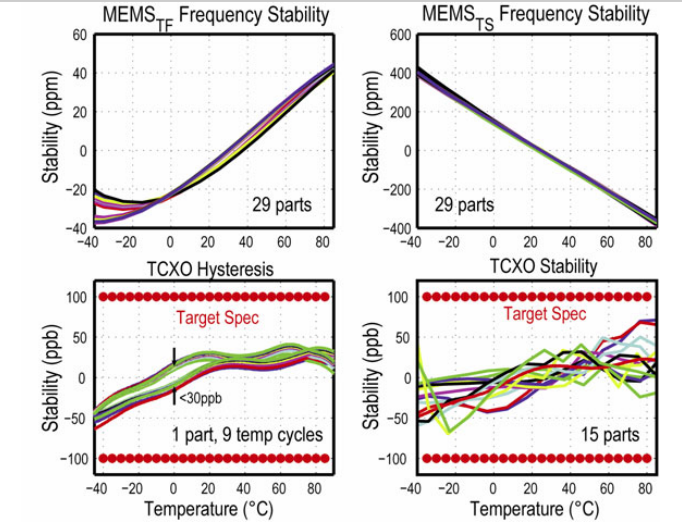

Figure 11.1.5: TF and TS frequencies plus frequency stability of 15 TCXO parts; TCXO hysteresis in a temperature ramp of 1°C/min.

	This work	[4]	[7]	[1]	[8]
Sensor Type	**Dual-MEMS Resonator**	Resistor	Resistor	Resistor	BJT
CMOS Technology	**0.18µm**	0.18µm	0.18µm	0.18µm	0.7µm
Chip Area	**0.54 mm²**	0.43 mm²	0.09 mm²	0.18 mm²	1.5 mm²
Power Consumption	**19mW**	51.6µW	31µW	13mW	159µW
Temperature Range	**-40°C to 85°C**	-40°C to 125°C	-40°C to 85°C	-40°C to 85°C	-40°C to 125°C
Conversion Time	**3.85ms**	0.1ms	32ms	100ms	2.2ms
Resolution	**0.04mK**	10mK	2.8mK	0.1mK	3mK
Resolution FoM[1]	**0.12pJK²**	0.52pJK²	8pJK²	13pJK²	3.2 pJK²

[1]Resolution FoM = Energy / Conversion × (Resolution)²

Figure 11.1.6: Performance comparison with previous state-of-the-art high-resolution temperature sensors.

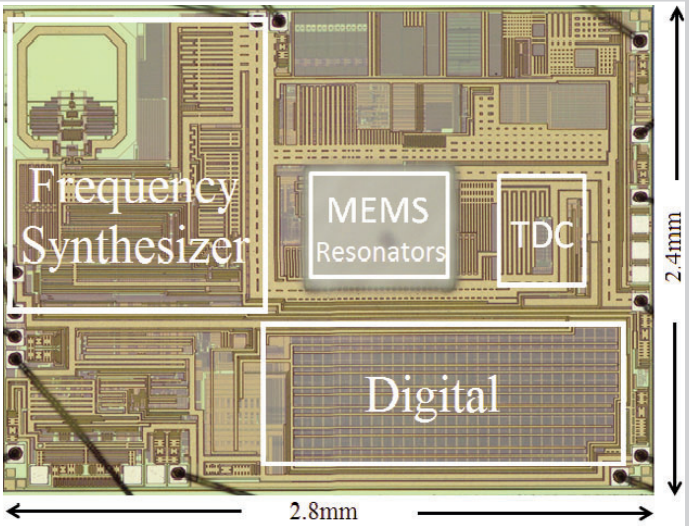

Figure 11.1.7: Micrograph of the 0.18µm CMOS die with the flipped MEMS die of the resonators at the top.

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