A 3 ppm 1.5 × 0.8 mm² 1.0 µA 32.768 kHz MEMS-Based Oscillator

Samira Zaliasl, *Member, IEEE*, Jim C. Salvia, *Member, IEEE*, Ginel C. Hill, Lijun (Will) Chen, Kimo Joo, Rajkumar Palwai, *Member, IEEE*, Niveditha Arumugam, Meghan Phadke, Shouvik Mukherjee, Hae-Chang Lee, Charles Grosjean, Paul M. Hagelin, Sudhakar Pamarti, *Member, IEEE*, Terri S. Fiez, *Fellow, IEEE*, Kofi A. A. Makinwa, *Fellow, IEEE*, Aaron Partridge, *Member, IEEE*, and Vinod Menon

***Abstract*—This paper describes the first 32 kHz low-power MEMS-based oscillator in production. The primary goal is to provide a small form-factor oscillator (1.5 × 0.8 mm²) for use as a crystal replacement in space-constrained mobile devices. The oscillator generates an output frequency of 32.768 kHz and its binary divisors down to 1 Hz. The frequency stability over the industrial temperature range (–40 °C to 85 °C) is ±100 ppm as an oscillator (XO) or ±3 ppm with optional calibration as a temperature compensated oscillator (TCXO). Supply currents are 0.9 µA for the XO and 1.0 µA for the TCXO at supply voltages from 1.4 V to 4.5 V. The MEMS resonator is a capacitively-transduced tuning fork at 524 kHz. The circuitry is fabricated in 180 nm CMOS and includes low power sustaining circuit, fractional-N PLL, temperature sensor, digital control, and low swing driver.**

***Index Terms*—Low power design, MEMS oscillator, MEMS resonator, real time clock, sub-threshold, 32 kHz oscillator, 32 kHz XO and TCXO.**

I. Introduction

TIMEKEEPING and low power functions are commonly maintained by low-frequency oscillators, historically 32.768 kHz (2^{15} Hz). Applications include timing, smart metering, power conservative clocking, and sensor interfaces. In mobile and other battery powered devices, 32 kHz oscillators are also employed in duty-cycling high power circuitry to prolong battery life. Key specifications for this clock are frequency accuracy, PCB area and power consumption. Moderate precision applications use quartz tuning fork crystals (X), or oscillators (XO) [1], while high precision applications use temperature compensated tuning fork oscillators (TCXO). For timekeeping application, 32 kHz quartz tuning fork crystals and oscillators are the most common [2]. They have a room-temperature accuracy of ±20 ppm and show a downward parabolic frequency curve of ∼0.035 ppm/C², which causes a frequency error of about −150 ppm at low and high temperature extremes [3], [4]. Smart metering and other precision applications require more accurate reference clocks which can be provided by temperature compensated tuning fork oscillators trimmed to maintain ±5 ppm accuracy over temperature [5]–[7].

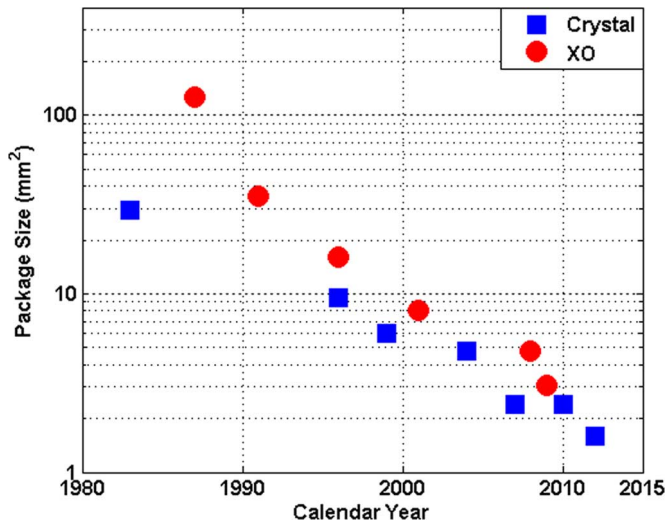

Fig. 1. Progress in size reduction of 32 kHz X and XOs.

Tuning fork oscillators are available in 3.2×1.5 mm² surface mount ceramic packages, while TCXOs are larger, commonly constructed with tuning fork crystals embedded in leaded plastic packages. Fig. 1 shows the size reduction of 32 kHz quartz oscillators over the past three decades [8]. Their rate of size reduction is likely slowing due to scaling limitations and packaging/assembling difficulties [9]. However, the growth in portable devices is increasing the demand for smaller footprint clock references.

Power consumption is commonly specified as ∼1 µA supply current across voltages from 1.5 V to 5 V. In applications with small batteries, such as wrist watches, the current consumption can be as low as ∼0.2 µA, and in TCXOs the consumption is commonly ∼3 µA.

In the past decade, several high frequency MEMS-based oscillators (both XOs and TCXOs) have been introduced [10]. They have been shown to match or outperform their quartz crystal counterparts. This has been enabled by the development of long-term stable MEMS resonators and temperature compensation circuit architectures [11]. Low-frequency MEMS

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S. Zaliasl, G. C. Hill, L. Chen, K. Joo, R. Palwai, N. Arumugam, M. Phadke, S. Mukherjee, H.-C. Lee, C. Grosjean, P. M. Hagelin, A. Partridge, and V. Menon are with SiTime Corporation, Sunnyvale, CA 94085 USA.

J. C. Salvia is with InvenSense, Sunnyvale, CA 95110 USA.

S. Pamarti is with the Department of Electrical Engineering, University of California, Los Angeles, CA 90095 USA.

T. S. Fiez is with Department of Electrical Engineering, Oregon State University, Corvallis, OR 97331 USA.

K. A. A. Makinwa is with Department of Electrical Engineering, Delft University of Technology, 2628 CN Delft, The Netherlands.

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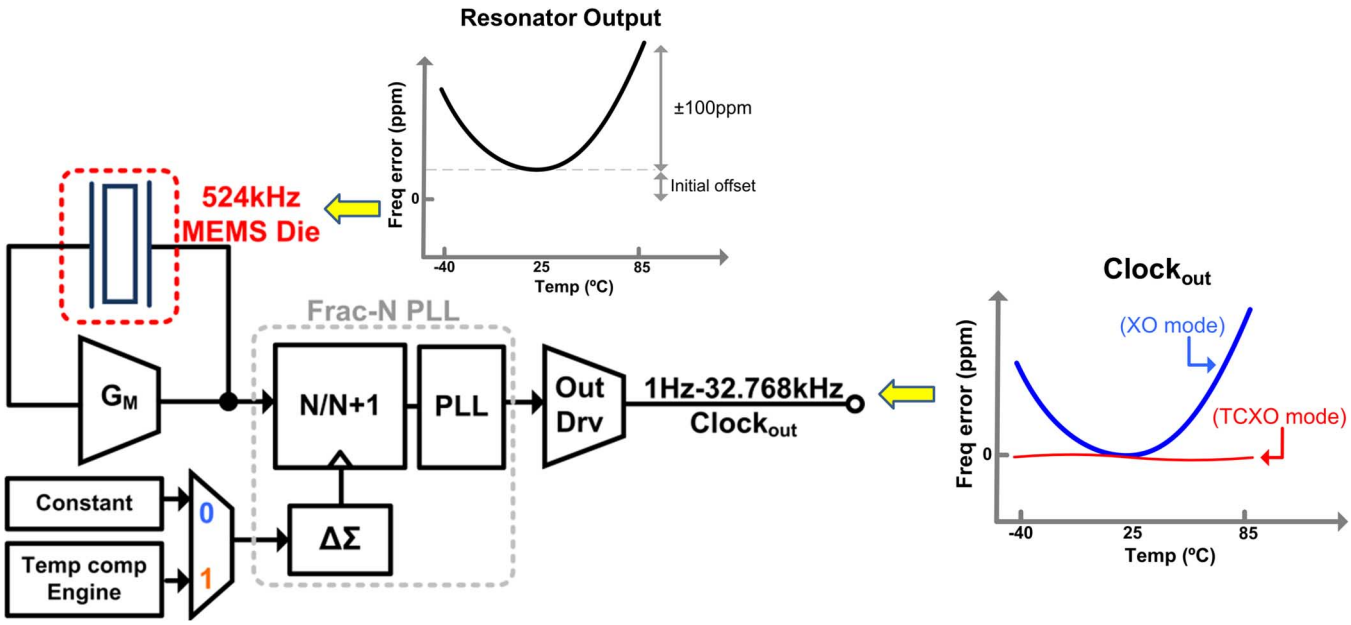

Fig. 2. Block diagram of the MEMS-based 32 kHz clock generator.

oscillators have been shown in academic work for two decades but none have been commercially introduced [12], [13].

This paper describes the smallest production 32 kHz XO and TCXO [14]. The XO combines a temperature stable MEMS resonator with sustaining amplifier and fractional-N PLL to calibrate the output frequency over production tolerances. When configured and calibrated as a TCXO, a temperature-to-digital converter (TDC) adjusts the frac-N to compensate frequency over temperature. The oscillator can be configured as a ± 100 ppm XO or with temperature compensation as a ± 3 ppm TCXO. Package size is 1.5×0.8 mm^2. Supply current is 0.9 μA for the XO and 1.0 μA for the TCXO at supply voltages from 1.4 V to 4.5 V.

Section II describes the architecture. Details of the circuit design of each block in this system, including the description of the key techniques to improve their performance, are presented in Section III. Measured results from the described oscillator are shown in Section IV, followed by conclusions in Section V.

II. System Level Design

The design of a sub-μA MEMS-based oscillator presents two primary challenges: (a) initial frequency offset due to process variations in the fabrication of the MEMS resonator, and (b) temperature sensitivity of the resonator. As shown in Fig. 2, the resonator employed in this work has a nominal frequency of 524 kHz that varies up to 2% over production tolerances and frequency stability of ± 100 ppm over a $-40\,^{\circ}$C to $85\,^{\circ}$C temperature range. The initial frequency offset must be corrected, while the frequency stability is sufficient for XO operation. For TCXO operation the temperature sensitivity of the resonator must be compensated. Since the initial frequency offset is too large to be corrected by pulling the resonator, a delta-sigma fractional-N phase locked loop is employed, as shown in Fig. 2.

The MEMS sustaining amplifier provides a 524 kHz reference clock. This reference is divided down to 32.768 kHz using a multi-modulus divider controlled by a digital delta-sigma modulator and fed to an integer-N PLL as shown in Fig. 2. In XO mode, the target frequency of 32.768 kHz is achieved by appropriately setting the fractional value of the digital delta-sigma modulator at factory calibration. In TCXO mode, the value of the modulator is continuously updated to compensate for temperature variation. Temperature calibration data is obtained in factory measurements. The integer-N PLL filters the quantization noise from the digital delta-sigma modulator. In a low-power XO mode, current consumption can be further reduced by bypassing the integer-N PLL. This delivers a high jitter clock, but for applications that only count time the noise is negligible. A final programmable divider can optionally reduce the frequency in powers of two to 1 Hz.

III. Circuit Level Implementation

A. MEMS Resonator and Sustaining Oscillator

The reference clock for this system is generated from a 524 kHz silicon MEMS resonator. The resonator is an H-style capacitively-transduced tuning-fork, shown in Fig. 3(a), with a nominal quality factor of 52,000. When a bias voltage of 2.4 V is applied between the tuning fork tines and the drive/sense electrodes shown in Fig. 3(b), the resonator presents an effective impedance between the drive and sense electrodes that is well-modeled as a series connection of a 70 aF capacitance (C_M), a 1.4 kH inductance (L_M), and a 90 kΩ resistor (R_M), as shown in Fig. 3(c) [16]. The frequency variation of this resonator is less than ± 100 ppm over the temperature range -40°C to $+85^{\circ}$C, which is 20$\times$ less variation than earlier commercial MEMS resonators [16] and less than earlier temperature-compensated MEMS resonators [17]–[19].

The oscillator circuit that drives the MEMS resonator is shown in Fig. 4. The architecture is a modified version of previously published Pierce configurations [20], [21]. A

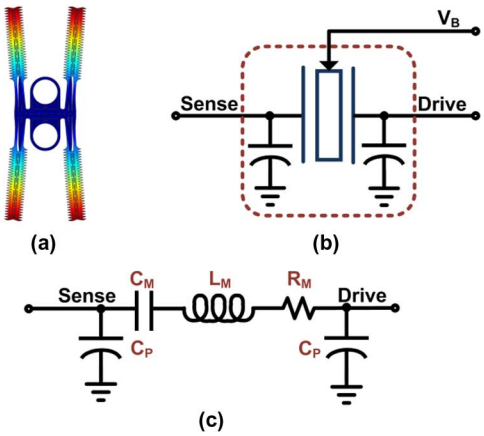

Fig. 3. (a) Tuning H-style fork 524 kHz MEMS resonator, (b) simplified block diagram, and (c) electrical model of the resonator.

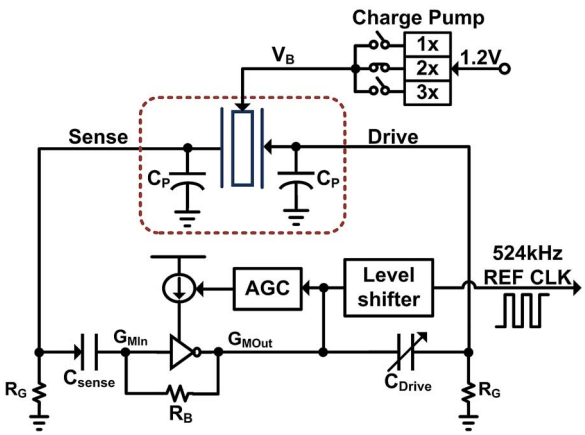

Fig. 4. Simplified block diagram of sustaining circuit.

current-starved inverter with gain control provides transconductance gain (G_M) to initiate and sustain oscillation. This element is connected to the MEMS resonator via on-chip coupling capacitors, C_{Drive} and C_{Sense}, which allows the DC biases of the resonator drive and sense terminals to be set by on-chip resistors R_G to ground. This guarantees that the effective MEMS bias voltage is determined by the voltage applied to the tuning fork tines and is not influenced by the G_M stage's DC operating point. Resistors R_G, together with the capacitive networks at the oscillator terminals, form high pass filters with corner frequencies well below the oscillation frequency. Before reaching the resonator, the AC output of the G_M stage is attenuated by the capacitive divider between C_{Drive} and C_P, where C_P is the parasitic capacitance on the resonator drive electrode. A trimmable C_{Drive} allows for adjustment of this capacitive divider, thereby enabling the power delivered to the resonator to be trimmed. While this divider might appear to lower the oscillator's loop gain, this effect is largely compensated by the gain of the G_M stage, $G_M(1/C_{Drive} + 1/C_P)$, which is inversely proportional to the series connection of C_{Drive} and C_P and therefore increases as the attenuation increase.

An automatic gain control circuit (AGC) controls the bias current of the G_M stage in order to maintain fixed AC voltage amplitude at the G_M stage's output. A simplified diagram of

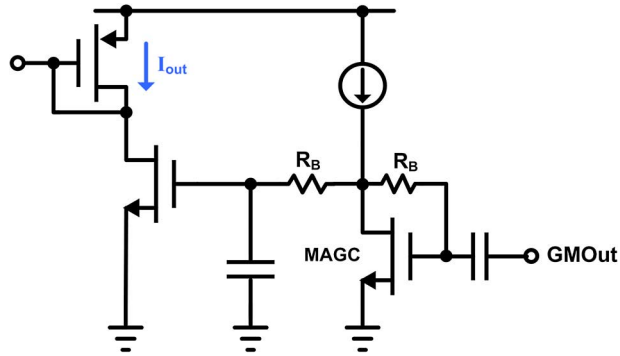

Fig. 5. Automatic gain control circuit.

the AGC is shown in Fig. 5. As described in [21], the nonlinear characteristics of device M_{AGC} ensure that an increase in the amplitude of the AC waveform at G_{MOut} results in a decrease in the DC voltage at the gate of M_{AGC}. A filtered version of this gate voltage is used to generate the bias current for the G_M stage, thereby providing negative feedback to control the amplitude of the system's oscillations. Resistive elements R_B in the G_M and AGC stages are implemented using sub-threshold MOS devices biased in the linear region. Extensive use of AC coupling makes the oscillator insensitive to the dynamic offset effects that can be produced by the nonlinear behavior of these sub-threshold MOS devices, even when signal swings exceed several thermal voltages. An AC-coupled level shifter is used to transform the small-amplitude sine wave at G_{MOut} into a rail-to-rail square wave, thereby providing a 524 kHz digital reference clock.

The resonator's motional resistance, R_M, is inversely proportional to the square of the resonator's bias voltage ($R_M \propto (1/V_B^2)$), and the transconductance required to sustain oscillations ($G_{M,MIN}$) is proportional to R_M:

$$G_{M,MIN} = R_M \omega_0^2 \frac{(C_1C_2 + C_2C_3 + C_1C_3)^2}{C_1C_2}$$

where ω_0 is the resonator's resonant frequency, and C_1, C_2, C_3 represent the capacitance from resonator sense electrode to ground, from resonator drive electrode to ground, and from resonator drive electrode to sense electrode, respectively [20]. As a result, increasing resonator bias voltage generally results in lower oscillator power consumption. To this end, the MEMS bias voltage is supplied from a programmable charge pump that can output integer multiples of a 1.2 V reference voltage, up to 3.6 V. However, resonator mechanical displacement also increases with bias voltage, and this displacement must be limited to avoid unwanted nonlinear effects [22]. The sensitivity of resonant frequency to variation in the bias voltage also increases with bias voltage. Consequently, although the oscillator power consumption is minimized when the charge pump output is 3.6 V, it was experimentally determined that 2.4 V bias provided better system-level performance for TCXO applications. Under this condition, the total current consumption of the MEMS sustaining circuit and charge pump is 240 nA.

B. Fractional-N PLL

Fig. 6 shows the detailed block diagram of the fractional-N PLL and temperature compensation path. This fractional-N PLL

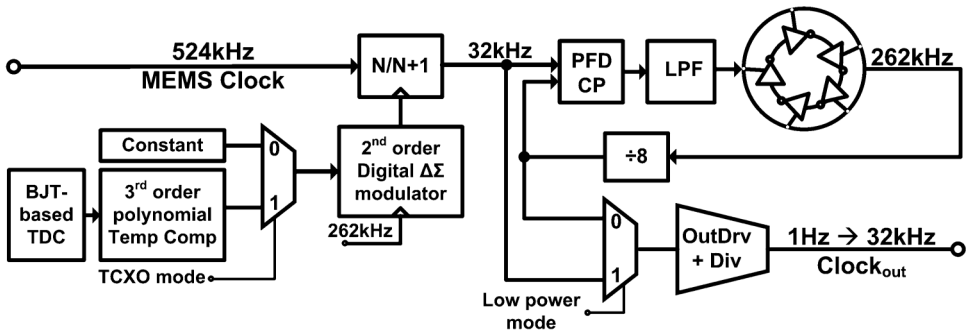

Fig. 6. Block diagram of PLL and its different configurations in XO, TCXO and low power mode.

is a variant of the classical delta-sigma fractional-N PLL [23]. Two specific differences can be noted. First, the multi-modulus frequency division (under the control of a digital delta-sigma modulator) is performed not in the PLL feedback path but in a pre-driver in the reference path. Second, the output is tapped from the integer divider in the feedback path rather than from the VCO itself.

Performing the fractional division in the reference path means that the pre-divider output is 32.768 kHz. This allows disabling and bypassing the PLL in the XO mode in order to reduce current consumption below 0.9 μA. Although the output of this pre-divider is already at the target frequency, it carries the quantization noise from $\Delta\Sigma$ modulator. This introduces output jitter, but it is not detrimental in applications that count pulses, e.g. 32,768 pulses to define one second. In applications where the jitter needs to be low, the integer-N PLL filters this noise. A 2nd order digital delta-sigma modulator provides optimum performance to power: a 1st order modulator would exhibit strong limit cycle behavior, whereas a 3rd order modulator would consume unnecessary current. The power consumption of the digital delta-sigma modulator is kept low by adopting a low supply voltage that is sufficient for reliable operation. Section III-E describes the voltage regulators.

As shown in Fig. 6, the integer-N PLL is a standard charge-pump based type II PLL [24] optimized for low power consumption. It has a phase frequency detector (PFD) and a 16 nA charge pump. The loop filter sets the loop bandwidth to 1 kHz to minimize the overall noise from the VCO and digital $\Delta\Sigma$ modulator. The VCO is a current-starved ring oscillator with a nominal frequency of 262 kHz. The total current consumption of the PLL including pre-divider is 290 nA.

C. Temperature to Digital Converter (TDC)

To achieve TCXO stability, a BJT-based temperature sensor is combined into a switched capacitor delta-sigma modular as shown in Fig. 7(a). BJT-based sensors are known to achieve the best combination of accuracy and energy efficiency [25]. It is also known that switched capacitor delta-sigma modulators offer high resolution at low power, particularly for low bandwidth applications such as tracking temperature changes.

The BJT-based sensor's block diagram is shown in Fig. 7(a). As shown, two identical NPNs are biased at a collector current ratio of $p = 6$. The resulting base-emitter voltage, $\mathrm{V_{BE}}$, has a negative temperature coefficient of approximately $-2\ \mathrm{mV/^{\circ}C}$. The difference between their base-emitter voltages is proportional-to-absolute temperature (PTAT), i.e. $\Delta\mathrm{V_{BE}} = \mathrm{V_{BE2}} - \mathrm{V_{BE1}} = (\mathrm{kT/q}) \cdot \ln(\mathrm{p})$ where k is Boltzmann constant, q is charge, and T is the absolute temperature, with unit of Kelvin. Rather than the more commonly used PNPs, NPNs were used in this design because of their higher current gain [26]. The temperature to digital converter (TDC) generates a digital bitstream, whose average value is proportional to $(\alpha\Delta\mathrm{V_{BE}})/\mathrm{V_{BG}}$, where $\alpha = 14$ and $\mathrm{V_{BG}} = \mathrm{V_{BE1}} + \alpha\Delta\mathrm{V_{BE}}$ is a voltage with a slightly positive temperature dependence, which improves the sensor's overall linearity [27]. The TDC is based on a 2nd-order switched-capacitor (SC) $\Delta\Sigma$ modulator. As shown in Fig. 7(a), its main components are two SC integrators and a 1-bit quantizer. Both integrators are based on folded-cascode OTAs, with the first OTA gain-boosted to improve its DC gain. Depending on the quantizer's output $(\mathrm{bit_{out}})$, the modulator's next input is either $-\mathrm{V_{BE1}}$ $(\mathrm{bit_{out}} = 1)$ or $\alpha\Delta\mathrm{V_{BE}}$ $(\mathrm{bit_{out}} = 0)$ [27]. This charge-balancing scheme ensures that the average value of $\mathrm{bit_{out}}$ is equal to the desired ratio $(\alpha\Delta\mathrm{V_{BE}})/(\mathrm{V_{BE}}+\alpha\Delta\mathrm{V_{BE}})$. $\Delta\mathrm{V_{BE}}$ is integrated over α clock cycles and then sampled exclusively [28]. This technique only have one unit sampling capacitor $(\mathrm{C_s})$ which avoids the extra area and mismatch errors associated with implementing α with multiple sampling capacitors, and also ensures that the first integrator's closed-loop gain is fixed, irrespective of the modulator's state. As shown, $-\mathrm{V_{BE}}$ is integrated during a single clock cycle, while $\Delta\mathrm{V_{BE}}$ is integrated over α clock cycles. In other words, each $\Delta\Sigma$ cycle takes either 1 or α clock cycles, when $\mathrm{bit_{out}}$ is 1 or 0, respectively.

Several dynamic techniques are used to improve the TDC's accuracy. The sensor front-end's current sources are dynamically matched to mitigate their mismatch, while the first integrator's offset and flicker noise are mitigated by employing correlated double sampling (CDS) [29]. To mitigate charge injection errors, the 1st integrator employs a fully differential structure using minimum size switches. Any residual offset is then removed by system-level chopping, at the expense of a doubled conversion time [30]. To provide a differential input to the first integrator, the positions of the current sources are swapped during the two phases of each $\Delta\Sigma$ clock cycle. This simultaneously averages out the mismatch between the two BJTs [27]. Applying dynamic element matching (DEM) technique to the front-end's current sources improves their matching, but since the modulator's input then changes over multiple $\Delta\Sigma$ clock cycles, it could also fold quantization-noise back into the signal

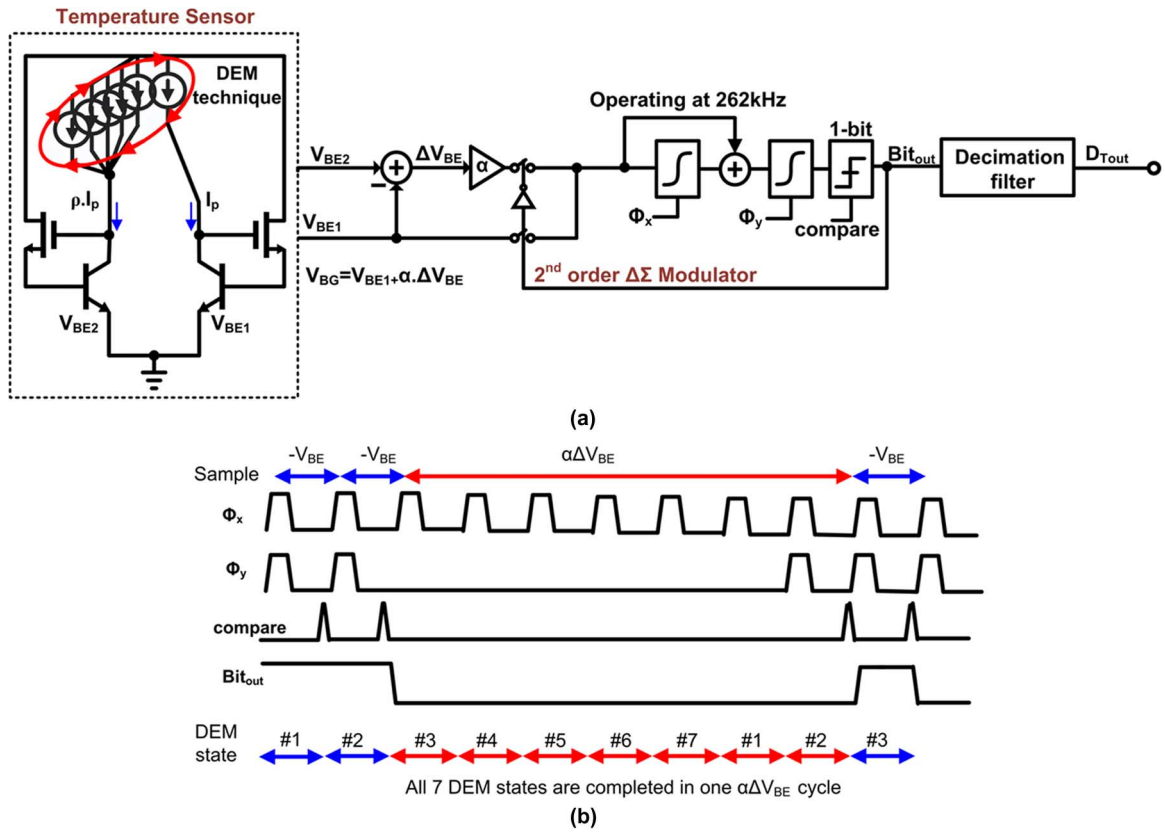

Fig. 7. (a) Block diagram of the temperature sensor. (b) The timing diagram of the proposed DEM algorithm.

band [31]. This could significantly impact the signal-to-noise ratio. Previous work mitigated this effect by randomization [32] or by the use of bitstream-controlled DEM [33]. We addressed this problem with the DEM principle illustrated in Fig. 7(b). Since a complete DEM cycle requires $(\rho + 1)$ clock cycles, it can be combined with the α clock cycles required to integrate ΔV_{BE}. By choosing $\alpha = n.(\rho + 1)$, where $n = 1, 2, 3, \ldots$, a full DEM cycle can be completed during exactly one $\Delta\Sigma$ cycle, thus avoiding any quantization-noise fold-back.

The total current consumption of the implemented TDC is 4.5 μA operating at a 262 kHz sampling clock. Of the total current consumption, 1.5 μA is consumed by the front-end, 1.7 μA is dissipated by the loop filter and 0.8 μA is used by the decimation filter, the digital filter, and the clock generator. System-level chopping requires two TDC conversions, which doubles the conversion time to 6 ms at room temperature. The TDC achieves a resolution of 25 mK (rms), which leads to a figure of merit $(\text{Energy}/\text{Conversion} \times \text{Resolution}^2)$ of 24 pJ °C^2 [25]. This compares favorably with the state of the art [34].

To meet the 1 μA total-current-consumption target, the TDC is duty-cycled to reduce its average current consumption. However, the use of duty-cycling leads to a trade-off between temperature tracking accuracy and power consumption. Applications require a frequency error of <1 ppm in the presence of temperature ramps of ± 1°C/sec. To meet this, the TDC's update rate is set to 3 Samples/sec. This results in an average current of 105 nA.

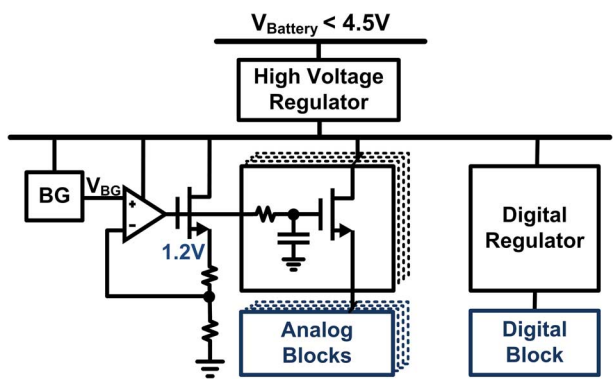

Fig. 8. Block diagram of voltage regulators. Analog regulator adopts open loop architecture.

D. Voltage Regulators

A significant fraction of the chip's total current consumption and area is dedicated to voltage regulation, which is important for three reasons. First, to meet the TCXO frequency stability specifications, the performance of the analog blocks must be preserved over a wide range of external supply voltages and supply ripple. In particular, the MEMS oscillation frequency is function of bias voltage and drive amplitude, so these must be regulated in the presence of supply variations or noise. Second, digital power consumption can be reduced by operating digital circuits at the minimum voltage required to meet all timing constraints. Third, some applications benefit from

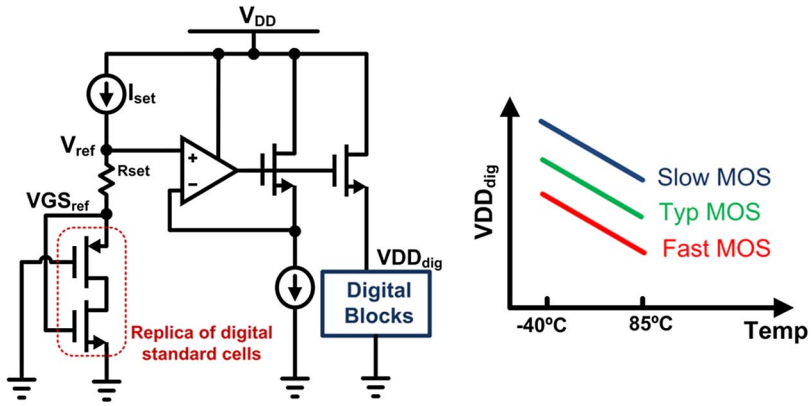

Fig. 9. Digital voltage regulator biases digital block with a minimum required supply over process and temperature corners.

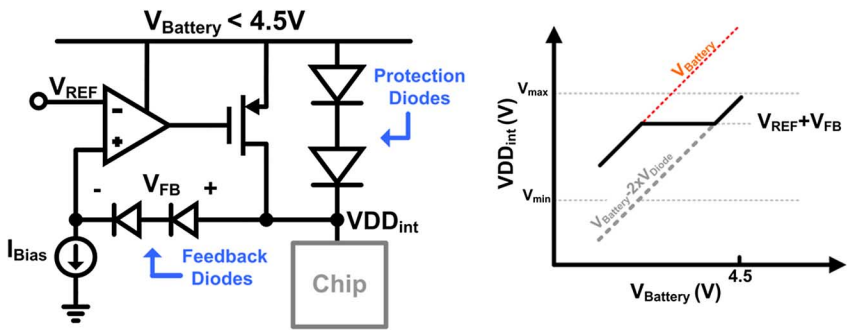

Fig. 10. Low-power high-voltage regulator.

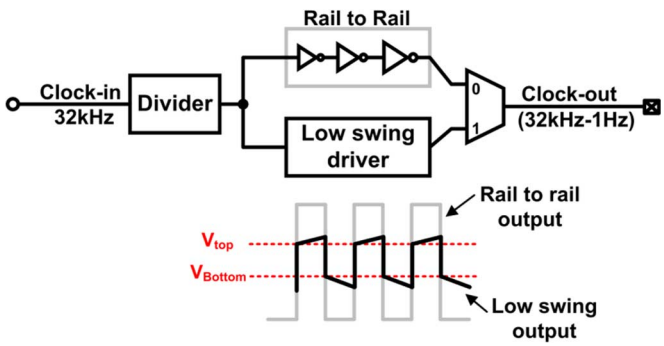

Fig. 11. Block diagram of output driver. Low-swing driver feature to reduce power.

powering the 32 kHz timing reference directly from an unregulated battery in order to reduce current consumption in standby mode. For these applications, a low power high voltage regulator has been included in the design to extend the supply range to 4.5 V without requiring external components or high-voltage fabrication process options. Fig. 8 shows a block diagram of the employed voltage regulation scheme. The components are described in detail below.

Bias Generation and Voltage Regulation for Analog Blocks: A bandgap voltage serves as the reference for a programmable closed-loop master analog voltage regulator as shown in Fig. 8. The 1.2 V output of this master regulator is replicated by open-loop slave stages, which provide stable independent power supplies for all remaining analog blocks on the chip. Separate power domains are important for isolating sensitive circuits from noisy ones (e.g. the highly duty-cycled TDC) and for reducing cross-talk between different clock domains. The open-loop slave architecture provides power savings compared to separate closed-loop regulators, since each slave stage maintains unconditional stability and consumes zero current. The bandgap reference and master/slave regulators consume 230 nA and enable the system to achieve supply sensitivity less than ± 0.25 ppm/V.

Voltage Regulator for Digital Block: The digital regulator uses a replica biasing architecture to minimize digital power consumption while guaranteeing timing closure over process and temperature variations. The replica structure in Fig. 9 consists of a series stack of NMOS and PMOS which match the devices used in the digital standard cells. Driving a constant current $\mathrm{I_{set}}$ into this series stack generates a voltage $\mathrm{VGS_{ref}}$, which varies inversely with MOS process and temperature as shown in Fig. 9. Using $\mathrm{VGS_{ref}}$ as the supply level for digital gates that match the replica transistors therefore guarantees that those gates have a minimum current drive capability of $\mathrm{I_{set}}$. A programmable resistor $\mathrm{R_{set}}$ is used to add margin $\mathrm{I_{set}} \times \mathrm{R_{set}}$ (maximum 100 mV) to the digital supply to ensure this minimum current drive capability even in the presence of threshold mismatch or supply droop. This master/slave architecture similar to that used in the analog regulators supplies the digital blocks with $\mathrm{VDD_{dig}} \approx \mathrm{VGS_{ref}} + \mathrm{I_{set}} \times \mathrm{R_{set}}$. This scheme guarantees the digital regulator's stability, even in the presence of the large supply current variations that result from duty-cycling the TDC and temperature compensation engine.

High Voltage Regulator: Operating directly from an unregulated 4.5 V supply, such as a battery, requires special

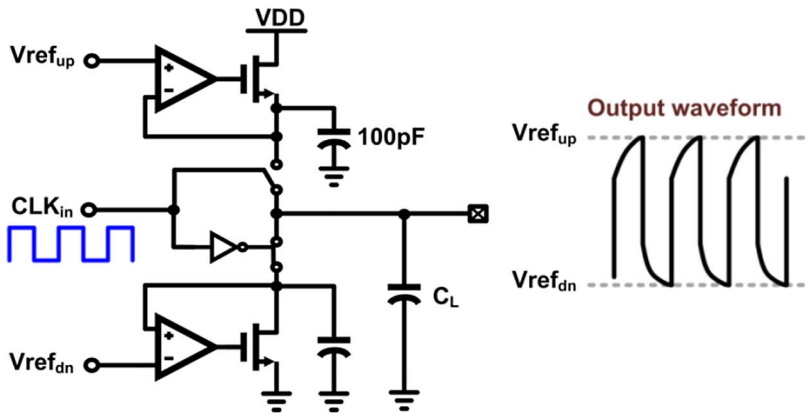

Fig. 12. Circuit implementation of low-swing driver. Full control on output swing by programming the regulator reference.

consideration to prevent over-voltage stress of the thick oxide devices in this 180 nm process, which have a maximum operating voltage of 3.63 V. A simple means of providing over-voltage protection would be to add two diodes in series with supply $\mathrm{V_{Battery}}$, thereby dropping the internal supply voltage ($\mathrm{VDD_{int}}$) to $\mathrm{V_{Battery}} - 2\mathrm{V_{Diode}}$, where $\mathrm{V_{Diode}}$ is the voltage drop across one of the protection diodes. Unfortunately, this solution places severe limits on the *minimum* external supply voltage required to maintain $\mathrm{VDD_{int}} > 1.2$ V, especially considering that the voltage drop across these diodes can vary dramatically with process, temperature, and supply current. To solve this problem, a regulator in parallel with two series protection diodes is employed, as shown in Fig. 10. In this circuit, when $\mathrm{V_{Battery}}$ is high, the two protection diodes conduct and $\mathrm{VDD_{int}} = \mathrm{V_{Battery}} - 2\ \mathrm{V_{Diode}}$. At intermediate voltages, the regulator partially bypasses the protection diodes and maintains $\mathrm{VDD_{int}} = \mathrm{V_{REF}} + \mathrm{V_{FB}}$, where $\mathrm{V_{REF}}$ is a 1.2 V reference provided by internal regulators and $\mathrm{V_{FB}}$ is the voltage drop across the feedback diodes biased with 8 nA current shown in Fig. 10. When $\mathrm{V_{Battery}}$ drops below $\mathrm{V_{REF}} + \mathrm{V_{FB}}$, the regulator simply acts as a switch shorting $\mathrm{VDD_{int}}$ to $\mathrm{V_{Battery}}$.

E. Drivers

There are two options for the output driver: a rail-to-rail CMOS and a low swing driver. With a low-swing driver, the CVF current can be reduced by $\mathrm{V_{swing}}/\mathrm{V_{DD}}$. In most applications, the following block driven by this oscillator does not require full swing input. As shown in Fig. 11, as long as the output clock waveform crosses the two defined thresholds of $\mathrm{V_{top}}$ and $\mathrm{V_{bottom}}$ it is suitable for the application. As shown in Fig. 12, in this design the driver has two regulators which together control its output swing. CMOS transmission gates are used to alternate between independently programmable $\mathrm{Vref_{up}}$ and $\mathrm{Vref_{dn}}$ giving control on the swing of the output clock. Capacitive charge sharing generates fast output transitions followed by slow single pole settling from the regulators. The total power consumption of each regulator is 60 nA.

To further reduce the output driver power consumption, the output frequency can be divided down to 1 Hz in powers of 2. Fig. 13 demonstrates a quantitative comparison between the full and low-swing driver current consumption versus capacitor load. The external VDD is set to 1.8 V, which limits the rail-to-rail driver to a 1.8 V output swing. For the low-swing driver, the output swing is set to 0.6 V. As shown, the low-swing driver reduces the total power consumption by 55% for a load capacitor of 15 pF.

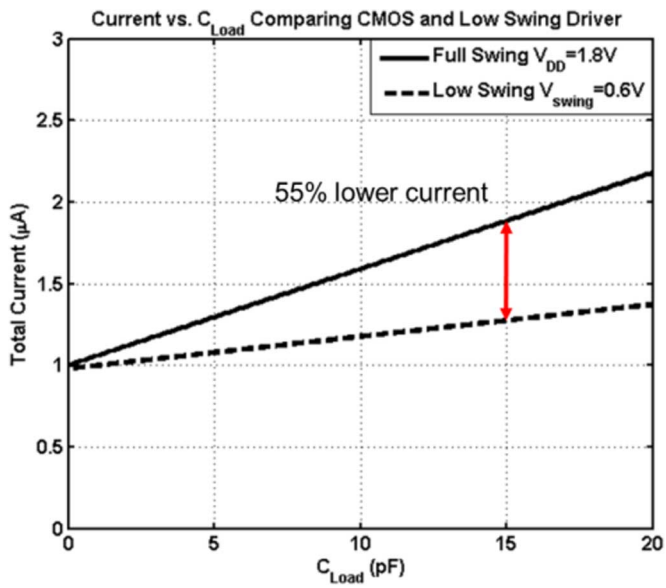

Fig. 13. Current consumption vs. load capacitor using CMOS and low swing driver.

IV. Measurement Results

Fig. 14(a) shows the 180 nm CMOS die with area of 1.2 mm^2, and the MEMS die with area of 0.17 mm^2. On the CMOS chip, the PLL, TDC, and OSC consume 0.3 mm^2 and the digital including 3rd order polynomial correction occupies 0.5 mm^2. The oscillator can be assembled in conventional wire-bonded plastic packages where the 524 kHz MEMS resonator is attached and wire-bonded to a programmable MEMS oscillator system to fit in a 2×1.2 mm^2 QFN package. To reduce the size further, the MEMS resonator can be flipped-chip bonded to the CMOS die in a 1.55 mm×0.85 mm chip-scale package (CSP), as shown

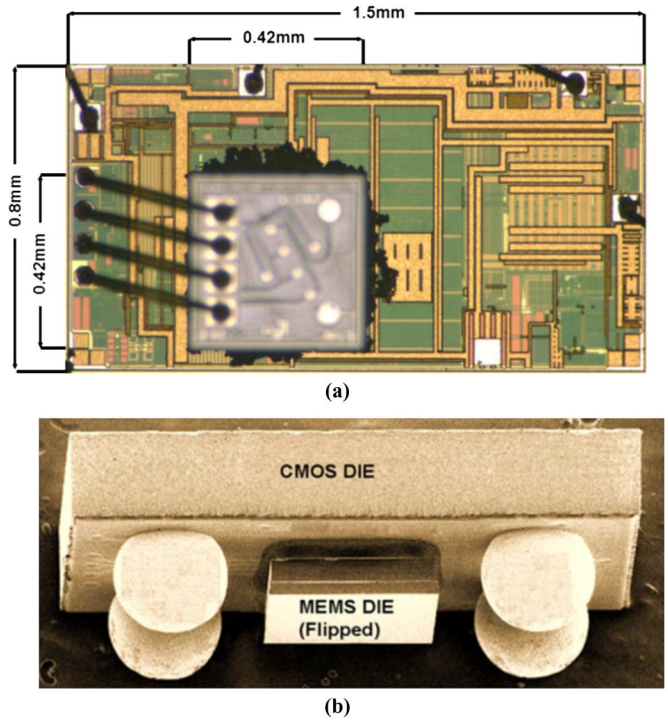

Fig. 14. Die photograph of 524 kHz MEMS die and a 180 nm CMOS chip in (a) QFN wire-bonded and (b) chip scale packages.

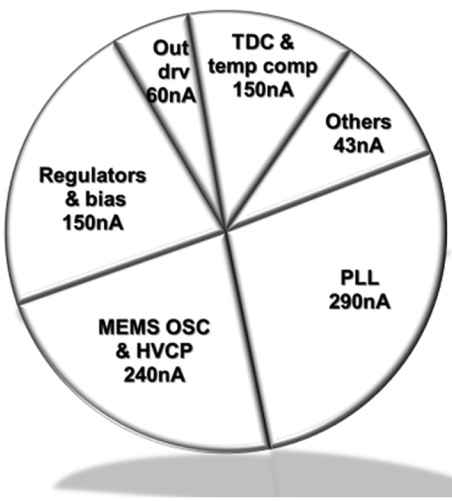

Fig. 15. The current consumption of each main block in the system.

in Fig. 14(b). In this packaging, epoxy under-fill is applied between two dies to fully insulate the MEMS-CMOS interconnections, leaving the complete package fully compatible with standard lead-free PCB assembly processes.

With a 3.3 V supply voltage, the measured average current of the chip is 1.0 μA with 32 kHz output under no external load condition. In the low-power XO mode, with the PLL disabled, a current consumption reduces to 0.6 μA. Fig. 15 shows a breakdown of the TCXO mode power consumption. SPICE-level simulation estimates that the oscillator (including charge pump) consumes 240 nA, the PLL (including delta-sigma modulator) consumes 290 nA, and the temperature sensor (including temperature compensation engine) consumes 150 nA. All the

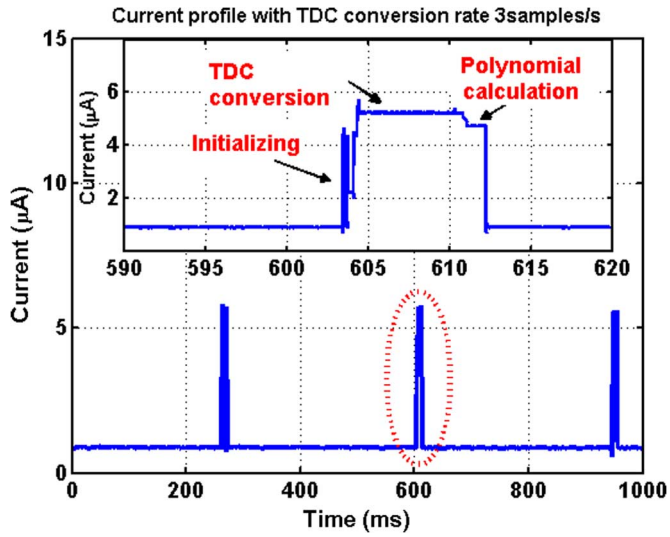

Fig. 16. Transient current profile of entire chip when TDC conversion rate is 3 Samples/sec.

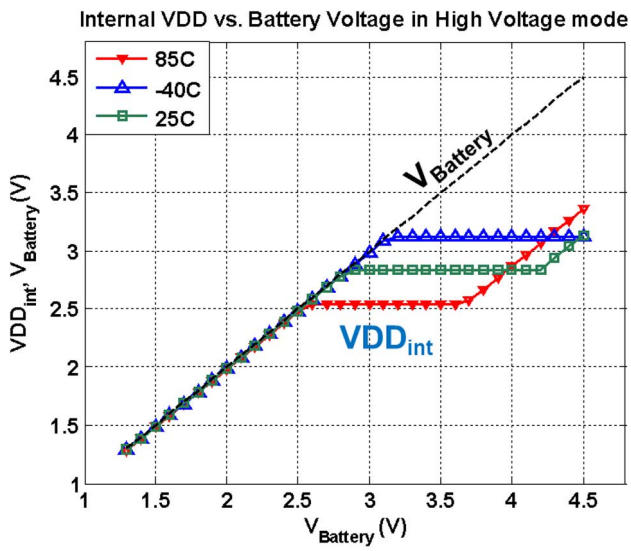

Fig. 17. Measured $\mathrm{VDD_{int}}$ versus $\mathrm{V_{Battery}}$ when high voltage regulator is enabled.

currents reported are with the internal supply voltages of the blocks set to 1.2–1.4 V. Fig. 16 displays the transient current profile with a peak value of 5.5 μA. The TDC conversion rate is set to 3 samples/sec. After each conversion, TDC and compensation engine sleep while a low power wake-up circuitry runs to turn on TDC every 330 mS. In each conversion, it takes 1 ms for the BJT core and modulator to initialize, 6 ms for two back-to-back conversions at 25 °C, and 2 ms to evaluate the polynomial.

Fig. 17 shows the measured $\mathrm{VDD_{int}}$ versus $\mathrm{V_{Battery}}$ when high voltage regulator is enabled. As shown, with this regulator, the internal voltage safely lands between 1.5 V and 3.63 V when $\mathrm{V_{Battery}}$ varies from between 1.5 V to 4.5 V.

Shown in Fig. 18(a), measured frequency stability over temperature of -40°C to $+85^{\circ}$C is better than $\pm$100 ppm for 28,000 XO devices. With only room temperature calibration, the initial accuracy of the XO devices is within $\pm$3 ppm. With temperature

TABLE I
PERFORMANCE SUMMARY OF XO AND TCXO DEVICES AND COMPARISON TABLE

	XO			TCXO			
Parameter	This work	Epson SG-3050	Micro crystal OV-7604	This work	Maxim DS32kHz	Epson TG-3530	Kyocera KT3225T
Supply Voltage (V)	1.2 to 4.5	1.2 to 5.5	1.2 to 5.5	1.5 to 4.5	2.7 to 3.5	2.2 to 5.5	2 to 5.5
Temperature Range (°C)	-40 to 85	-20 to 70	-40 to 85	-40 to 85	-40 to 85	-20 to 70	-40 to 85
Frequency Stability vs. Temp (ppm)	100 max	120 max	160 max	± 3	± 7.5	± 5	± 5
Supply Sensitivity (ppm/V)	± 0.25	± 3	± 1.5	± 0.25	2.5	± 1	± 1
OSC Start up (s)	0.2	1	0.5	0.2	1	3	3
Current (µA) Clock enabled, no load	0.9 typ 1.4 max 0.6 LPM	- typ 2 max	0.4 typ 0.6 max	1 typ 1.5 max	1.85 typ 4 max	1.7 typ 4 max	1.5 typ 4 max
Package Size (mmxmm)	1.55x0.85	2.2x1.4	3.2x1.5	1.55x0.85	18.5x6.35	5x10.1	3.2x2.5

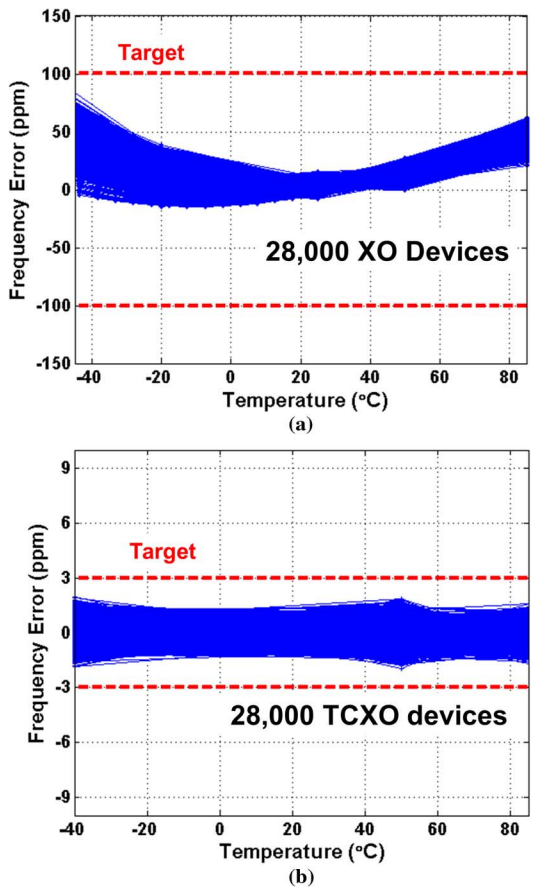

Fig. 18. Frequency stability in (a) XO and (b) TCXO configurations.

compensation enabled (TCXO mode), the measured frequency accuracy improved to ±3 ppm for 28,000 TCXO devices as displayed in Fig. 18(b). These devices are trimmed individually at five temperature points on wafer level. The reader may wonder with individual trimming process all techniques such as DEM, CDS in temperature sensor were not necessary. However, these

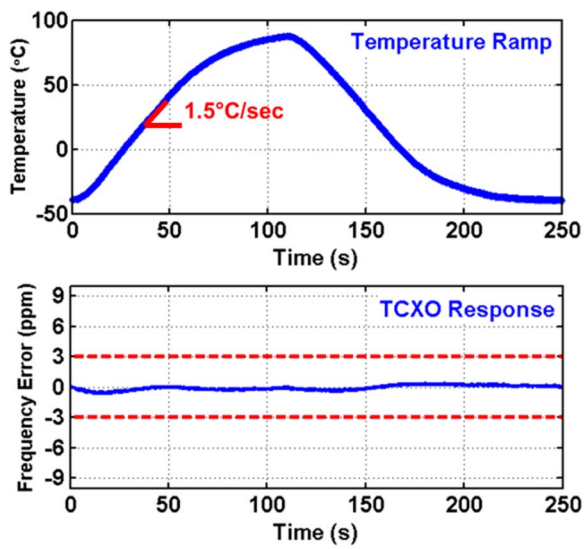

Fig. 19. TCXO response to temperature ramp.

techniques are implemented to reduce stress sensitivity. As a result, solder down shift is limited to be less than ±1.5 ppm over temperature range of −40°C to 85°C. Fig. 19 shows the temperature tracking performance of TCXO device: a temperature transient as fast as 1.5°C/sec is applied and measured normalized frequency error is plotted. An evident from the figure, temperature compensation with TDC conversion rate of 3 Samples/sec is able to correct frequency changes over temperature to within ±3 ppm.

Noise performance of a 32 kHz clock is critical when it is used in wake-up circuitry for phones. The overall noise performance applicable for this application is shown in Fig. 20 which demonstrates the wake-up time accuracy. It is the measured peak-to-peak long term jitter (LTJ) at stride of 2.5 sec for 100 devices with a mean value of 0.7 μsec. As shown, it is well below the target noise performance suited for this application.

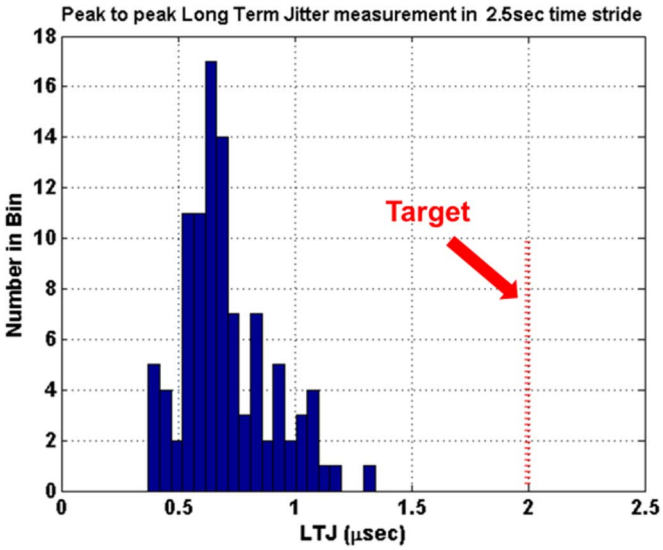

Fig. 20. Measured long term jitter in 2.5 sec time stride for 100 TCXO devices.

In low power mode where the PLL and TDC are powered down, LTJ is 3.6 μs.

Table I summarizes the measured performance and compares it with existing quartz-based 32 kHz XO and TCXO devices. As shown, the described 32 kHz MEMS-based oscillator outperforms quartz crystal-based solutions in several aspects but most notably in current consumption (at least 2$\times$ less) and package area (at least 6$\times$ smaller package) while demonstrating $\pm$3 ppm frequency stability over the industrial temperature range.

V. Conclusion

This paper has presented the first 32 kHz MEMS-based oscillator. It achieves TCXO frequency stability of $\pm$3 ppm, a footprint of 1.5 $\times$ 0.8 mm^2, and 1 μA current consumption. Frequency stability performance and low power consumption are achieved by combining a low temperature sensitivity MEMS resonator with an accurate temperature-to-digital converter and a low power fractional-N PLL, and by employing sub-threshold circuit design, duty-cycling, open-loop voltage regulation, and low swing drivers.

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Samira Zaliasl (S'09–M'12) received the B.S. degree in electrical and computer engineering from the University of Tehran, Tehran, Iran, in 2008, and the Ph.D. degree in electrical engineering from Oregon State University, Corvallis, OR, USA, in 2014. Her doctoral dissertation focused on solutions for non-idealities in delta-sigma-based modulators.

Since 2012, she has been with SiTime, Sunnyvale, CA, USA, where she now works on analog/mixed signal circuitries for high-performance temperature compensated MEMS-based oscillators.

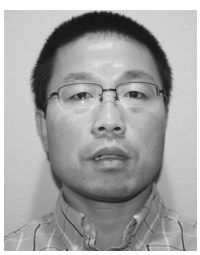
Jim C. Salvia (S'03–M'10) received the B.S. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 2005, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 2008 and 2010, respectively. His Ph.D. dissertation, "Micro-Oven Based Temperature Compensation Systems for MEMS Oscillators," focused on circuit and system development for the stabilization and temperature control of microresonator-based oscillators.

In 2010, he joined SiTime Corporation, Sunnyvale, CA, USA, where he developed CMOS circuitry for high-performance MEMS timing references. Since 2013, he has been with the Advanced Technology Division at InvenSense Corporation, San Jose, CA, USA, developing new sensor technology for the mobile consumer market.

Dr. Salvia is a National Science Foundation Graduate Fellow and a National Defense Science and Engineering Graduate Fellow.

Ginel C. Hill received the B.A. degree in physics from Williams College, Williamstown, MA, USA, in 2000, and the Ph.D. degree in applied physics from Stanford University, Stanford, CA, USA, in 2009. Her doctoral dissertation utilized dual-axis MEMS force sensors to measure the adhesive properties of gecko foot-hairs.

In 2009 and 2010, as a Postdoctoral Scholar working on a collaboration between IBM Almaden Research Center, San Jose, CA, USA, and Stanford University, she used ultrasensitive MEMS cantilevers in nanoscale Magnetic Resonance Imaging (nano-MRI.) In 2010, she joined SiTime Corporation, Sunnyvale, CA, USA, as a MEMS Development Engineer, where she now works on MEMS resonators for timing applications.



Lijun (Will) Chen received the B.S.E.E. degree from Xian Jiaotong University, China, in 1995 and the M.S.E.E. degree from Tsinghua University, China, and Oregon State University, Corvalllis, OR, USA, in 1998 and 2000, respectively.

Since then, he has held analog/RF design positions with various companies such as Xicor, Chrontel, Entropic Communications, Sigma Designs and Siport. Currently, he is with SiTime Corporation, Sunnyvale, CA, USA, designing MEMS-based high-performance CMOS circuit for timing reference chips.

Kimo Joo received the B.S.E.E. degree in computer engineering from Pusan National University, Korea, in 1994.

Since then, he has been working as a digital design engineer with several companies. He worked for Samsung Electronics in Korea for eight years, where he mainly developed Sigma-Delta ADC/DAC for audio applications. He also worked for Eastman Kodak for two years in charge of image signal processing development for CMOS sensors. In 2011, he joined SiTime Corporation, Sunnyvale, CA, USA, designing MEMS-based high-performance CMOS circuits for timing reference chips, and working on temperature compensation and sigma-delta modulators for fractional PLLs.

Rajkumar Palwai (M'13) received the M.Eng. degree from the Indian Institute of Science, Bangalore, India, in 2007.

He joined Texas Instruments, Bangalore, in 2010, where he worked on JESD I/O circuits for the high-speed pipeline ADCs. In 2012, he joined SiTime Corporation, Sunnyvale, CA, USA, and is currently working on the development of high-performance and low-power delta-sigma PLLs.

Niveditha Arumugam received the Bachelors degree in mechanical engineering from the College of Engineering Guindy, Chennai, India, in 2006, and the M.S. degree in mechanical engineering from Stanford University, Stanford, CA, USA, in 2008, specializing in MEMS and mechatronics.

She has been with SiTime Corporation, Sunnyvale, CA, USA, since 2007, and is the Manager of the Systems Design and Packaging Engineering group. She is an expert in characterization, testing, and packaging of MEMS-based timing devices and has most recently focused on the design of the innovative 2-die chip-scale package and development of the calibration techniques and test methodology for the 32 kHz XO and TCXO devices. Prior to SiTime, she was a Research Assistant in the Stanford Microsystems Group, focusing on microfabricated devices for small-scale biomechanics.

Meghan Phadke received the B.Tech. degree from the Indian Institute of Technology Madras, India, in 2009, and the M.S. degree from Stanford University, Stanford, CA, USA, in 2011, both in mechanical engineering.

He has worked on characterizing MEMS-based oscillators at SiTime Corporation, Sunnyvale, CA, USA.

Shouvik Mukherjee, photograph and biography not available at the time of publication.

Hae-Chang Lee received the B.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1998 and 2007, respectively.

He is currently a Director at Altera responsible for Analog and Transceiver IP used in the FPGA. Prior to Altera, he was Director of circuit design, characterization, and packaging at SiTime. In this role, he was responsible for overseeing products from architecture definition to new product introduction. He has also worked at Arda Technologies and Rambus.

Dr. Lee is a member of Phi Beta Kappa and Tau Beta Pi.

Charles Grosjean received the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, CA, USA.

He has been with SiTime Corporation, Sunnyvale, CA, USA, since 2006.

Paul M. Hagelin received the B.S. degree in engineering from Harvey Mudd College, Claremont, CA, USA, in 1991. He studied robotics in Europe as an IBM Thomas J. Watson Fellow in 1992, received the M.Sc. degree with Distinction in mechatronics and optical engineering from Loughborough University, Leicestershire, U.K., in 1993, and the Ph.D. degree in electrical engineering from the University of California, Davis, CA, USA, in 2000.

He co-founded C Speed Corporation in 1998, where he led the development of microelectromechanical systems (MEMS) micromirrors for optical switching. In 2005, he joined SiTime, Sunnyvale, CA, USA, to direct the development and fabrication of MEMS resonators and is currently VP of MEMS Engineering. Under his leadership, SiTime delivered the industry's first production MEMS used in timing. He has over 30 patents and 12 published papers in the fields of micromachining and optical systems.

Sudhakar Pamarti (S'98–M'03) received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, in 1995, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, San Diego, CA, USA, in 1999 and 2003, respectively.

He is an Associate Professor of electrical engineering at the University of California, Los Angeles (UCLA), CA, USA. Prior to joining UCLA, he worked at Rambus Inc. (2003–2005) and Hughes Software Systems (1995–1997) developing high-speed I/O circuits and embedded software and firmware for a wireless-in-local-loop communication system, respectively.

Dr. Pamarti was a recipient of the National Science Foundation's CAREER award for developing digital signal conditioning techniques to improve analog, mixed-signal, and radio frequency integrated circuits.

Terri S. Fiez (M'85–SM'95–F'05) received the B.S. and M.S. degrees in electrical engineering from the University of Idaho, Moscow, ID, USA, in 1984 and 1985, respectively, and the Ph.D. degree in electrical and computer engineering from Oregon State University, Corvallis, OR, USA, in 1990.

She is a Professor of electrical engineering and computer science (EECS) at Oregon State University (OSU). Prior to February 2014, she was Head of the School of EECS for 14 years. She has been involved in starting up and working with startup companies during the last decade. She has been very active professionally as a researcher in high performance analog signal processing integrated circuits and innovative engineering education approaches. She has served in numerous leadership roles within IEEE including conference committees and associate editorships. Prior to joining OSU in 1999, she was an assistant and associate professor at Washington State University from 1990 to 1999.

Dr. Fiez has previously received the NSF Young Investigator Award, the IEEE Solid-State Circuit Pre-doctoral Fellowship, and the 2006 IEEE Education Activities Board Innovative Education Award.

Kofi A. A. Makinwa (M'97–SM'05–F'11) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Nigeria, in 1985 and 1988, respectively. In 1989, he received the M.E.E. degree from the Philips International Institute, The Netherlands, and in 2004, the Ph.D. degree from Delft University of Technology, Delft, The Netherlands.

He is currently an Antoni van Leeuwenhoek Professor with the Faculty of Electrical Engineering, Computer Science and Mathematics, Delft University of Technology, which he joined in 1999. From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on interactive displays and on front-ends for optical and magnetic recording systems. His main research interests are in the design of precision mixed-signal circuits, sigma-delta modulators, smart sensors and sensor interfaces. This has resulted in 8 books, 22 patents and over 180 technical papers.

Dr. Makinwa is on the program committees of the European Solid-State Circuits Conference (ESSCIRC) and the Advances in Analog Circuit Design (AACD) workshop. From 2006 to 2012, he was on the Program Committee of the IEEE International Solid-State Circuits Conference (ISSCC). He has been a guest editor of three issues of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) and a Distinguished Lecturer of the IEEE Solid-State Circuits Society (2008 to 2011). For his doctoral research, he was awarded the 2005 Simon Stevin Gezel Award from the Dutch Technology Foundation. He was a co-recipient of several best paper awards, from the JSSC, ISSCC, Transducers, and ESSCIRC, among others. He is an alumnus of the Young Academy of the Royal Netherlands Academy of Arts and Sciences and an elected member of the IEEE Solid-State Circuits Society AdCom, the society's governing board.

Aaron Partridge (M'05) He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1996, 1999 and 2003. His thesis delivered MEMS accelerometers for the NASA X-33 space plane and the first thin-film encapsulated piezoresistive accelerometers.

He is Founder and Chief Scientist of SiTime Corporation, Sunnyvale, CA, USA, where he guides the technological direction. SiTime was founded in 2005 to develop MEMS-based timing references. From 2001 through 2004, he was Project Manager at Robert Bosch Research and Technology Center, where he coordinated the MEMS resonator and packaging research. From 1987 through 1991, he was a founder and Chief Scientist of Atomis, Inc., a manufacturer of STM, AFM, and BEEM (Scanning Tunneling, Atomic Force, and Ballistic Emission Electron) Microscopes. He has authored and co-authored 30 scientific papers and holds 60 patents.

Dr. Partridge serves on the IEEE International Solid-State Circuits Conference; Imagers, MEMS, Medical and Displays Subcommittee, is the Editorial Chair of the IEEE International Frequency Control Symposium, and is an Associate Editor for the IEEE TRANSACTIONS ON ULTRASONICS, FERROELECTRICS, AND FREQUENCY CONTROL.

Vinod Menon received the B.Tech. degree in electrical engineering from IIT Bombay, India, and the M.S. degree in electrical and computer engineering from the University of California, Santa Barbara, CA, USA.

He is Executive Vice President of Engineering at SiTime Corporation, Sunnyvale, CA, USA, and has over 30 years of semiconductor industry experience leading international IC development organizations and delivering innovative high-value products. Prior to joining SiTime, he was the VP, Serial Interface & Protocols Solutions at LSI Corporation, where he led high-speed SerDes, analog mixed-signal, Ethernet PHY and protocol IP developments for 65 nm/40 nm/28 nm ASICs and ASSPs. Before LSI, Vinod was a Business Unit and Engineering Director at National Semiconductor, where he led the successful turnaround of the Interface Division and delivered multiple generations of high-performance analog BiCMOS and CMOS products, including precision timing solutions. Earlier in his career, he directed product developments for wired and wireless networking, and storage connectivity at Advanced Micro Devices.