

### Description

The SiT92110 is a 10 output low-jitter clock, fan-out buffer, intended to be used in low jitter, high frequency clock/data distribution. The low impedance LVCMOS outputs are designed to drive 50  $\Omega$  series or parallel terminated transmission lines.

The buffer can choose a clock input from primary, secondary or crystal source. The primary and secondary clock sources can be single ended or fully differential. The selected clock is distributed to 10 LVCMOS output drivers.

The SiT92110 operates from a 3.3 V/2.5 V/1.8 V core supply and 3.3 V/2.5 V/1.8 V/1.5 V output supply. The core supply and output supply are independent of each other and no supply sequencing is required.

### Features

- Additive jitter performance of 50 fs RMS.
- Typical output skew between clock outputs is 30 ps
- Level translation with core supply voltage of 3.3 V/2.5 V/1.8 V and 3.3 V/2.5 V/1.8 V/1.5 V output supply for LVCMOS output drivers.
- The device inputs consists of primary, secondary and crystal inputs.
- The inputs are selected by programming input select pins of SiT92110. The input clock receiver in SiT92110 can accept LVPECL, LVDS, LVCMOS, SSTL, HCSL and XTAL waveforms.
- Crystal frequencies from 8 MHz to 50 MHz are supported.
- Crystal input can be over driven with frequency up to 250 MHz in crystal bypass mode
- SiT92110 buffer is available in a 32-pin, 5mm x 5mm QFN package.



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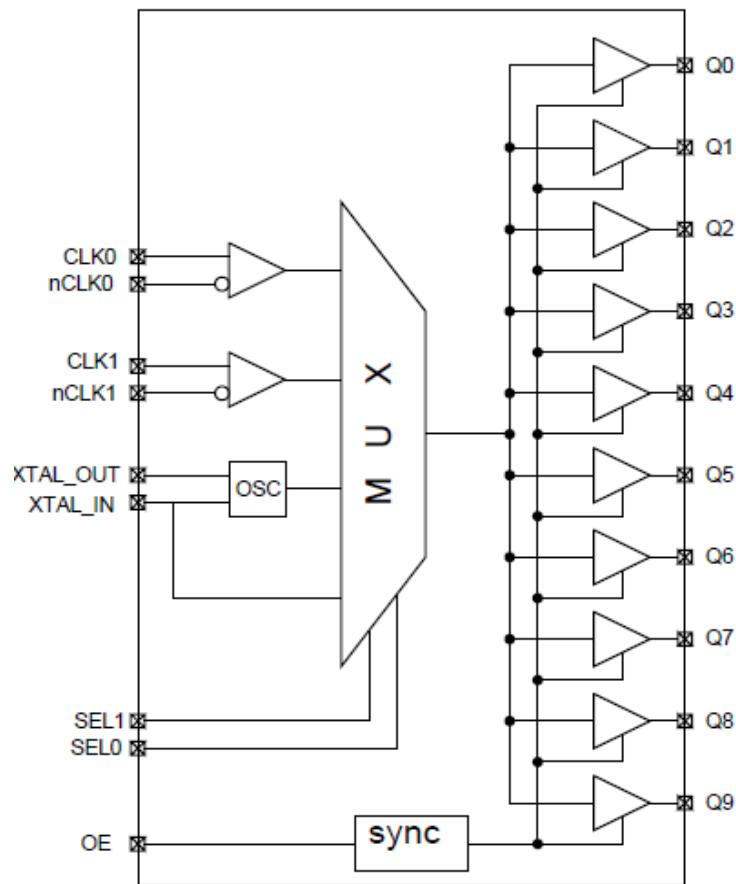
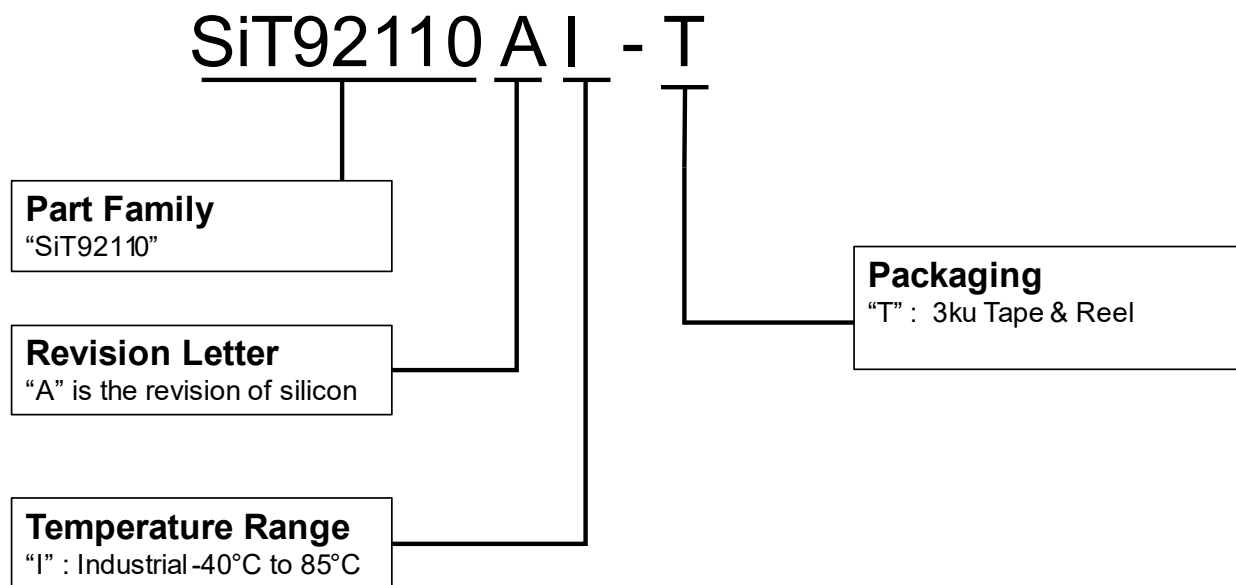


Figure 1. SiT92110 Functional Overview

## Table of Contents

|                                                                                |    |
|--------------------------------------------------------------------------------|----|
| Description .....                                                              | 1  |
| Features .....                                                                 | 1  |
| Ordering Information .....                                                     | 4  |
| Electrical Characteristics .....                                               | 5  |
| Functional Description .....                                                   | 12 |
| VDD and VDDO Power Supplies .....                                              | 12 |
| Clock Inputs .....                                                             | 12 |
| Clock States (Input vs Output States) .....                                    | 12 |
| Application Information .....                                                  | 14 |
| Driving the Clock Inputs .....                                                 | 14 |
| Driving Clock Inputs with LVCMOS Driver (AC coupled) .....                     | 14 |
| Driving Clock Inputs with LVCMOS Driver (DC coupled) .....                     | 15 |
| Driving XTAL_IN with LVCMOS Driver (AC coupled) .....                          | 18 |
| Driving XTAL_IN with LVCMOS Driver (DC coupled) .....                          | 19 |
| LVDS (DC coupled) .....                                                        | 20 |
| HCSL (DC coupled) .....                                                        | 20 |
| LVPECL (DC coupled) .....                                                      | 20 |
| SSTL (DC coupled) .....                                                        | 22 |
| LVDS (AC coupled) .....                                                        | 22 |
| LVPECL (AC coupled) .....                                                      | 23 |
| Termination of Output Driver of SiT92110 for Various Load Configurations ..... | 23 |
| SiT92110 Output ODR Termination for AC Coupled mode .....                      | 23 |
| SiT92110 Output ODR Termination for DC Coupled mode .....                      | 24 |
| CMOS (Capacitive load) .....                                                   | 26 |
| Power Considerations .....                                                     | 26 |
| Core Current in XO Mode .....                                                  | 27 |
| Parameter Measurement Information .....                                        | 27 |
| Differential Input Level .....                                                 | 27 |
| Skew and Input to Output Delay .....                                           | 27 |
| Rise and Fall Times .....                                                      | 28 |
| Isolation .....                                                                | 28 |
| Thermal Information .....                                                      | 29 |
| HOT Swap Recommendations .....                                                 | 30 |
| Introduction .....                                                             | 30 |
| Typical Differential Input Clock .....                                         | 30 |
| Input Clock Termination with Hot Swap Protection .....                         | 31 |
| LVPECL Termination Example .....                                               | 31 |
| LVDS Input Clock Termination Example .....                                     | 32 |
| HCSL Input Clock Termination Example .....                                     | 32 |
| LVCMOS Input Clock Termination with Hot Swap Protection .....                  | 33 |
| LVCMOS Output Clock Termination with Hot Swap Protection .....                 | 34 |
| Operation in Multiple VDDO Supply Domains .....                                | 35 |
| Package Dimensions and Patterns .....                                          | 36 |

Ordering Information



## Electrical Characteristics

**Table 1. Absolute Maximum Ratings**

| Parameters                                | Conditions | Symbol    | Min  | Typ | Max          | Units |
|-------------------------------------------|------------|-----------|------|-----|--------------|-------|
| Core Supply Voltage                       |            | $V_{DD}$  | -0.5 |     | 3.6          | V     |
| Output Supply Voltage                     |            | $V_{DDO}$ | -0.5 |     | 3.6          | V     |
| Input voltage, All Inputs, except XTAL_IN |            | $V_{IN}$  | -0.3 |     | $V_{DD}+0.3$ | V     |
| XTAL_IN                                   |            | $V_{IN}$  | -0.5 |     | 1.8          | V     |
| Storage temperature                       |            | $T_{STG}$ | -55  |     | 150          | °C    |
| Junction Temperature                      |            | $T_J$     |      |     | 125          | °C    |
| Moisture Saturation Level                 |            | MSL       |      | 3   |              |       |

**Notes:**

- Exceeding maximum ratings may shorten the useful life of the device.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage

**Table 2. Recommended Operating Conditions**

| Parameters            | Conditions | Symbol    | Min   | Typ | Max   | Units |
|-----------------------|------------|-----------|-------|-----|-------|-------|
| Core supply voltage   |            | $V_{DD}$  | 3.135 | 3.3 | 3.465 | V     |
|                       |            |           | 2.375 | 2.5 | 2.625 | V     |
|                       |            |           | 1.71  | 1.8 | 1.89  | V     |
| Output supply voltage |            | $V_{DDO}$ | 3.135 | 3.3 | 3.465 | V     |
|                       |            |           | 2.375 | 2.5 | 2.625 | V     |
|                       |            |           | 1.6   | 1.8 | 2     | V     |
|                       |            |           | 1.35  | 1.5 | 1.65  | V     |
| Ambient Temperature   |            | $T_A$     | -40   | 27  | 85    | °C    |

**Table 3 DC Electrical Characteristics**

Unless otherwise specified:  $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ ,  $V_{DDO} = 3.3\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ ,  $1.8\text{ V} \pm 10\%$ ,  $1.5\text{ V} \pm 10\%$ ,  $-40\text{ °C} \leq T_A \leq 85\text{ °C}$ , CLK0/1 driven differentially, input slew rate  $\geq 2\text{ V/ns}$ . Typical values represent most likely parametric norms at  $V_{DD} = 3.3\text{ V}$ ,  $V_{DDO} = 3.3\text{ V}$ ,  $T_A = 25\text{ °C}$ .

| Parameters                                           | Conditions                                                        | Symbol            | Min | Typ | Max  | Units |
|------------------------------------------------------|-------------------------------------------------------------------|-------------------|-----|-----|------|-------|
| <b>Current Consumption</b>                           |                                                                   |                   |     |     |      |       |
| Static current taken by core supply when no toggling | $V_{DD} = 3.3\text{ V}$ , $V_{DDO} = 3.3\text{ V}$ , $F_{in} = 0$ | $I_{CORE,STATIC}$ |     | 16  | 19.8 | mA    |

|                                                               |                                                                                |                              |                    |      |                    |            |
|---------------------------------------------------------------|--------------------------------------------------------------------------------|------------------------------|--------------------|------|--------------------|------------|
| Static current taken by output driver supply when no toggling | $V_{DD} = 3.3\text{ V}$ , $V_{DDO} = 3.3\text{ V}$ , $F_{in} = 0$              | $I_{ODR,STATIC}$             |                    | 3.5  | 4.2                | mA         |
| Current taken by core supply, if XTAL is enabled              | $V_{DD} = 3.3\text{ V}$ , $V_{DDO} = 3.3\text{ V}$ , $F_{OSC} = 25\text{ MHz}$ | $I_{CORE,STATIC,XTAL}^{(1)}$ |                    | 11.5 | 14                 | mA         |
| Power Dissipation Capacitance per output                      | $V_{DD} = 3.3\text{ V}$ , $V_{DDO} = 3.3\text{ V}$ , $F_{in} = 200\text{ MHz}$ | $C_{PD}^{(1)}$               |                    | 4    | 5.2                | pF         |
| Dynamic current taken by core supply                          | $V_{DD} = 3.3\text{ V}$ , $V_{DDO} = 3.3\text{ V}$ , $F_{in} = 100\text{ MHz}$ | $I_{CORE,DYN}$               |                    | 1.3  | 1.56               | mA         |
| <b>Input Control Pin Characteristic</b>                       |                                                                                |                              |                    |      |                    |            |
| High level input voltage                                      |                                                                                | $V_{IH}$                     | $0.7 \cdot V_{DD}$ |      | $V_{DD}$           | V          |
| Low level input voltage                                       |                                                                                | $V_{IL}$                     | GND                |      | $0.3 \cdot V_{DD}$ | V          |
| High level input current                                      | $V_{IH} = V_{DD} = 3.3\text{ V}$                                               | $I_{IH}$                     |                    | 30   | 50                 | uA         |
| Low level input current                                       |                                                                                | $I_{IL}$                     | -20                | 0.1  |                    | uA         |
| Pull down resistance                                          |                                                                                | $R_{PULLDOWN}$               |                    | 200  |                    | K $\Omega$ |
| Input capacitance                                             |                                                                                | $C_{IN}$                     |                    | 2    |                    | pF         |

**Notes:**

1. Specification is guaranteed by characterization and is not tested in production

**Table 4 Input Clock Characteristics**

Unless otherwise specified:  $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ ,  $V_{DDO} = 3.3\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ ,  $1.8\text{ V} \pm 10\%$ ,  $1.5\text{ V} \pm 10\%$ ,  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , CLK0/1 driven differentially, input slew rate  $\geq 2\text{ V/ns}$ . Typical values represent most likely parametric norms at  $V_{DD} = 3.3\text{ V}$ ,  $V_{DDO} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ .

| Parameter                                                      | Condition                                                                 | Symbol                 | Min  | Typ | Max             | Unit       |
|----------------------------------------------------------------|---------------------------------------------------------------------------|------------------------|------|-----|-----------------|------------|
| <b>DC Characteristics of universal input clock pins</b>        |                                                                           |                        |      |     |                 |            |
| High level input current                                       | $V_{IH} = V_{DD} = 3.465\text{ V}$                                        | $I_{IH}$               |      |     | 650             | uA         |
| Low level input current                                        |                                                                           | $I_{IL}$               | -650 |     |                 | uA         |
| Pull up or pull down resistor on CLK0/1                        |                                                                           | $R_{PULLUP\_PULLDOWN}$ |      | 7.5 |                 | K $\Omega$ |
| Differential Input Voltage Swing (peak to peak) <sup>(1)</sup> |                                                                           | $V_{IDIFF}$            | 0.15 |     | 1.3             | V          |
| Differential Input Common Mode Voltage <sup>(2)</sup>          | $V_{IDIFF} = 150\text{ mV}$                                               | $V_{ICM}$              | 0.25 |     | $V_{DD} - 0.85$ | V          |
| Single Ended Input High Voltage <sup>(2)</sup>                 | Inverting differential input held at $V_{DD}/2$ , $V_{DD} = 3.3\text{ V}$ | $V_{IHSE}$             | 2    |     | $V_{DD} + 0.3$  | V          |
|                                                                | Inverting differential input held at $V_{DD}/2$ , $V_{DD} = 2.5\text{ V}$ |                        | 1.6  |     | $V_{DD} + 0.3$  | V          |
| Single Ended Input Low Voltage <sup>(2)</sup>                  | Inverting differential input held at $V_{DD}/2$ , $V_{DD} = 3.3\text{ V}$ | $V_{ILSE}$             | -0.3 |     | 1.3             | V          |

|                                                                                           |                                                                                                                                                                 |                         |      |             |      |                    |
|-------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|------|-------------|------|--------------------|
|                                                                                           | Inverting differential input held at VDD/2, V <sub>DD</sub> = 2.5 V                                                                                             |                         | -0.3 |             | 0.9  | V                  |
| <b>AC Characteristics of universal input clock pins</b>                                   |                                                                                                                                                                 |                         |      |             |      |                    |
| Input slew rate                                                                           | 20% to 80%                                                                                                                                                      | $\Delta V_i / \Delta T$ |      | 2           |      | V/ns               |
| Input Capacitance                                                                         | Single ended                                                                                                                                                    | C <sub>IN</sub>         | —    | 700         | —    | fF                 |
| Input Frequency Range <sup>(4)</sup>                                                      | LVDS and LVPECL outputs                                                                                                                                         | f <sub>IN</sub>         | —    | —           | 250  | MHz                |
|                                                                                           | HCSL outputs                                                                                                                                                    |                         | —    | —           | 250  | MHz                |
|                                                                                           | LVCMOS outputs                                                                                                                                                  |                         | —    | —           | 250  | MHz                |
| Input duty cycle, such that output duty cycle is equal to input duty cycle <sup>(5)</sup> | The pass condition for the measurement is that output duty cycle is within $\pm 5\%$ of input duty cycle. The input clock amplitude is same as LVPECL standard. | I <sub>DC</sub>         | 40   |             | 60   | %                  |
| Mux isolation clk0 to clk1 <sup>(3)</sup>                                                 | Foffset > 50 KHz,<br>Pclkin = 0 dBm,<br>Fclkin0 = 156.25 MHz                                                                                                    | ISO <sub>MUX</sub>      |      | -85         |      | dBc                |
| <b>Crystal Characteristic</b>                                                             |                                                                                                                                                                 |                         |      |             |      |                    |
| Equivalent series resistance                                                              |                                                                                                                                                                 | ESR                     |      | 35          | 60   | $\Omega$           |
| load capacitance                                                                          |                                                                                                                                                                 | C <sub>L</sub>          | 6    | 8           | 10   | pF                 |
| Shunt Capacitance                                                                         |                                                                                                                                                                 | C <sub>o</sub>          |      | 2           | 3    | pF                 |
| Drive level                                                                               |                                                                                                                                                                 |                         |      | 100         | 200  | $\mu$ W            |
| Mode of oscillation                                                                       |                                                                                                                                                                 |                         |      | fundamental |      |                    |
| Supported crystal frequency range <sup>(3)</sup>                                          |                                                                                                                                                                 | Frequency               | 8    |             | 50   | MHz                |
| Input Voltage Swing                                                                       | Bypass mode                                                                                                                                                     | V <sub>in_SE</sub>      | 1    |             | 1.8  | V <sub>pp_se</sub> |
| V <sub>ih_se</sub>                                                                        | Bypass DC coupled mode.<br>SEL[1] = 1 & SEL[0]=1                                                                                                                | V <sub>ih</sub>         | 0.98 |             |      | V                  |
| V <sub>il_se</sub>                                                                        |                                                                                                                                                                 | V <sub>il</sub>         |      |             | 0.36 | V                  |
| F <sub>osc</sub> = 8 MHz                                                                  | Settling time required for output in crystal mode                                                                                                               | t <sub>settle</sub>     |      | 14          |      | ms                 |
| F <sub>osc</sub> = 25, 50 MHz                                                             |                                                                                                                                                                 |                         |      | 8           |      | ms                 |
| XO bypass AC coupled mode additive jitter <sup>(3)</sup>                                  | V <sub>DDO</sub> = 3.3 V<br>Slew Rate > 2 V/ns<br>Fin = 48 MHz                                                                                                  | t <sub>jit</sub>        |      | 100         |      | fs                 |

|                                     |                                                                                                                                                            |           |  |     |  |    |
|-------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--|-----|--|----|
|                                     | $V_{DDO} = 2.5\text{ V}$<br>Slew Rate > 2 V/ns<br>$F_{in} = 48\text{ MHz}$                                                                                 |           |  | 115 |  | fs |
|                                     | $V_{DDO} = 1.8\text{ V}$<br>Slew Rate > 2 V/ns<br>$F_{in} = 48\text{ MHz}$                                                                                 |           |  | 230 |  | fs |
| Crystal Phase jitter <sup>(6)</sup> | RMS, integration BW<br>12 KHz to 5 MHz,<br>$F_{crystal} = 25\text{ MHz}$ . Crystal<br>input select<br><br>Measured at<br>$V_{DD} = V_{DDO} = 2.5\text{ V}$ | $t_{jit}$ |  | 155 |  | fs |

**Notes:**

1. Inverting differential input clock pin biased at  $V_{DD}/2$
2. Input common mode defined as  $V_{IH}$  (see [Figure 26](#))
3. Specification is guaranteed by characterization and is not tested in production
4. If the input clock is initially absent when the chip is just powered up, it will take at least 2 falling edge of clock cycles for the output to appear. Therefore, the buffer level translates DC only after it sees two consecutive falling edge of input clock
5. Output duty cycle equals input duty cycle. ATE measurement done with 80% on time and 20% off time waveform to make sure that output duty cycle is equal to input duty cycle even with skewed input duty cycle.
6. Crystal Phase Jitter is measure on following part number, 7M-25.000MAKV-T

**Table 5 Output Clock Characteristics – LVCMOS**

| Parameter                                              | Condition                                                           | Symbol    | Min  | Typ | Max  | Unit     |
|--------------------------------------------------------|---------------------------------------------------------------------|-----------|------|-----|------|----------|
| Maximum output frequency                               | Universal clock input                                               | $F_{out}$ |      |     | 250  | MHz      |
|                                                        | XTAL <sup>(1)</sup>                                                 |           |      |     | 50   | MHz      |
| Output duty cycle                                      | For $F_{in} \leq 200\text{ MHz}$                                    | Odc       | 45   |     | 55   | %        |
|                                                        | For $200\text{ MHz} < F_{in} < 250\text{ MHz}$                      |           | 40   |     | 60   |          |
| Output high level voltage                              | $V_{DDO} = 3.3 \pm 5\%$ , 12 mA pull down current                   | $V_{OH}$  | 2.6  |     |      | V        |
|                                                        | $V_{DDO} = 2.5 \pm 5\%$ , 8 mA pull down current                    |           | 1.8  |     |      | V        |
|                                                        | $V_{DDO} = 1.8\text{ V} \pm 200\text{ mV}$ , 2 mA pull down current |           | 1.2  |     |      | V        |
|                                                        | $V_{DDO} = 1.5\text{ V} \pm 150\text{ mV}$ , 2 mA pull down current |           | 0.95 |     |      | V        |
| Output low level voltage                               | $V_{DDO} = 3.3 \pm 5\%$ , 12 mA pull up current                     | $V_{OL}$  |      |     | 0.5  | V        |
|                                                        | $V_{DDO} = 2.5 \pm 5\%$ , 8 mA pull up current                      |           |      |     | 0.5  | V        |
|                                                        | $V_{DDO} = 1.8\text{ V} \pm 200\text{ mV}$ , 2 mA pull up current   |           |      |     | 0.4  | V        |
|                                                        | $V_{DDO} = 1.5\text{ V} \pm 150\text{ mV}$ , 2mA pull up current    |           |      |     | 0.35 | V        |
| Effective output impedance, for maximum slice strength | $V_{DDO} = 3.3\text{ V}$                                            | $R_{out}$ |      | 15  |      | $\Omega$ |
|                                                        | $V_{DDO} = 2.5\text{ V}$                                            |           |      | 18  |      | $\Omega$ |
|                                                        | $V_{DDO} = 1.8\text{ V}$                                            |           |      | 23  |      | $\Omega$ |
|                                                        | $V_{DDO} = 1.5\text{ V}$                                            |           |      | 28  |      | $\Omega$ |
| Output skew <sup>(1)</sup>                             | $V_{DDO} = 3.465\text{ V}$                                          | $t_{sk}$  |      | 40  |      | ps       |
|                                                        | $V_{DDO} = 2.5\text{ V}$                                            |           |      | 35  |      | ps       |
|                                                        | $V_{DDO} = 1.62\text{ V}$                                           |           |      | 31  |      | ps       |
|                                                        | $V_{DDO} = 1.35\text{ V}$                                           |           |      | 36  |      | ps       |



|                                                  |                                                                                                          |           |  |     |     |       |
|--------------------------------------------------|----------------------------------------------------------------------------------------------------------|-----------|--|-----|-----|-------|
| Time for output enable or disable <sup>(1)</sup> |                                                                                                          | $t_{en}$  |  |     | 4   | cycle |
| Input to clock edge to output clock edge delay   | $V_{DDO} = 3.465\text{ V}$ , PCB trace of 5 inch, 10 pF capacitor AC coupled 50 $\Omega$ load            | $t_d$     |  | 1.4 |     | ns    |
|                                                  | $V_{DDO} = 2.5\text{ V}$ , PCB trace of 5 inch, 10 pF capacitor AC coupled 50 $\Omega$ load              |           |  | 1.5 |     | ns    |
|                                                  | $V_{DDO} = 1.62\text{ V}$ , PCB trace of 5 inch, 10 pF capacitor AC coupled 50 $\Omega$ load             |           |  | 2   |     | ns    |
|                                                  | $V_{DDO} = 1.35\text{ V}$ , PCB trace of 5 inch, 10 pF capacitor AC coupled 50 $\Omega$ load             |           |  | 2.5 |     | ns    |
| Additive jitter <sup>(1)</sup>                   | $V_{DDO} = 3.465\text{ V}$<br>Slew rate (SiT92110) $\geq 2\text{ V/ns}$                                  | $t_{jit}$ |  | 21  |     | fs    |
|                                                  | $V_{DDO} = 2.5\text{ V}$<br>Slew rate (SiT92110) $\geq 2\text{ V/ns}$                                    |           |  | 37  |     | fs    |
|                                                  | $V_{DDO} = 1.62\text{ V}$<br>Slew rate (SiT92110) $\geq 2\text{ V/ns}$                                   |           |  | 87  |     | fs    |
|                                                  | $V_{DDO} = 1.35\text{ V}$<br>Slew rate (SiT92110) $\geq 2\text{ V/ns}$                                   |           |  | 233 |     | fs    |
| Rise time <sup>(1)</sup>                         | Output rise time 20% to 80%<br>Load cap 5 pF,<br>$V_{DDO} = 3.3\text{ V}$ , AC coupled 50 $\Omega$ load  | $t_R$     |  |     | 605 | ps    |
|                                                  | Output rise time 20% to 80%<br>Load cap 5 pF,<br>$V_{DDO} = 2.5\text{ V}$ , AC coupled 50 $\Omega$ load  |           |  |     | 605 | ps    |
|                                                  | Output rise time 20% to 80%<br>Load cap 5 pF,<br>$V_{DDO} = 1.62\text{ V}$ , AC coupled 50 $\Omega$ load |           |  |     | 605 | ps    |
|                                                  | Output rise time 20% to 80%<br>Load cap 5 pF,<br>$V_{DDO} = 1.35\text{ V}$ , AC coupled 50 $\Omega$ load |           |  |     | 605 | ps    |
| Fall time <sup>(1)</sup>                         | Output fall time 20% to 80%<br>Load cap 5 pF,<br>$V_{DDO} = 3.3\text{ V}$                                | $t_F$     |  |     | 605 | ps    |
|                                                  | Output fall time 20% to 80%<br>Load cap 5 pF,<br>$V_{DDO} = 2.5\text{ V}$                                |           |  |     | 605 | ps    |
|                                                  | Output fall time 20% to 80%<br>Load cap 5 pF,<br>$V_{DDO} = 1.62\text{ V}$                               |           |  |     | 605 | ps    |
|                                                  | Output fall time 20% to 80%<br>Load cap 5 pF,<br>$V_{DDO} = 1.35\text{ V}$                               |           |  |     | 605 | ps    |

**Notes:** Specification is guaranteed by characterization and is not tested in production

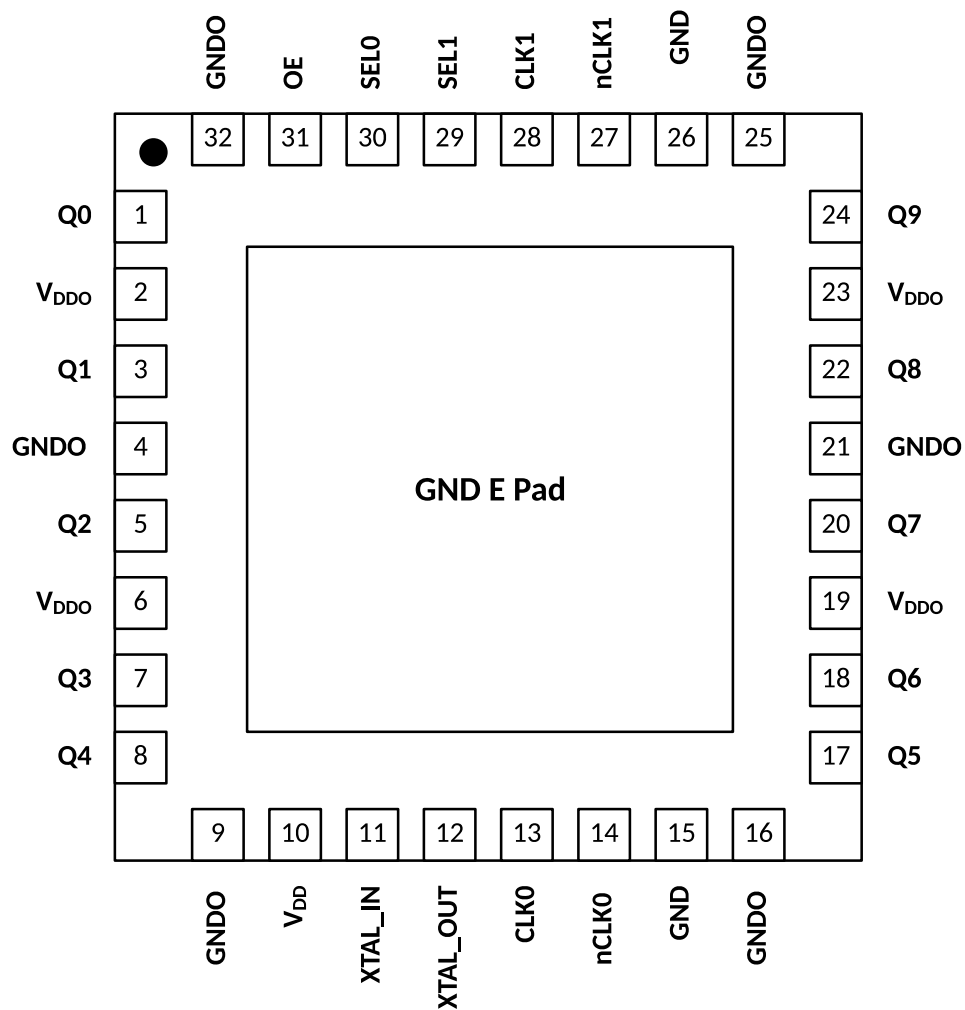


Figure 2. SiT92110 Top View

Table 6. Detailed Pin Description

| Pin Name                            | Pin Number | Functionality SiT92110                                                                                                                                                                                                                                                                                                                                                            |
|-------------------------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Pin group: Clock output pins</b> |            |                                                                                                                                                                                                                                                                                                                                                                                   |
| Q0                                  | 1          | LVCMOS output 0                                                                                                                                                                                                                                                                                                                                                                   |
| Q1                                  | 3          | LVCMOS output 1                                                                                                                                                                                                                                                                                                                                                                   |
| Q2                                  | 5          | LVCMOS output 2                                                                                                                                                                                                                                                                                                                                                                   |
| Q3                                  | 7          | LVCMOS output 3                                                                                                                                                                                                                                                                                                                                                                   |
| Q4                                  | 8          | LVCMOS output 4                                                                                                                                                                                                                                                                                                                                                                   |
| Q5                                  | 17         | LVCMOS output 5                                                                                                                                                                                                                                                                                                                                                                   |
| Q6                                  | 18         | LVCMOS output 6                                                                                                                                                                                                                                                                                                                                                                   |
| Q7                                  | 20         | LVCMOS output 7                                                                                                                                                                                                                                                                                                                                                                   |
| Q8                                  | 22         | LVCMOS output 8                                                                                                                                                                                                                                                                                                                                                                   |
| Q9                                  | 24         | LVCMOS output 9                                                                                                                                                                                                                                                                                                                                                                   |
| <b>Pin group: Power pins</b>        |            |                                                                                                                                                                                                                                                                                                                                                                                   |
| VDDO                                | 2          | I/O power pins 3.3/2.5/1.8/1.5 V                                                                                                                                                                                                                                                                                                                                                  |
| VDDO                                | 6          | I/O power pins 3.3/2.5/1.8/1.5 V                                                                                                                                                                                                                                                                                                                                                  |
| VDDO                                | 19         | I/O power pins 3.3/2.5/1.8/1.5 V                                                                                                                                                                                                                                                                                                                                                  |
| VDDO                                | 23         | I/O power pins 3.3/2.5/1.8/1.5 V                                                                                                                                                                                                                                                                                                                                                  |
| VDD                                 | 10         | Line supply 3.3/2.5/1.8 V - SiT92110 can support 1.8 V on line supply                                                                                                                                                                                                                                                                                                             |
| GNDO                                | 9          | Ground                                                                                                                                                                                                                                                                                                                                                                            |
| GND                                 | 15         | Ground                                                                                                                                                                                                                                                                                                                                                                            |
| GNDO                                | 16         | Ground                                                                                                                                                                                                                                                                                                                                                                            |
| GNDO                                | 4          | Ground                                                                                                                                                                                                                                                                                                                                                                            |
| GNDO                                | 21         | Ground                                                                                                                                                                                                                                                                                                                                                                            |
| GND                                 | 26         | Ground                                                                                                                                                                                                                                                                                                                                                                            |
| GNDO                                | 25         | Ground                                                                                                                                                                                                                                                                                                                                                                            |
| GNDO                                | 32         | Ground                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Pin group: Clock input Pins</b>  |            |                                                                                                                                                                                                                                                                                                                                                                                   |
| XTAL_IN                             | 11         | Input for crystal. It can be over driven by an ac-coupled single ended clock in crystal over drive mode.<br>In the external bypass mode, the max voltage at the pin needs to be 1.8 V. If the driver is swinging to say 3.3 V rail, then a resistor divider is needed on PCB to restrict the swing at XTAL_IN to 1.8 V<br>Load supported 6 pF to 10 pF, frequency 8 MHz to 50 MHz |
| XTAL_OUT                            | 12         | crystal oscillator pin                                                                                                                                                                                                                                                                                                                                                            |
| CLK0                                | 13         | Non-inverting differential or single-ended primary input                                                                                                                                                                                                                                                                                                                          |
| nCLK0                               | 14         | Inverting differential primary input                                                                                                                                                                                                                                                                                                                                              |
| nCLK1                               | 27         | inverting differential secondary input                                                                                                                                                                                                                                                                                                                                            |
| CLK1                                | 28         | Non-Inverting differential or single ended secondary input                                                                                                                                                                                                                                                                                                                        |
| <b>Pin group: Control Pins</b>      |            |                                                                                                                                                                                                                                                                                                                                                                                   |
| SEL1                                | 29         | Input clock select 1                                                                                                                                                                                                                                                                                                                                                              |
| SEL0                                | 30         | Input clock select 0                                                                                                                                                                                                                                                                                                                                                              |
| OE                                  | 31         | Output enable                                                                                                                                                                                                                                                                                                                                                                     |

## Functional Description

The SiT92110 is a 10-output differential clock fan out buffer with low additive jitter that can operate up to 250 MHz. It features a 3:1 input multiplexer with an optional crystal oscillator input and ten LVCMOS output. The input selection and output buffer modes are controlled via pin strapping. The device is offered in a 32 pin QFN package.

## VDD and VDDO Power Supplies

The SiT92110 has separate 3.3 V/2.5 V/1.8 V core (VDD) and 3.3 V/2.5 V/1.8 V/1.5 V output power supply (VDDO). Output supply operation at 2.5 V/1.8 V/1.5 V enables lower power consumption and output-level compatibility with 2.5 V/1.8 V/1.5 V receiver devices. The output levels LVCMOS (VOH) is referenced to its respective VDDO supply.

## Clock Inputs

The input clock can be selected from primary universal clock input, secondary universal clock input, or Xin. Clock input selection is controlled using the SEL[1:0] inputs as shown in [Table 7](#)

**Table 7 Input Clock Selection**

| SEL[1] | SEL[0] | Selected Clock                                  |
|--------|--------|-------------------------------------------------|
| 0      | 0      | CLK0                                            |
| 0      | 1      | CLK1                                            |
| 1      | 0      | Crystal<br>Or<br>Crystal bypass AC coupled mode |
| 1      | 1      | Crystal bypass DC coupled mode                  |

## Clock States (Input vs Output States)

**Table 8 Input versus Output Stages**

| State of Selected Clock input | Output State |
|-------------------------------|--------------|
| Inputs are floating           | Logic low    |
| Inputs are logic low          | logic low    |
| Inputs are logic high         | logic high   |

## Output Enable

Pulling OE to LOW, forces the outputs to the high-impedance state after the four falling edge of the input signal. The outputs remain in the high-impedance state as long as OE is LOW. The OE signal is internally synchronized to the selected input clock. This allows disabling the output clock at the falling edge of input clock in a glitch free manner.

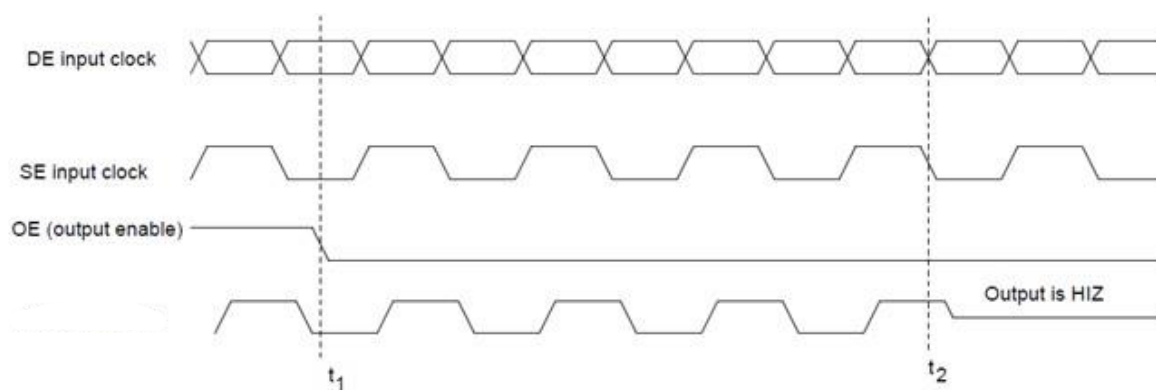
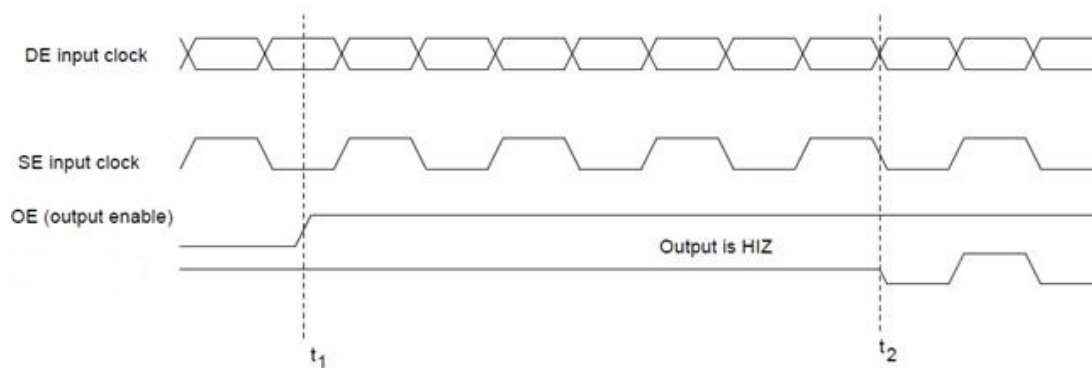
When OE goes from low to high, the output clock is enabled within a time delay  $t_d$ , where  $t_d$  is given by the following equation.

$$t_{d,refout\_en} = 0.5n + 4 * T_{in}.$$

$T_{in}$  is the time period of the input clock.

**Table 9 OE Functionality**

| OE | Output State   |
|----|----------------|
| 0  | Disabled (HIZ) |
| 1  | Enabled        |

**Figure 3 OE: Output disable.****Figure 4 OE: Output enable.**

## Application Information

### Driving the Clock Inputs

The SiT92110 has two universal clock inputs (CLK0/nCLK0 and CLK1/nCLK1). SiT92110 can accept 3.3 V/2.5 V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet input common mode, slew rate and swing requirements specified in the Electrical Characteristics. The SiT92110 supports a wide common mode voltage range and input signal swing.

### Driving Clock Inputs with LVCMOS Driver (AC coupled)

Figure 5 shows how a differential input can be wired to accept LVCMOS single ended levels in AC coupled mode. The bypass capacitor (C1) is used to help filter noise on the DC bias on the inverting pin of the clock input. This bypass should be located as close to the input pin as possible. Two resistors  $R_{T1}$  and  $R_{T2}$  set the common mode voltage at the output of the LVCMOS driver to  $VDD/2$ . This prevents average DC leakage current from the LVCMOS driver and avoids unnecessary power dissipation.

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the  $R_{T1}$  and  $R_{T2}$  values should be adjusted to set the V1 at 1.25 V. This configuration requires

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have high slew rate of 2 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter.

It is recommended to drive the input signal differentially for better slew rate and jitter. The user can also drive a single ended clock. If the user is driving the single ended clock signal on say CLK0, then nCLK0 pin need to be connected to a 0.1 uF capacitor on the PCB.

that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in the following way. First,  $R_{T1}$  and  $R_{T2}$  in parallel should equal the transmission line impedance. For most 50  $\Omega$  applications,  $R_{T1}$  and  $R_{T2}$  can be 100  $\Omega$ .

$$Z_o = R_o + R_s = 50 \Omega$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50 \Omega$$

$$\frac{VDD * R_{T2}}{R_{T1} + R_{T2}} = \frac{VDD}{2}$$

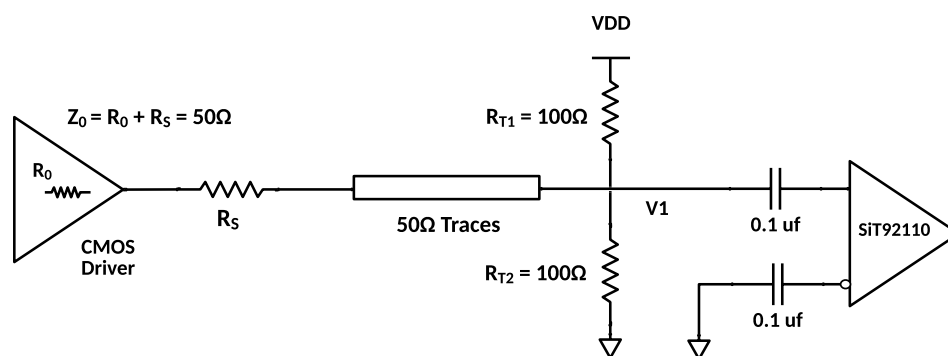


Figure 5 AC coupling LVCMOS clock to SiT92110

The inverting differential input can be connected to a 0.1 uF bypass capacitor. This pin is biased internally to a voltage close to  $VDD/2$ .

Another variant of the AC coupling of LVCMOS input clock is shown in Figure 6. We use single termination resistor of 50  $\Omega$  to ground. A 0.1 uF AC coupling capacitor is

connected in series with the LVCMOS clock source to prevent DC leakage current.

$$Z_o = R_o + R_s = 50 \Omega$$

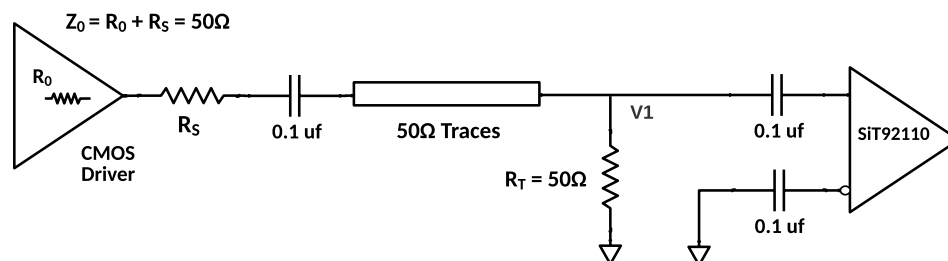


Figure 6 AC coupling of LVCMOS clock with single 50 Ω resistor termination to ground

### Driving Clock Inputs with LVCMOS Driver (DC coupled)

Figure 7 shows how a differential input can be wired to accept LVCMOS single ended clock signals in DC coupled mode. The reference voltage  $V1 = VDD/2$  is generated by the bias resistors  $R_{S1}$  and  $R_{S2}$ . The bypass capacitor ( $C1$ ) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of  $R_{S1}$  and  $R_{S2}$  might need to be adjusted to position the bias voltage  $V2$  in the center of the input voltage swing. Typical values of bias circuit resistance are  $R_{S1} = 1\text{ K}\Omega$  and  $R_{S2} = 1\text{ K}\Omega$

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{VDD * R_{s2}}{R_{s1} + R_{s2}} = \frac{VDD}{2}$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ \Omega$$

$$\frac{VDD * R_{T2}}{R_{T1} + R_{T2}} = \frac{VDD}{2}$$

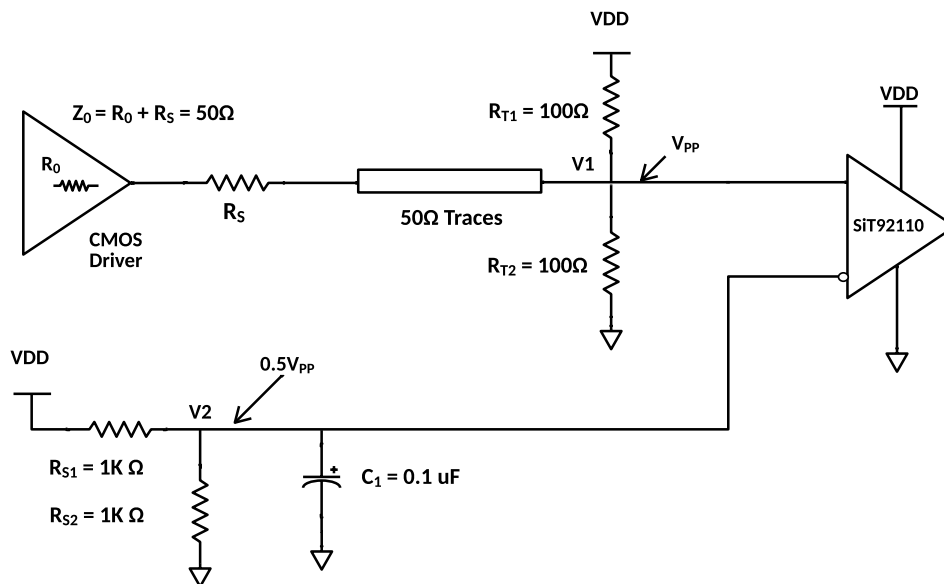


Figure 7 DC coupling of LVCMOS clock to SiT92110 – configuration 1

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the  $R_{S1}$  and  $R_{S2}$  values should be adjusted to set the V2 at 1.25 V. The values below are for when both the single ended swing and VDD are at the same voltage.

This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First,  $R_{T1}$  and  $R_{T2}$  in parallel should equal the transmission line impedance. For most 50  $\Omega$  applications,  $R_{T1}$  and  $R_{T2}$  can be 100  $\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 8 shows a second input clock configuration where  $R_{T1}$ ,  $R_{T2}$  are removed and replaced with a 50  $\Omega$  termination

resistor  $R_T$  to ground. It is possible that LVCMOS driver (or clock source) may not be able to drive 50  $\Omega$  load in DC coupled mode. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 8 is given below

$$Z_o = R_o + R_s = 50 \text{ Ohm}$$

$$\frac{VDD * R_{s2}}{R_{s1} + R_{s2}} = \frac{V_{pp}}{2}$$

The LVCMOS single ended clock input with series RC termination near the buffer is shown in Figure 9. There is a single termination resistor  $R_T$  which is connected to ground through a capacitor  $C_{AC}$ . The value of series capacitor is given by a formula.

$$C_{AC} \geq \frac{3T_D}{50\Omega}, T_D \text{ is the transmission line delay}$$



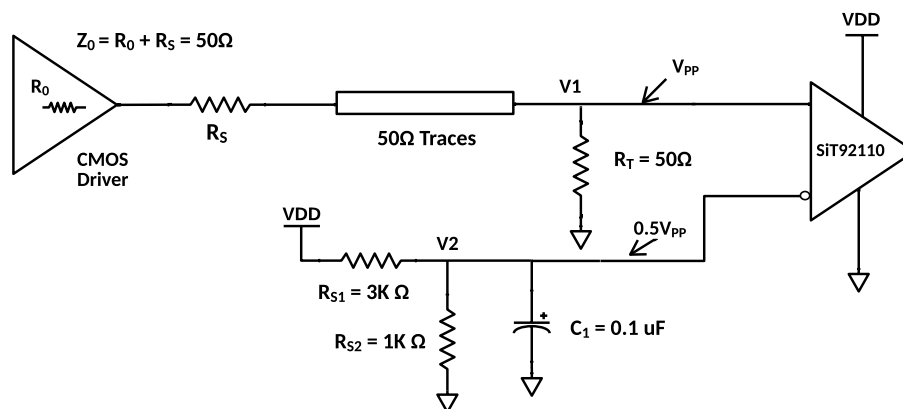


Figure 8 DC coupled LVCMOS input clock configuration – configuration 2

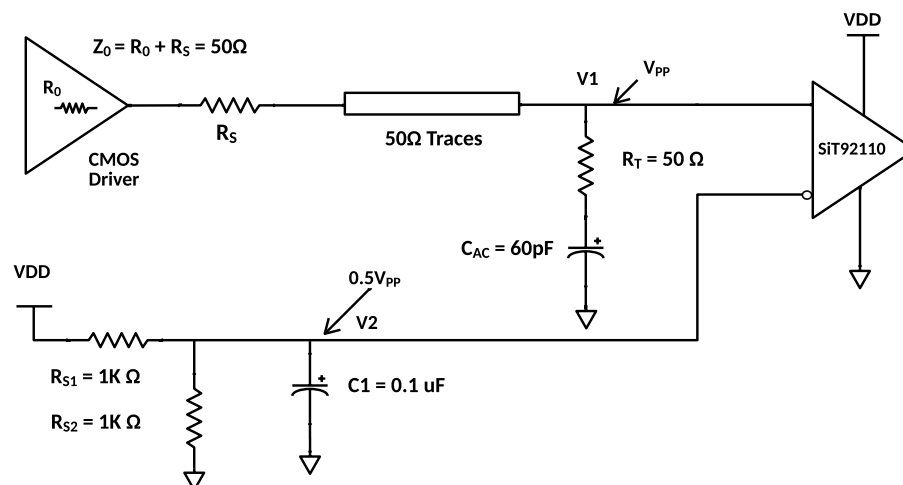


Figure 9 DC coupled LVCMOS input clock with series RC termination – configuration 3

For low frequencies we can direct couple the LVCMOS clock to SiT92110 input clock pin as shown in Figure 10.

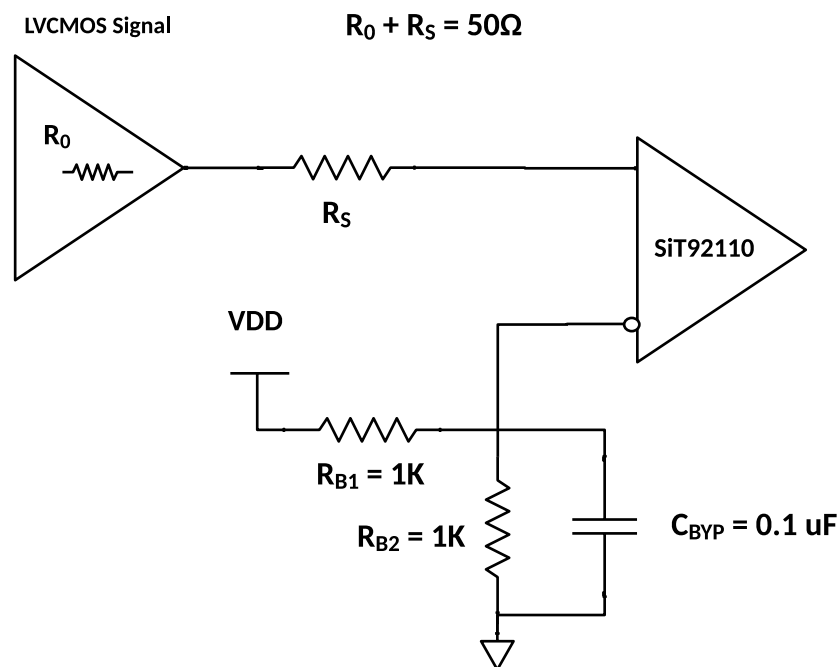


Figure 10: Direct coupling of LVCMOS clock to SiT92110

### Driving XTAL\_IN with LVCMOS Driver (AC coupled)

The crystal input XTAL\_IN can be overdriven with single ended clock (LVCMOS driver or one side of a differential driver). The peak swing at XTAL\_IN should be limited to 1.8 V. The XTAL\_OUT pin, in this case can be floating. The SEL1, SEL0 should be 2'b10. The maximum voltage at XTAL\_IN should not exceed 1.8 V and minimum voltage should not go below -0.5 V. The slew rate at XTAL\_IN should be greater than 0.2 V/ns.

For 3.3 V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 11 shows an example of the interface diagram for a high speed 3.3 V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver

crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_{T1}$  and  $R_{T2}$  in parallel should equal the transmission line impedance. For most 50  $\Omega$  applications,  $R_{T1}$  and  $R_{T2}$  can be 100  $\Omega$ .

$$Z_o = R_o + R_s = 50 \text{ Ohm}$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50 \text{ Ohm}$$

$$\frac{VDD * R_{T2}}{R_{T1} + R_{T2}} = \frac{VDD}{2}$$

For both the AC coupled configurations, the maximum peak to peak swing before the ac coupling capacitor is 1.8V. The maximum DC bias voltage of XTAL\_IN is 0.675V. Therefore the maximum swing at the XTAL\_IN pin is given by the equation given below.

$$V_{swing,pk,XTAL\_IN} = 0.675 + 0.5 * 1.8 = 1.575V$$

( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the

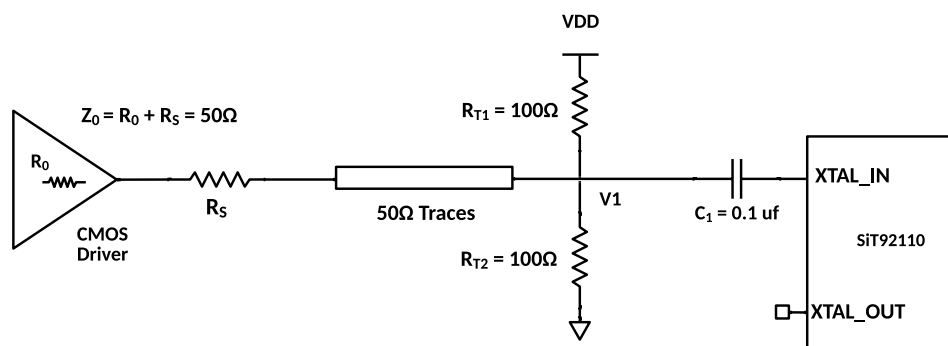


Figure 11 Single ended LVCMOS input – configuration 1, AC coupling to crystal input

Figure 12 shows a second input clock configuration where  $R_{T1}$ ,  $R_{T2}$  are removed and replaced with a  $50\Omega$

termination resistor  $R_T$  to ground. A  $0.1\mu\text{F}$  is in series with the CMOS driver to prevent any DC leakage current.

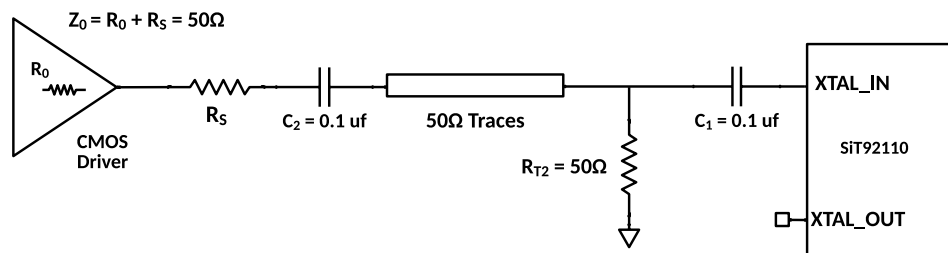


Figure 12 Single ended LVCMOS input – configuration 2, AC coupling to crystal input

### Driving XTAL\_IN with LVCMOS Driver (DC coupled)

The crystal input XTAL\_IN can be overdriven with single ended clock as shown in Figure 13 in DC coupled mode. The peak swing at XTAL\_IN should be limited to 1.8 V. The

XTAL\_OUT pin, in this case can be floating. The SEL1, SEL0 should be 2'b11. If the LVCMOS driver is on higher supply, say 3.3 V, use a resistor divider on the PCB to scale down the peak output voltage to 1.8 V

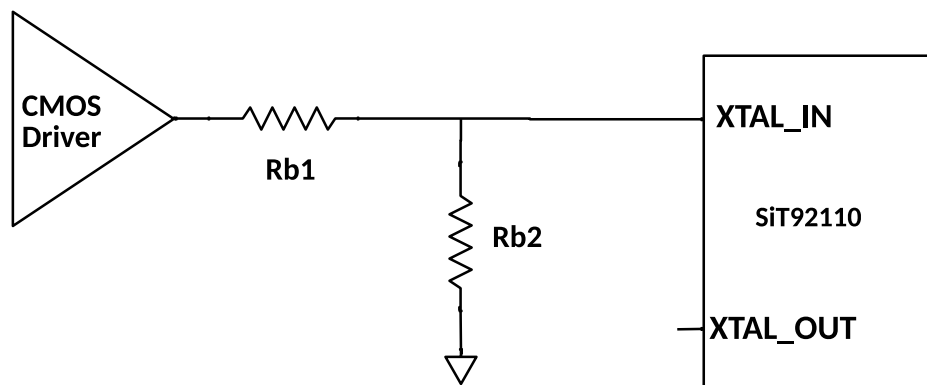


Figure 13 Single ended LVCMOS input, DC coupling to crystal input

## LVDS (DC coupled)

Terminate with a differential 100  $\Omega$  as close to the receiver as possible. This is shown in [Figure 14](#).

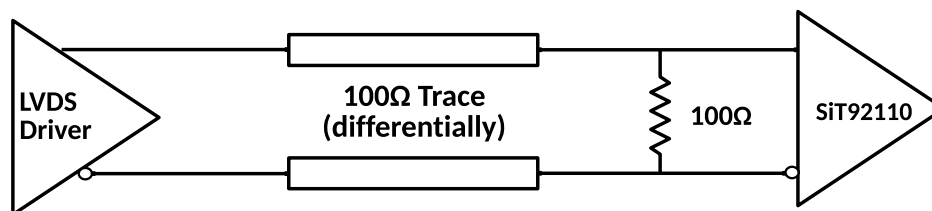


Figure 14 Termination scheme for DC coupled LVDS

## HCSL (DC coupled)

Termination resistor is 50  $\Omega$  to ground, close to the output driver. A series resistance  $R_S$  is sometimes used to limit the

overshoot during fast transients. The termination scheme is shown in [Figure 15](#).

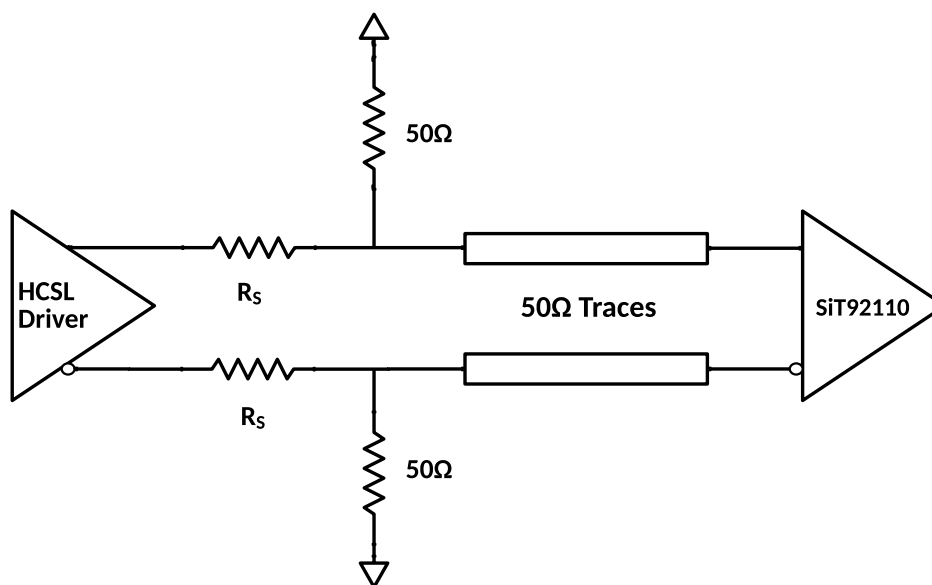


Figure 15 Termination scheme for DC coupled HCSL

## LVPECL (DC coupled)

For DC coupled operation, the 50  $\Omega$  termination resistors are placed close to the receiver. The termination resistors are biased with a voltage source  $V_{TT}$ .

$$V_{TT} = V_{DDO} - 2V.$$

This termination scheme is shown in [Figure 16](#). Alternatively, the user can also implement a Thevenin

equivalent of  $V_{TT}$  using a resistor divider. This scheme and the values of the resistors in the resistor divider are given in [Figure 17](#).

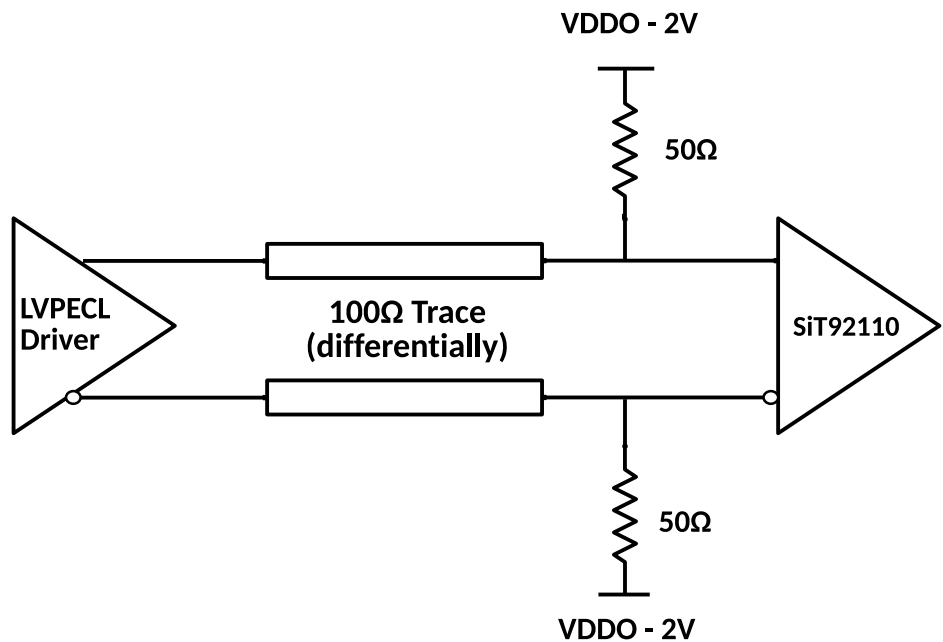
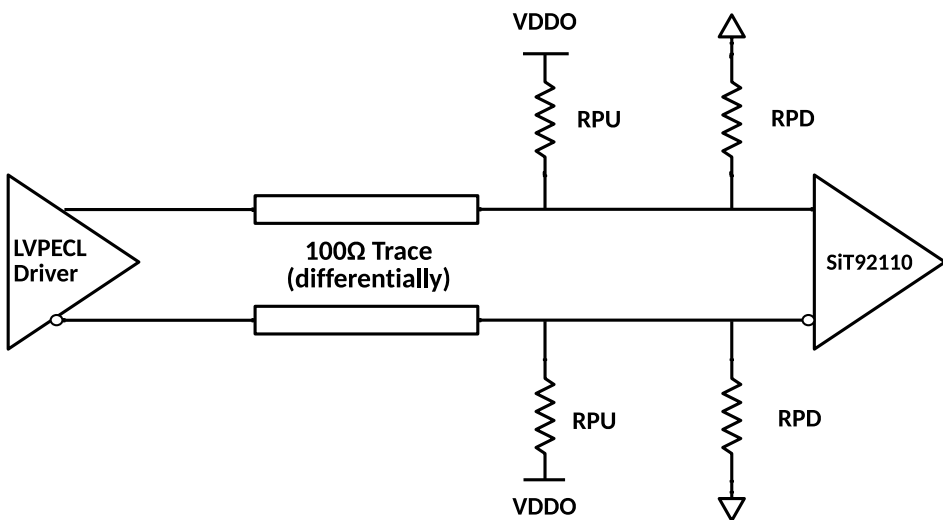


Figure 16 Termination scheme for DC coupled LVPECL.



| VDDO  | RPU   | RPD    | VTT    |
|-------|-------|--------|--------|
| 3.3 V | 120 Ω | 82 Ω   | ~1.3 V |
| 2.5 V | 250 Ω | 62.5 Ω | 0.5 V  |

Figure 17 Termination scheme for DC coupled LVPECL, Thevenin equivalent

The design equations for the LVPECL Thevenin equivalent termination are given below.

$$\frac{R_{PD} * R_{PU}}{R_{PD} + R_{PU}} = 50\Omega$$

$$\frac{R_{PD} * VDDO}{R_{PD} + R_{PU}} = VDDO - 2V$$

## SSTL (DC coupled)

The SSTL input clock configuration is shown in [Figure 18](#). The transmission line impedance is 60  $\Omega$  in the application

example given. Therefore, we use two 120  $\Omega$  resistors from VDDO to ground for biasing the clock input pins. The effective termination impedance in this case is 60  $\Omega$ .

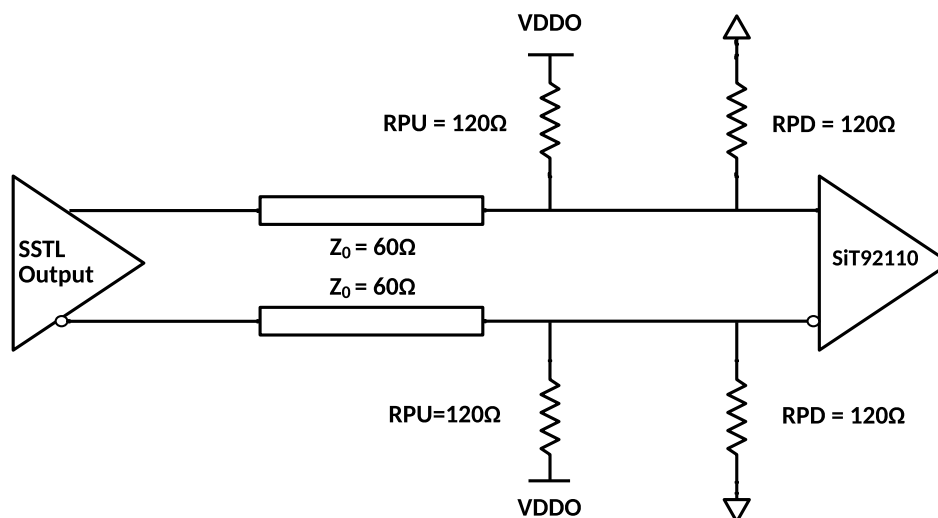


Figure 18 Example of input clock termination for SSTL clock.

## LVDS (AC coupled)

The load termination resistor should be placed before the AC coupling capacitors. The load termination resistor and

the AC coupling capacitors should be placed close to the receiver. The termination scheme is shown in [Figure 19](#).

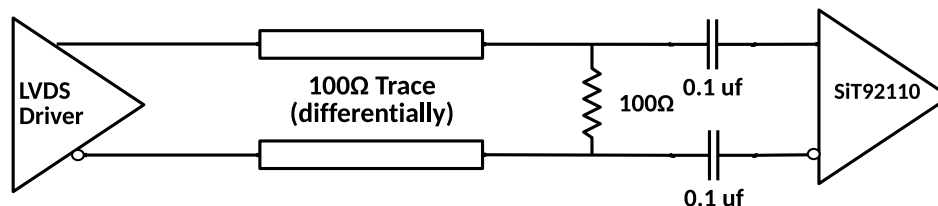
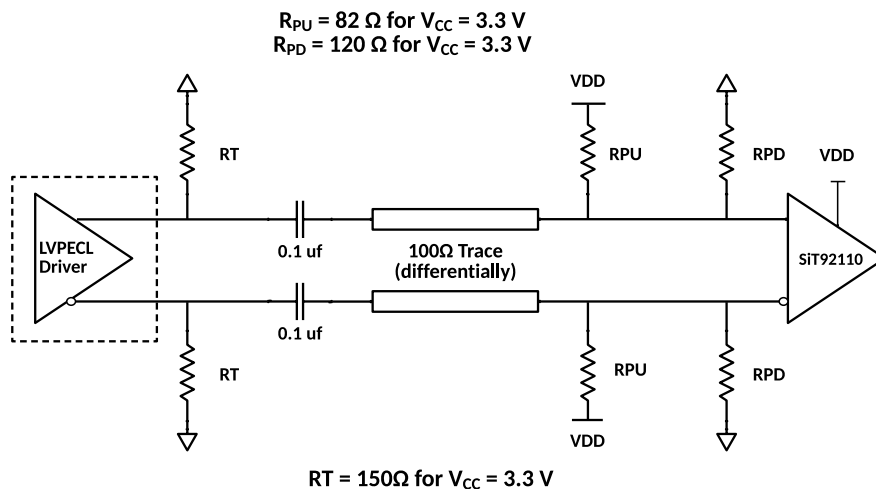


Figure 19 Termination scheme for AC coupled LVDS

## LVPECL (AC coupled)

The LVPECL should have a DC path to ground. So, the user must place a resistance  $R_T$ , close to the output driver. The

LVPECL AC coupling and Thevenin equivalent VTT termination scheme is shown in [Figure 20](#)



**Figure 20 Termination scheme for AC coupled LVPECL, Thevenin Equivalent**

The pull up resistance  $R_{PU}$  and pull down resistance  $R_{PD}$  sets the input common mode voltage for SiT92110. The value of the input common mode voltage can be estimated by the equation given below

$$V_{ICM} = \frac{V_{DD} * R_{PD}}{R_{PU} + R_{PD}} = \frac{3.3 * 120}{120 + 82} = 1.961V$$

The differential input common mode specification of SiT92110 (from data sheet) is  $V_{DD} - 1.1 = 2.2 V$ , therefore the input common mode set by LVPECL AC coupled

termination meets the SiT92110 input common mode specification.

The LVPECL driver chip has resistance  $R_T$  providing DC path for the output driver current in the LVPECL driver. The effective load impedance at the input side of SiT92110 (receiver side) is formed by parallel combination of  $R_{PU}$ ,  $R_{PD}$ .

The effective termination resistor value is given by the equation below

$$R_{termination} = \frac{R_{PU} * R_{PD}}{R_{PU} + R_{PD}} = \frac{120 * 82}{120 + 82} = 48.7 \Omega$$

## Termination of Output Driver of SiT92110 for Various Load Configurations

### SiT92110 Output ODR Termination for AC Coupled mode

AC coupling of SiT92110 LVCMOS output driver is shown in [Figure 21](#). We use single termination resistor of  $50 \Omega$ s to ground. A  $0.1 \mu F$  AC coupling capacitor is connected in series with the LVCMOS clock source to prevent DC leakage current. The receiver side is terminated with a single  $50 \Omega$  resistance to ground. The clock signal is then

AC coupled to the receiver, in this example.  $C_1$  is a bypass capacitor that is used to suppress noise on the inverting differential input of the receiver.

$$Z_o = R_o + R_s = 50 \text{ Ohm}$$

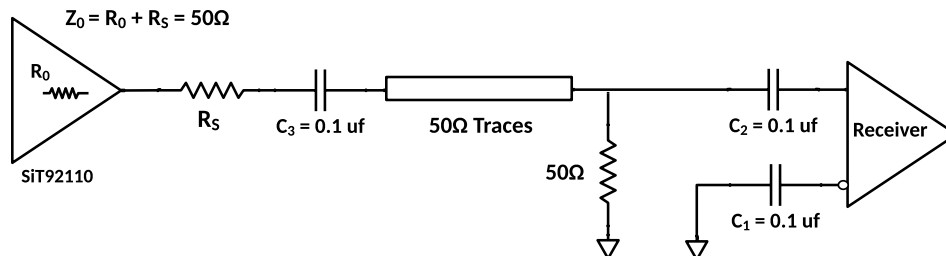


Figure 21 AC coupling of LVCMOS clock with single 50 Ω resistor termination to ground

### SiT92110 Output ODR Termination for DC Coupled mode

Figure 22 shows how SiT92110 LVCMOS output drive can be terminated to send clock signals in DC coupled mode. The reference voltage  $V1 = VDD/2$  is generated by the bias resistors  $RS1$  and  $RS2$ . The bypass capacitor ( $C1$ ) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of  $RS1$  and  $RS2$  might need to be adjusted to position the bias voltage  $V2$  in the center of the input voltage swing.

$$Z_o = R_o + R_s = 50 \text{ Ohm}$$

$$\frac{VDD * R_{S2}}{R_{S1} + R_{S2}} = \frac{VDD}{2},$$

$$\text{Typical value of } R_{S1} = R_{S2} = 1K\Omega$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50 \text{ Ohm},$$

$$\text{Typical value of } R_{T1} = R_{T2} = 100\Omega$$

$$\frac{VDD * R_{T2}}{R_{T1} + R_{T2}} = \frac{VDD}{2}$$

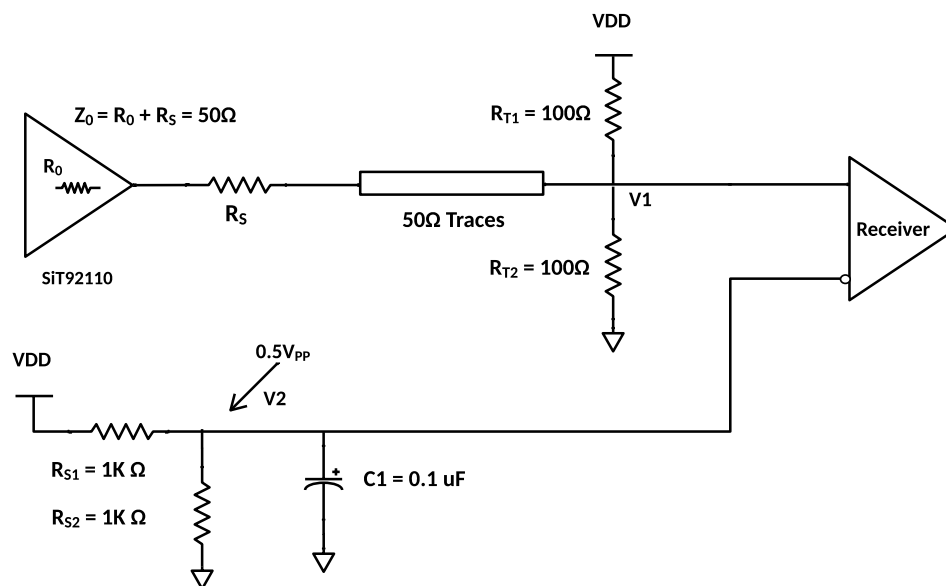


Figure 22 DC coupling of LVCMOS output clock termination – configuration 1

For example, if the SiT92110 supply is 2.5 V then the DC offset (or swing center) of this signal is 1.25 V, the  $RS1$  and  $RS2$  values should be adjusted to set the  $V2$  at 1.25 V. The

values below are for when both the single ended swing and VDD are at the same voltage.



This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First,  $R_{T1}$  and  $R_{T2}$  in parallel should equal the transmission line impedance. For most 50  $\Omega$  applications,  $R_{T1}$  and  $R_{T2}$  can be 100  $\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 23 shows a second input clock configuration where  $R_{T1}$ ,  $R_{T2}$  are removed and replaced with a  $50\ \Omega$  termination resistor  $R_T$  to ground. There will be DC leakage current from SiT92110, for the output termination shown in Figure 23. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 23 is given below

$$Z_o = R_o + R_s = 50 \, \Omega$$

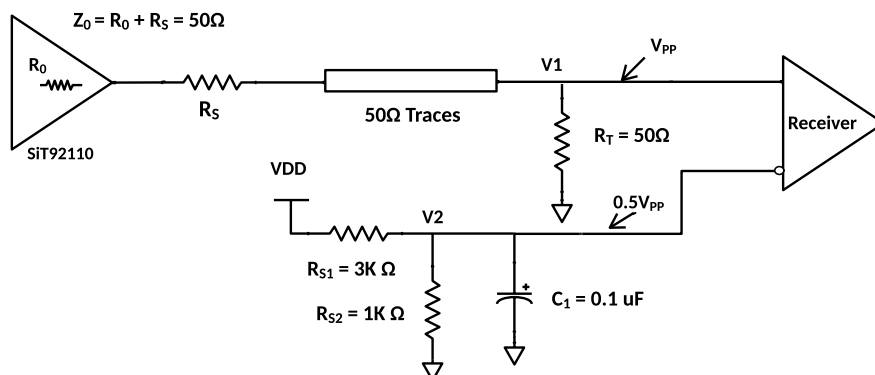
$$\frac{VDD * R_{s2}}{R_{s1} + R_{s2}} = \frac{V_{pp}}{2} = \frac{VDD}{4},$$

Typical value of  $R_{s1} = 3K\Omega, R_{s2} = 1K\Omega$

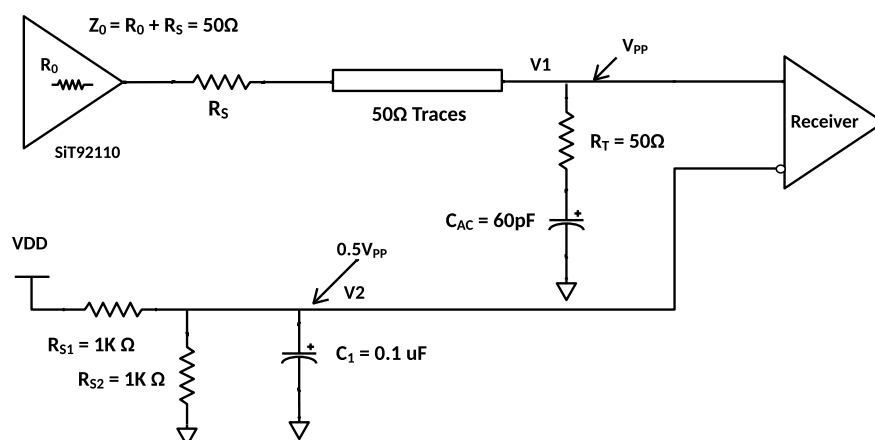
The SiT92110 LVCMOS output driver termination with series RC termination near the buffer is shown in [Figure 24](#). There is a single termination resistor  $R_T$  which is connected to ground through a capacitor  $C_{AC}$ . The value of series capacitor is given by a formula.

$$C_{AC} \geq \frac{3T_D}{50\Omega}, T_D \text{ is the transmission line delay}$$

Typical value for  $C_{AC}$  is 60 pF, assuming delay of  $T_D = 200$  ps/inch and 5 inch input clock route length.



**Figure 23 DC coupled LVCMOS output clock configuration – configuration 2**

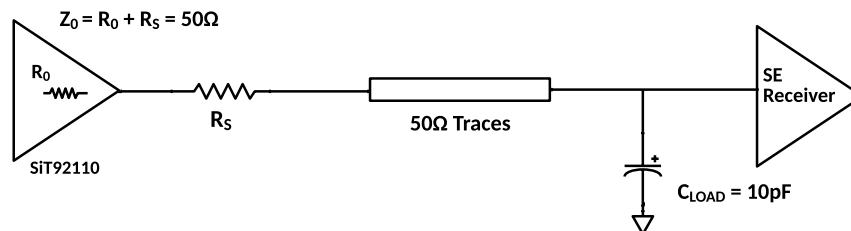


**Figure 24 DC coupled LVCMOS output clock with series RC termination – configuration 3**

The typical value of  $R_{S1}$  and  $R_{S2}$  in this case is 1 K $\Omega$  and that of  $C_{AC}$  is 60 pF.

## CMOS (Capacitive load)

The capacitive load can be driven as shown in [Figure 25](#).  $R_S = 33\ \Omega$  for  $V_{DDO} = 3.3\text{ V}$ .



**Figure 25 Typical application load**

## Power Considerations

The following power consideration refers to the device-consumed power consumption only. The device power consumption is the sum of static power and dynamic power. The dynamic power usage consists of two components:

- Power used by the device as it switches states

- Power required to charge any output load. The output load can be capacitive-only or capacitive and resistive. Use the following formula to calculate the power consumption of the device:

$$P_{DEV} = P_{STATIC} + P_{DYNAMIC} + P_{CLOAD}$$

$$P_{STATIC} = I_{CORE\_STATIC} * VDD + I_{ODR\_STATIC} * VDDO$$

$$P_{DYNAMIC} = I_{CORE\_DYNAMIC\_100MHZ} * VDD * \frac{F_{in}(\text{units in MHz})}{100} + C_{PD} * 10 * F_{in} * VDDO^2$$

$$P_{CLOAD} = C_{LOAD} * 10 * F_{in} * VDDO^2$$

Let us calculate typical power dissipation for CLOAD of 2 pF at input clock of 100 MHz. Assume that  $VDD = VDDO = 3.3\text{ V}$ .

$$P_{STATIC} = 16mA * 3.3V + 3.5mA * 3.3V = 64.35mW$$

$$P_{DYNAMIC} = 1.5mA * \frac{100}{100} * 3.3V + 4.0pF * 1 * 100MH * 3.3V * 3.3V = 48.51\text{ mW}$$

$$P_{CLOAD} = 2pF * 10 * 100MHz * 3.3V * 3.3V = 21.78mW$$

### Core Current in XO Mode

The crystal mode standalone block current is measured in ATE. We can calculate total VDD core current in crystal

mode, in typical condition using the below equation. The worst case VDD core current will be 14 mA, in crystal mode.

$$I_{core\_crystal} = 8.5 + I_{xo\_standalone} = 11.5mA, typical$$

$$P_{DEV} = 134.64mW$$

### Parameter Measurement Information

#### Differential Input Level

The parameter definitions related to differential input level is shown in [Figure 26](#).

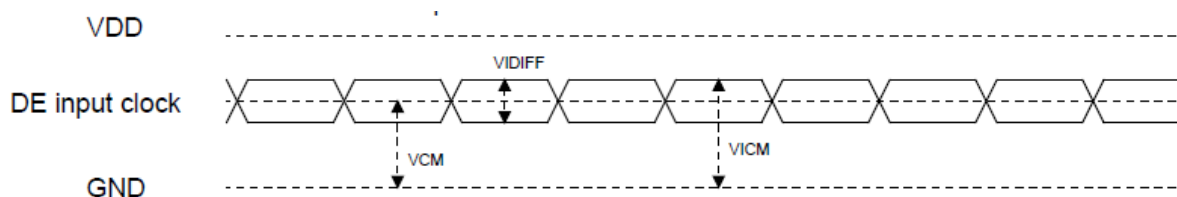


Figure 26 Parameters related to differential input level

#### Skew and Input to Output Delay

The parameter definitions related to propagation delay and skew are shown in [Figure 27](#).

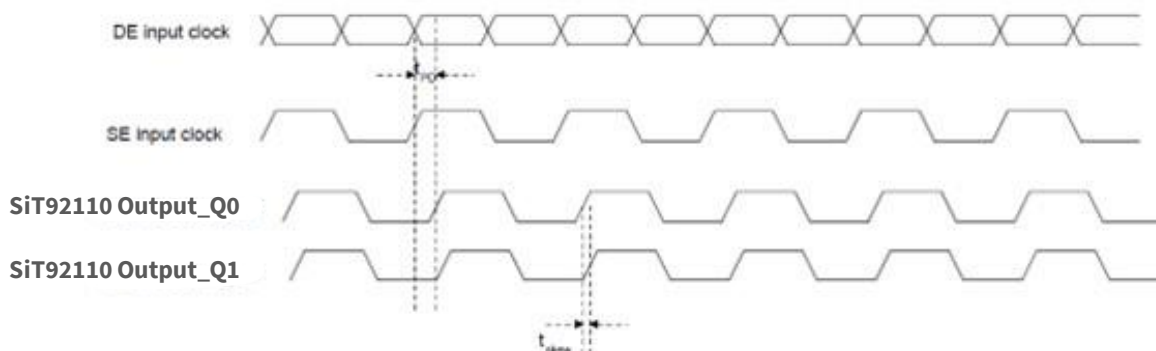


Figure 27 Parameter definitions of propagation delay and skew

### Rise and Fall Times

The parameter definitions related to propagation rise and fall times are shown in [Figure 28](#).

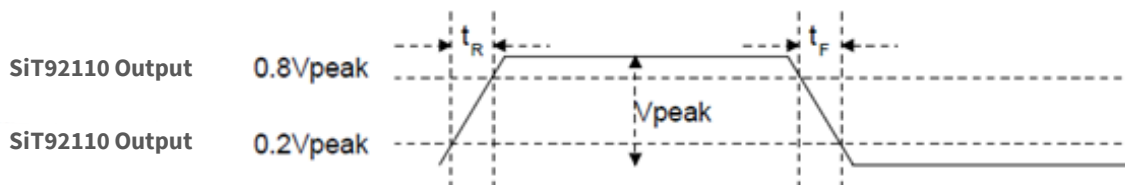


Figure 28 Parameter definitions related to rise and fall times

### Isolation

Isolation is a measure of the coupling of clock toggling in unselected input clock path on the output clock. Let us say that CLOCK0 path is selected and there the clock frequency is 156.5 MHz at 0 dBm power. If a clock is toggling in CLOCK1 path at 156 MHz at 0 dBm, then there may be a tone at an offset of 0.5 MHz from the carrier, in the output clock. The power of this tone with respect to the carrier is called isolation.

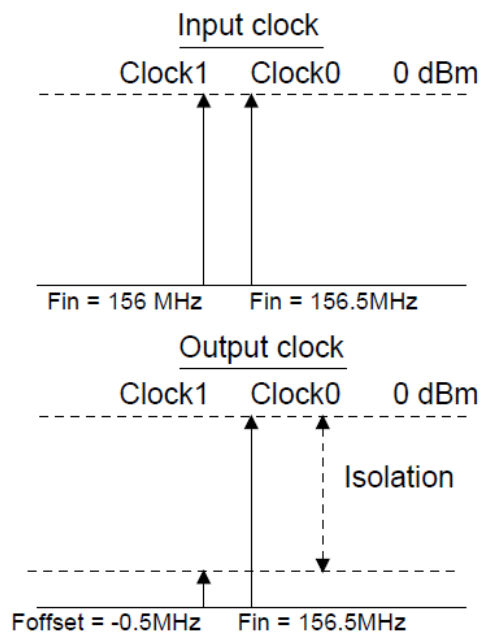


Figure 29 Parameter definition of isolation

Thermal Information

Table 10 Thermal Metrics of SiT92110

| Thermal Metric                                                     | SiT92110<br>RHB<br>32 pins | Units |
|--------------------------------------------------------------------|----------------------------|-------|
| $\theta_{JA}$ Junction to ambient thermal resistance, flow = 0 m/s | 43.4                       | °C/W  |
| $\theta_{JA}$ Junction to ambient thermal resistance, flow = 1 m/s | 38.7                       | °C/W  |
| $\theta_{JA}$ Junction to ambient thermal resistance, flow = 2 m/s | 37.4                       | °C/W  |
| $\theta_{JB}$ Junction to board                                    | 16.62                      | °C/W  |
| $\theta_{JC}$ Junction to case                                     | 23.7                       | °C/W  |
| $\psi_{JT}$ Junction to top characterization parameter             | 0.75                       | °C/W  |

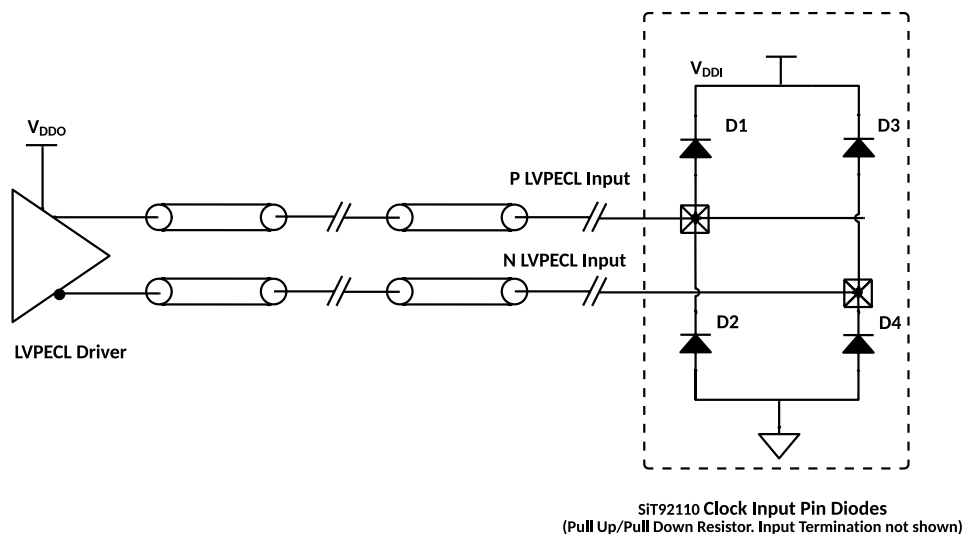
## HOT Swap Recommendations

### Introduction

Hot-swap is a term used to refer to the insertion and removal of a dSighter card from a backplane without powering down the system power. With today's high speed data and redundancy requirements, many systems are required to run continuously without being powered down. If special considerations are not taken, the device can be damaged.

### Typical Differential Input Clock

For example, Figure 30 shows a typical LVPECL driver and differential input. If the power of the driver (VDDO) is turned on before the input supply (VDDI), there is a possibility that the input current could exceed the limit and damage diode D1.



**Figure 30 Typical input differential clock**

To ensure the input current does not exceed its limit and damage the device, a current limiting resistor can be used. Below are examples of the most common termination topologies using a series current limiting resistor. Though

it's not necessary, but if board space allows, some of the examples have an optional 100pf capacitor which assists with the integrity of the rise time. It is also recommended that the current limiting resistor be as close to the receiver as possible.

## Input Clock Termination with Hot Swap Protection

### LVPECL Termination Example

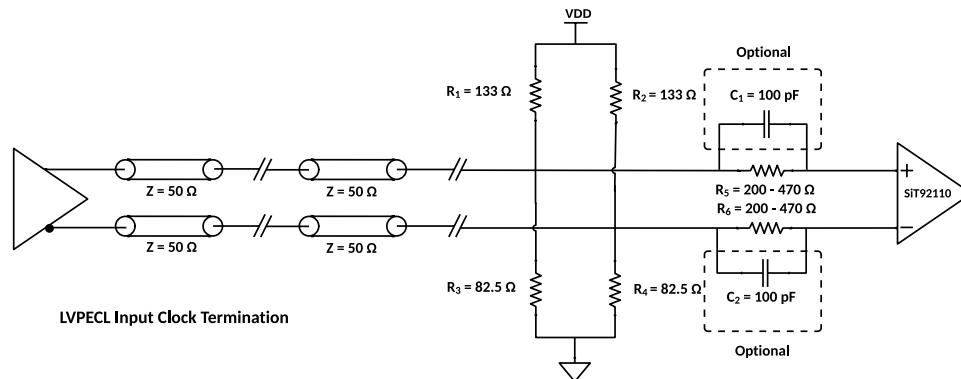


Figure 31 LVPECL termination with hot swap protection

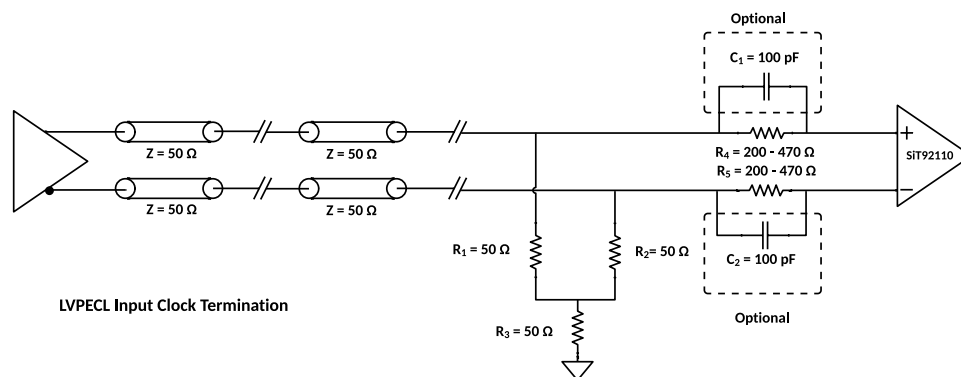


Figure 32 LVEPCL termination with hot swap protection

## LVDS Input Clock Termination Example

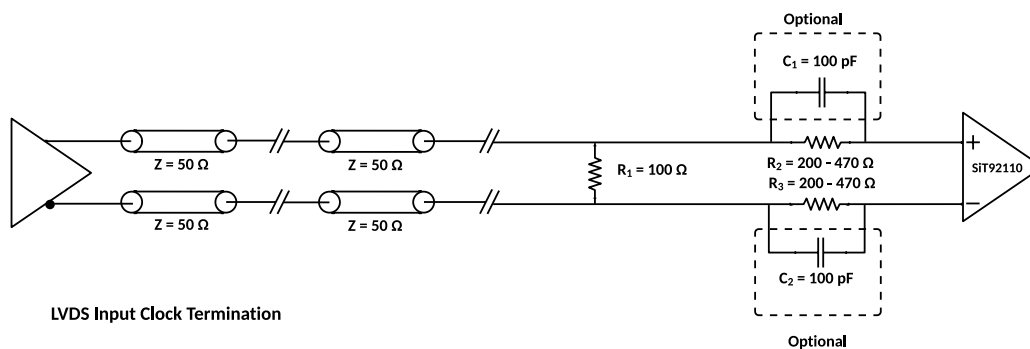


Figure 33 LVDS termination with hot swap protection

## HCSL Input Clock Termination Example

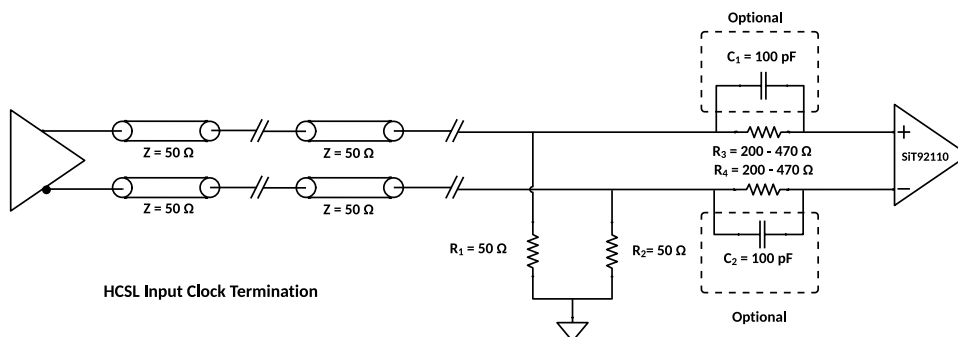


Figure 34 HCSL termination with hot swap protection



## LVCMOS Input Clock Termination with Hot Swap Protection

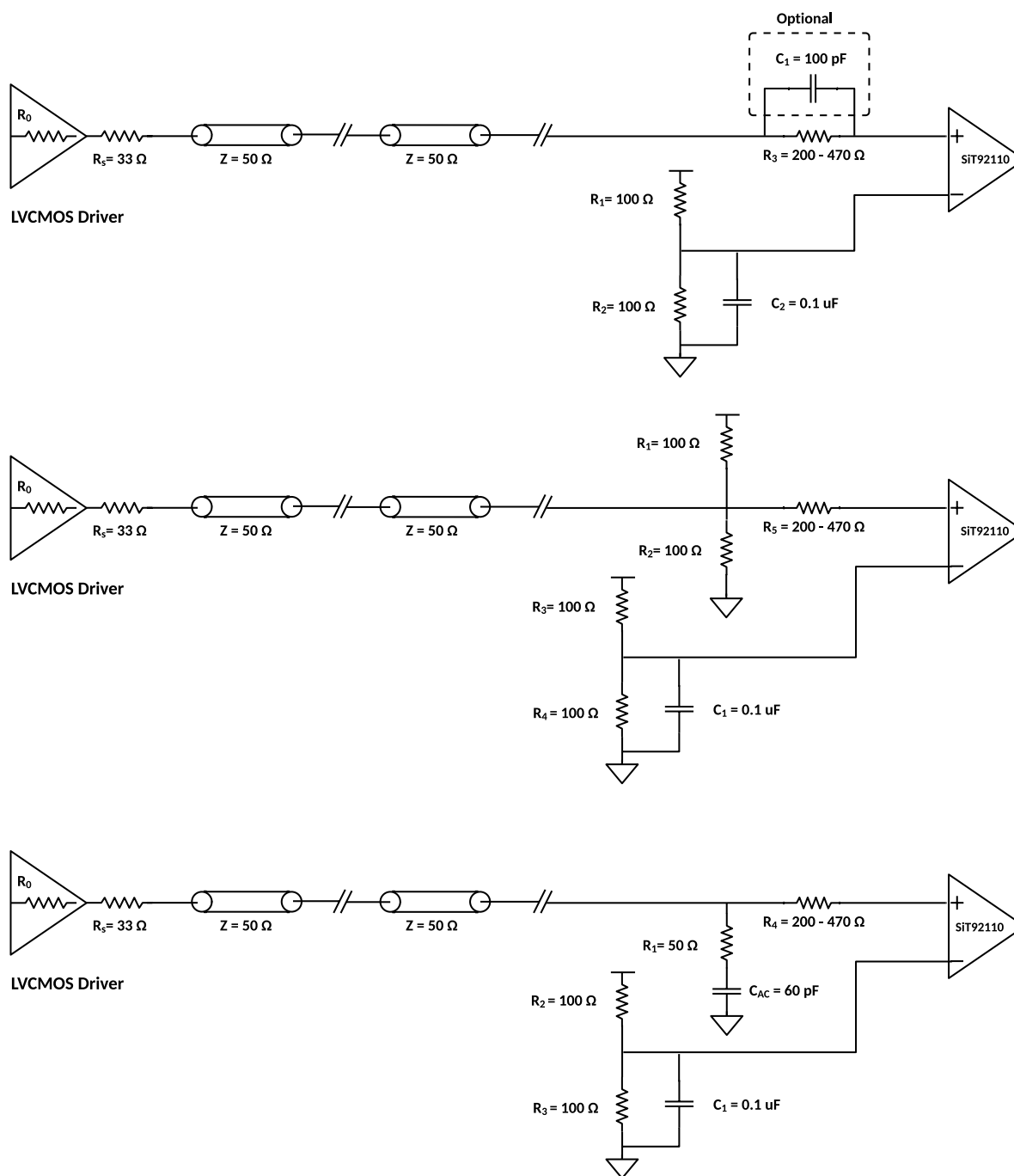


Figure 35 LVCMOS input clock termination with hot swap protection

## LVCMOS Output Clock Termination with Hot Swap Protection

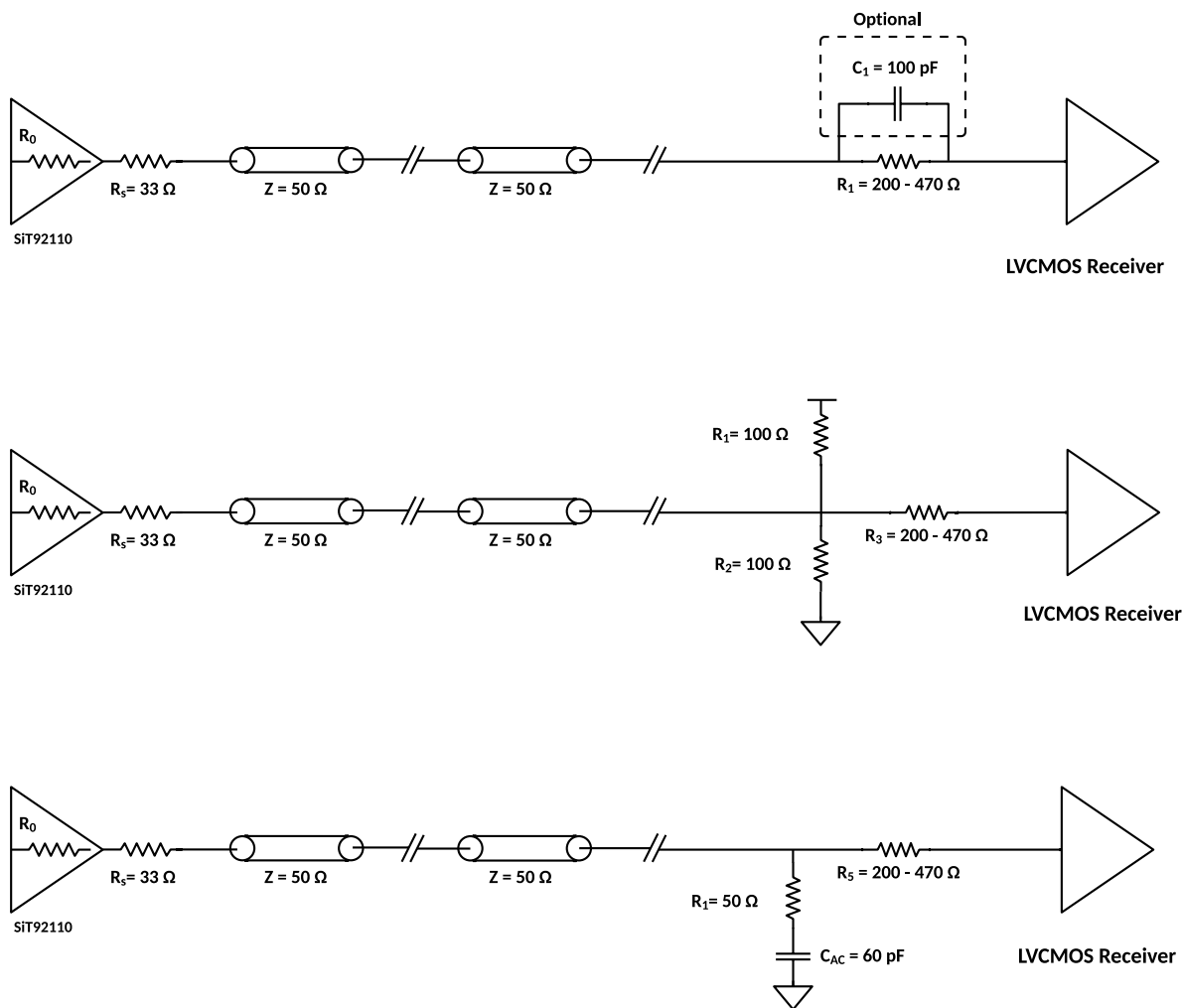


Figure 36 Different types of LVCMOS output clock termination with hot swap protection

## Operation in Multiple VDDO Supply Domains

The VDDO pins, 2 and 6 on the left side are shorted internally. These pins along with ODR Q0 to Q4 belong to a single supply domain. The VDDO pins, 23 and 19 on the left side are shorted internally. These pins along with ODR Q5 to Q9 belong to a single supply domain. These two supply

domains are totally independent of each other. Pin 2, 6 can be connected to say 3.3 V while pin 23, 19 can be connected to 1.8 V. In this example, Q0 to Q4 will be 3.3 V LVCMOS driver. Q5 to Q9 will be 1.8 V LVCMOS driver.

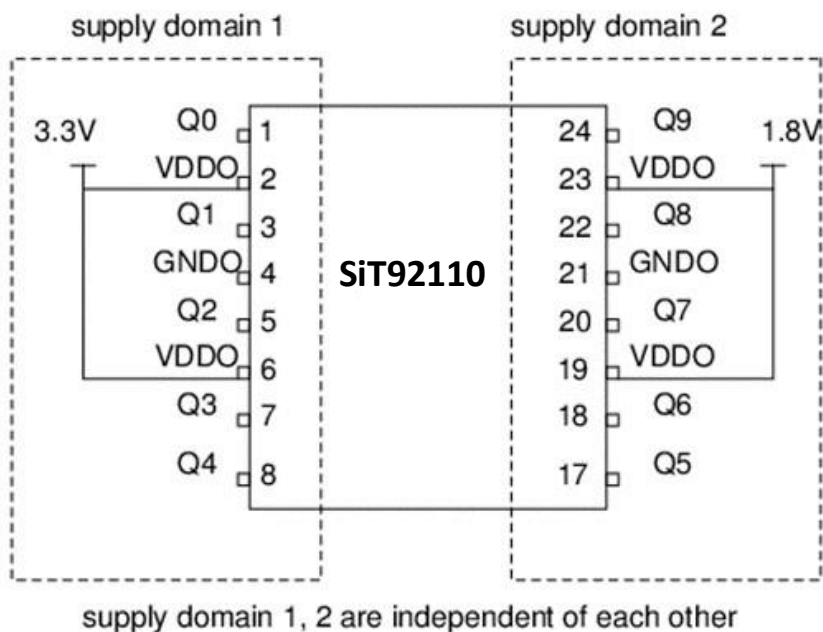
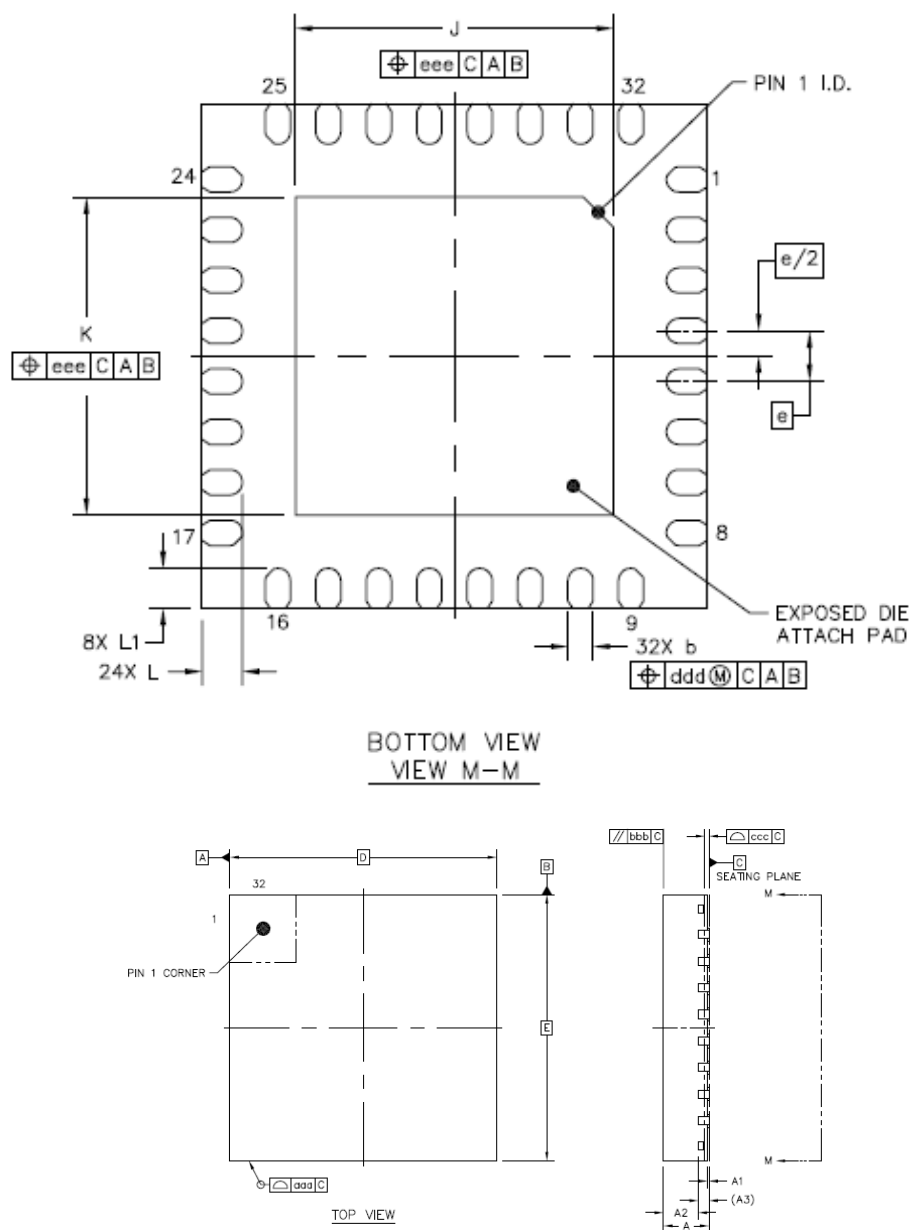


Figure 37: Example of multi supply operation of SiT92110

## Package Dimensions and Patterns



### Figure 38 SiT92110 32 pin QFN package dimensions

|                        |   | SYMBOL | MILLIMETER |       |      |
|------------------------|---|--------|------------|-------|------|
|                        |   |        | MIN        | NOM   | MAX  |
| Total Thickness        |   | A      | 0.8        | 0.85  | 0.90 |
| Stand Off              |   | A1     | 0          | 0.035 | 0.05 |
| Mold Thickness         |   | A2     | -          | 0.65  | -    |
| L/F Thickness          |   | A3     | 0.203 REF  |       |      |
| Lead Width             |   | b      | 0.2        | 0.25  | 0.3  |
| Body Size              | X | D      | 5 BSC      |       |      |
|                        | Y | E      | 5 BSC      |       |      |
| Lead Pitch             |   | e      | 0.5 BSC    |       |      |
| EP Size                | X | J      | 3.05       | 3.15  | 3.25 |
|                        | Y | K      | 3.05       | 3.15  | 3.25 |
| Lead Length            |   | L      | 0.35       | 0.4   | 0.45 |
|                        |   | L1     | 0.3        | 0.4   | 0.35 |
| Package Edge Tolerance |   | aaa    | 0.1        |       |      |
| Mold Flatness          |   | bbb    | 0.1        |       |      |
| Coplanarity            |   | ccc    | 0.08       |       |      |
| Lead Offset            |   | ddd    | 0.1        |       |      |
| Exposed Pad Offset     |   | eee    | 0.1        |       |      |

Table 11. Revision History

| Revisions | Release Date | Change Summary  |
|-----------|--------------|-----------------|
| 0.5       | Nov 9, 2023  | Initial Release |

**SiTime Corporation**, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439

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